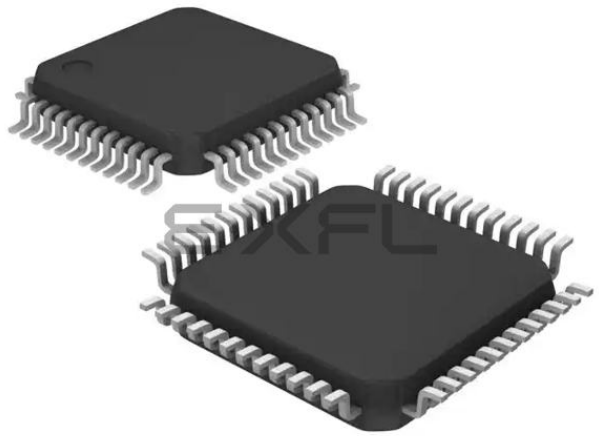

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc120ld2dn

List of Figures

4.2 Pin Configuration

4.2.1 NuMicro® NUC100 Pin Diagram

4.2.1.1 NuMicro® NUC100VxxDN LQFP 100 pin

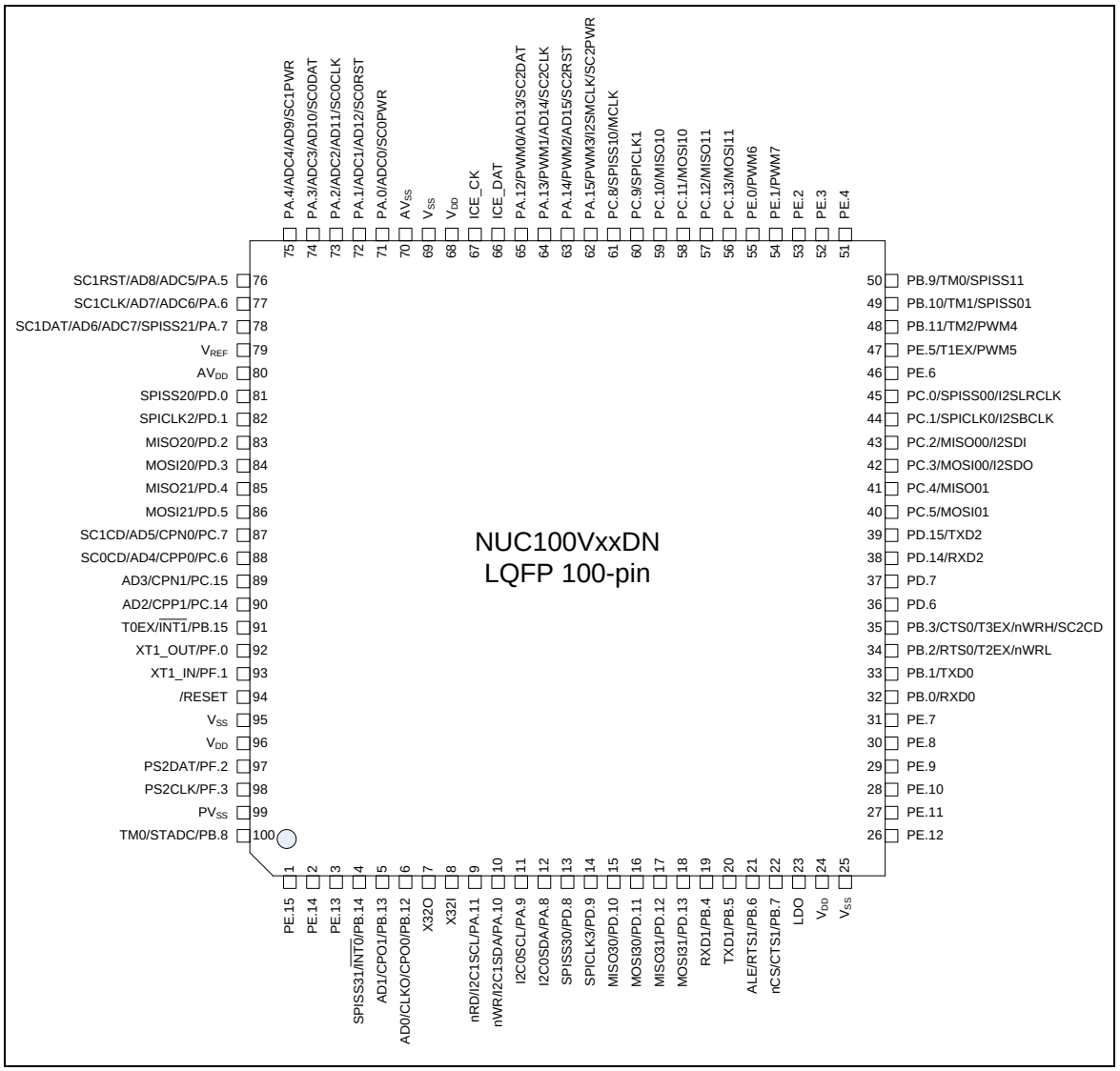

Figure 4-2 NuMicro® NUC100VxxDN LQFP 100-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			T1EX	I	Timer1 external capture input pin.
48	30	22	PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49	31	23	PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPISS01	I/O	2nd SPI0 slave select pin.
50	32	24	PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPISS11	I/O	2nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			MOSI11	I/O	2nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			MISO11	I/O	2nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			MOSI10	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			MISO10	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	I/O	General purpose digital I/O pin.
			SPICLK1	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			SPISS10	I/O	1st SPI1 slave select pin.
			MCLK	O	EBI external clock output pin
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.

4.3.2 NuMicro® NUC120 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	**I/O**	General purpose digital I/O pin.
2			PE.14	**I/O**	General purpose digital I/O pin.
3			PE.13	**I/O**	General purpose digital I/O pin.
4	1		PB.14	**I/O**	General purpose digital I/O pin.
			/INT0	**I**	External interrupt0 input pin.
			SPISS31	**I/O**	2nd SPI3 slave select pin.
5	2		PB.13	**I/O**	General purpose digital I/O pin.
			CPO1	**O**	Comparator1 output pin.
			AD1	**I/O**	EBI Address/Data bus bit1
6	3	1	PB.12	**I/O**	General purpose digital I/O pin.
			CPO0	**O**	Comparator0 output pin
			CLKO	**O**	Frequency Divider output pin
			AD0	**I/O**	EBI Address/Data bus bit0
7	4	2	X32O	**O**	External 32.768 kHz low speed crystal output pin
8	5	3	X32I	**I**	External 32.768 kHz low speed crystal input pin
9	6	4	PA.11	**I/O**	General purpose digital I/O pin.
			I2C1SCL	**I/O**	I^2C1 clock pin.
			nRD	**O**	EBI read enable output pin
10	7	5	PA.10	**I/O**	General purpose digital I/O pin.
			I2C1SDA	**I/O**	I^2C1 data input/output pin.
			nWR	**O**	EBI write enable output pin
11	8	6	PA.9	**I/O**	General purpose digital I/O pin.
			I2C0SCL	**I/O**	I^2C0 clock pin.
12	9	7	PA.8	**I/O**	General purpose digital I/O pin.
			I2C0SDA	**I/O**	I^2C0 data input/output pin.
13			PD.8	**I/O**	General purpose digital I/O pin.
			SPISS30	**I/O**	1st SPI3 slave select pin.
14			PD.9	**I/O**	General purpose digital I/O pin.
			SPICLK3	**I/O**	SPI3 serial clock pin.
15			PD.10	**I/O**	General purpose digital I/O pin.
			MISO30	**I/O**	1st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	**I/O**	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			MOSI30	**I/O**	1st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	**I/O**	General purpose digital I/O pin.
			MISO31	**I/O**	2nd SPI3 MISO (Master In, Slave Out) pin.
18			PD.13	**I/O**	General purpose digital I/O pin.
			MOSI31	**I/O**	2nd SPI3 MOSI (Master Out, Slave In) pin.
19	10	8	PB.4	**I/O**	General purpose digital I/O pin.
			RXD1	**I**	Data receiver input pin for UART1.
20	11	9	PB.5	**I/O**	General purpose digital I/O pin.
			TXD1	**O**	Data transmitter output pin for UART1.
21	12		PB.6	**I/O**	General purpose digital I/O pin.
			RTS1	**O**	Request to Send output pin for UART1.
			ALE	**O**	EBI address latch enable output pin
22	13		PB.7	**I/O**	General purpose digital I/O pin.
			CTS1	**I**	Clear to Send input pin for UART1.
			nCS	**O**	EBI chip select enable output pin
23	14	10	LDO	**P**	LDO output pin
24	15	11	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
25	16	12	V_{SS}	**P**	Ground pin for digital circuit.
26			PE.8	**I/O**	General purpose digital I/O pin.
27			PE.7	**I/O**	General purpose digital I/O pin.
28	17	13	VBUS	**USB**	Power supply from USB host or HUB.
29	18	14	V_{DD33}	**USB**	Internal power regulator output 3.3V decoupling pin.
30	19	15	D-	**USB**	USB differential signal D-.
31	20	16	D+	**USB**	USB differential signal D+.
32	21	17	PB.0	**I/O**	General purpose digital I/O pin.
			RXD0	**I**	Data receiver input pin for UART0.
33	22	18	PB.1	**I/O**	General purpose digital I/O pin.
			TXD0	**O**	Data transmitter output pin for UART0.
34	23	29	PB.2	**I/O**	General purpose digital I/O pin.
			RTS0	**O**	Request to Send output pin for UART0.
			T2EX	**I**	Timer2 external capture input pin.
			nWRL	**O**	EBI low byte write enable output pin

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
75	48	36	PA.4	**I/O**	General purpose digital I/O pin.
			ADC4	**AI**	ADC4 analog input.
			SC1PWR	**O**	SmartCard1 power pin.
			AD9	**I/O**	EBI Address/Data bus bit9
76	49	37	PA.5	**I/O**	General purpose digital I/O pin.
			ADC5	**AI**	ADC5 analog input.
			SC1RST	**O**	SmartCard1 reset pin.
			AD8	**I/O**	EBI Address/Data bus bit8
77	50	38	PA.6	**I/O**	General purpose digital I/O pin.
			ADC6	**AI**	ADC6 analog input.
			SC1CLK	**I/O**	SmartCard1 clock pin.
			AD7	**I/O**	EBI Address/Data bus bit7
78	51	39	PA.7	**I/O**	General purpose digital I/O pin.
			ADC7	**AI**	ADC7 analog input.
			SC1DAT	**O**	SmartCard1 data pin.
			SPISS21	**I/O**	2nd SPI2 slave select pin.
			AD6	**I/O**	EBI Address/Data bus bit6
79			V_{REF}	**AP**	Voltage reference input for ADC.
80	52	40	AV_{DD}	**AP**	Power supply for internal analog circuit.
81			PD.0	**I/O**	General purpose digital I/O pin.
			SPISS20	**I/O**	1st SPI2 slave select pin.
82			PD.1	**I/O**	General purpose digital I/O pin.
			SPICLK2	**I/O**	SPI2 serial clock pin.
83			PD.2	**I/O**	General purpose digital I/O pin.
			MISO20	**I/O**	1st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	**I/O**	General purpose digital I/O pin.
			MOSI20	**I/O**	1st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	**I/O**	General purpose digital I/O pin.
			MISO21	**I/O**	2nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	**I/O**	General purpose digital I/O pin.
			MOSI21	**I/O**	2nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	**I/O**	General purpose digital I/O pin.
			CPN0	**AI**	Comparator0 negative input pin.

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

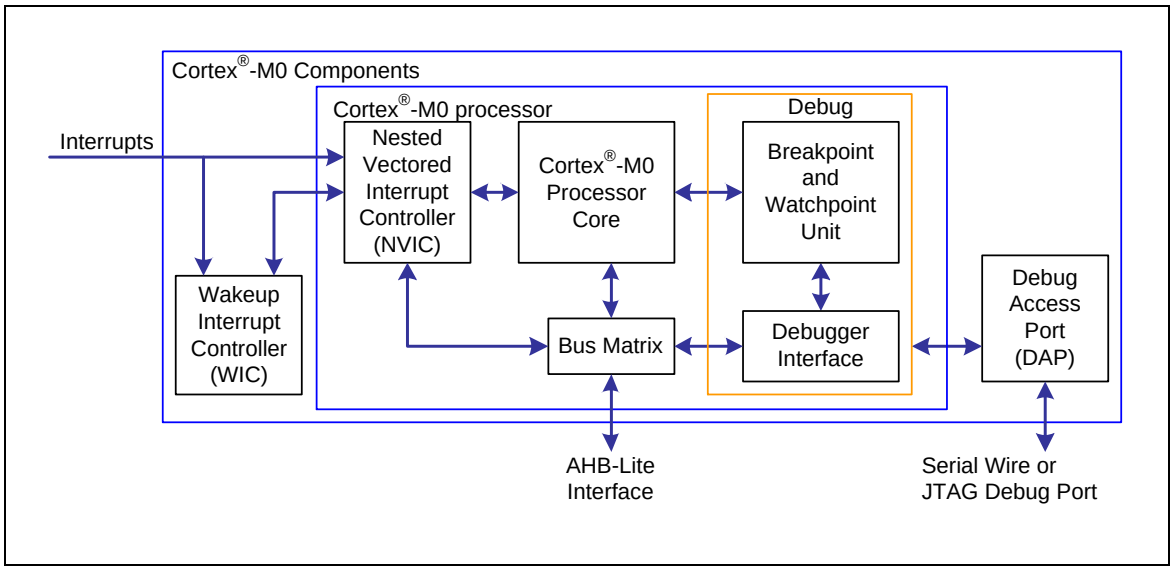

Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from RSTSRC register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIP_RST (IPRSTC1[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPU_RST (IPRSTC1[1])

Power-on Reset or CHIP_RST (IPRSTC1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

(CLKSEL1[1:0])								
XTL12M_STB (CLKSTATUS[0])	0x0	-	-	-	-	-	-	-
XTL32K_STB (CLKSTATUS[1])	0x0	-	-	-	-	-	-	-
PLL_STB (CLKSTATUS[2])	0x0	-	-	-	-	-	-	-
OSC10K_STB (CLKSTATUS[3])	0x0	-	-	-	-	-	-	-
OSC22M_STB (CLKSTATUS[4])	0x0	-	-	-	-	-	-	-
CLK_SW_FAIL (CLKSTATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
WTE (WTCR[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
WTCR	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
WTCRALT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTRLD	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCR	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	-
WWDTSR	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCVR	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-	-
BS (ISPCON[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
DFBADR	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS (ISPSTA[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP (ISPSTA[20:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							-
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6-1 Reset Value of Registers

AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time (16*HCLK cycles), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time. The RSTS_RESET (RSTSRC[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6-5 shows the Low Voltage Reset waveform.

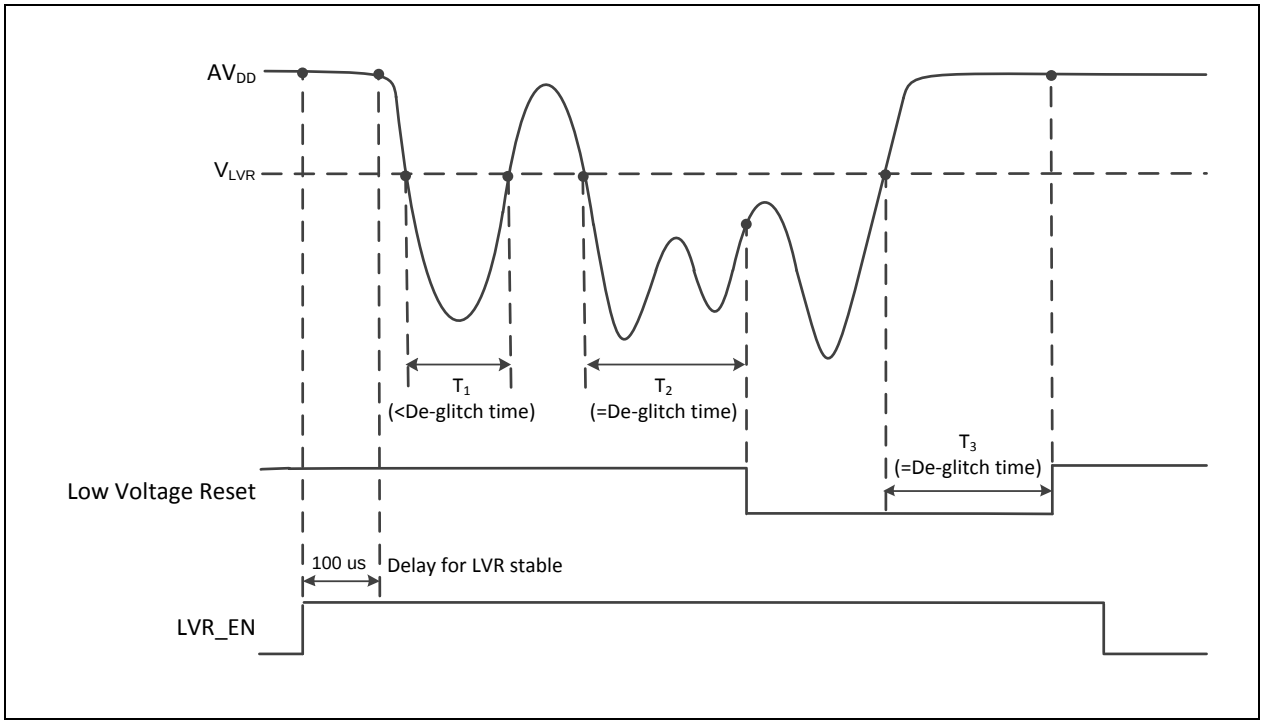

Figure 6-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BOD_EN (BODCR[0]), Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BOD_EN (BODCR[0]) and BOD_VL (BODCR[2:1]) and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BOD_EN, BOD_VL and BOD_RSTEN is set by flash controller user configuration register CBODEN (CONFIG0[23]), CBOV1-0 (CONFIG0[22:21]) and CBORST (CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6-6 shows the Brown-Out Detector waveform.

3. If TIMER clock source is selected as LXT/LIRC and LXT/LIRC is on.
4. If PWM clock source is selected as LXT and LXT is on.
5. If WDT clock source is selected as LXT/LIRC and LXT/LIRC is on.
6. If RTC clock source LXT is on.

	Normal Mode	Idle Mode	Power-down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt
LXT (32 kHz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
EBI	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	ON/OFF[4]
WDT	ON	ON	ON/OFF[5]
WWDT	ON	ON	Halt
RTC	ON	ON	ON/OFF[6]
UART	ON	ON	Halt
SC	ON	ON	Halt
PS/2	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
I^2S	ON	ON	Halt
USB	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, RTC, UART, BOD, GPIO and USB

6.3.2 Clock Generator

The clock generator consists of 5 clock sources as listed below:

- One external 32.768 kHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 kHz low speed oscillator

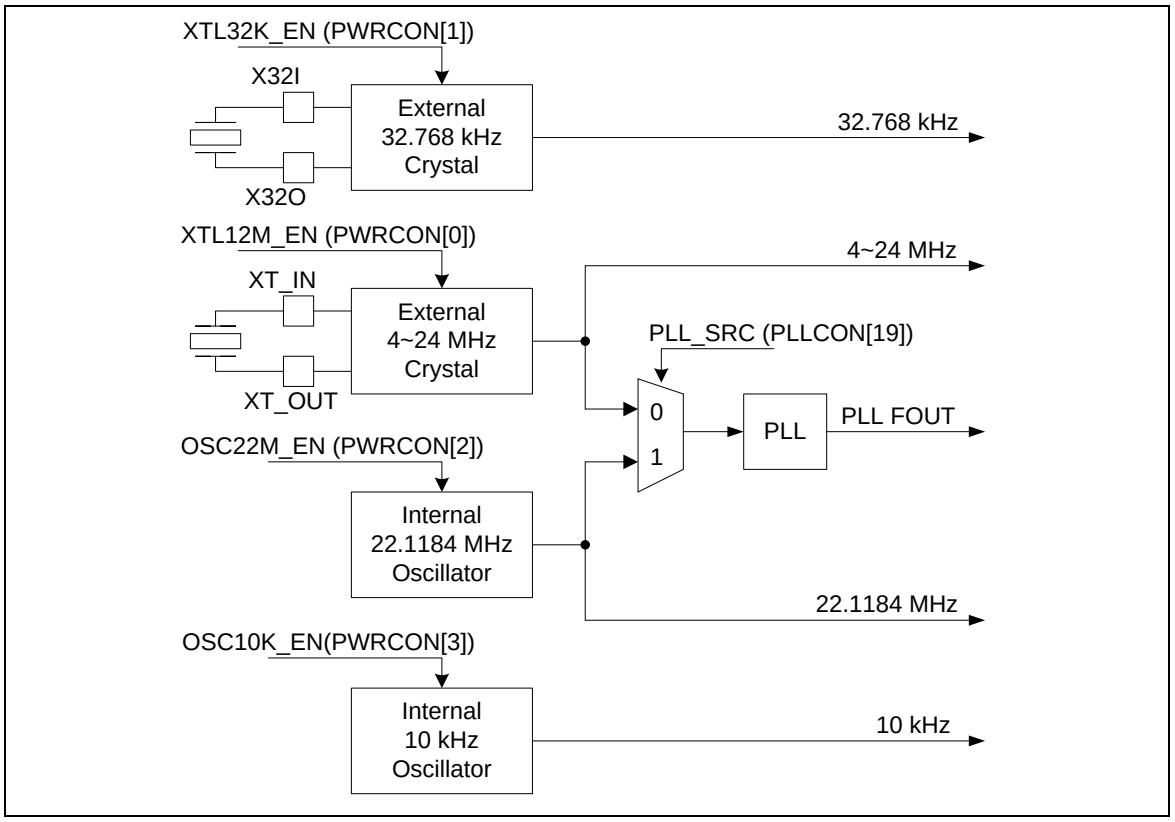

Figure 6-11 Clock Generator Block Diagram

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NuMicro® NUC100 series has up to 84 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 84 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B/C/D/E port has the maximum of 16 pins and GPIOF port has the maximum of 4 pins. Each of the 84 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

6.8 Timer Controller (TMR)

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon time-out, or provide the current value during operation.

6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports external pin capture function for interval measurement
- Supports external pin capture function for reset timer counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated (TIF set to 1)

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NuMicro® NUC100 series has 2 sets of PWM groups supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

6.16 PS/2 Device Controller (PS2D)

6.16.1 Overview

The PS/2 device controller provides a basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the receive/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a “Request to Send” state, but host has ultimate control over communication. Data of DATA line sent from the host to the device is read on the rising edge and sent from the device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. Software can select 1 to 16 bytes for a continuous transmission.

6.16.2 Features

- Host communication inhibit and Request to Send state detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- Software override bus

6.22 Analog Comparator (ACMP)

6.22.1 Overview

The NuMicro® NUC100 series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to cause an interrupt when the comparator output value changes.

6.22.2 Features

- Analog input voltage range: 0~ V_{DDA}
- Supports Hysteresis function
- Supports optional internal reference voltage input at negative end for each comparator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.2		1.8	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.2V_{DD}$ -0.2	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	V_{DD} +0.5	V	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-24	-28	-32	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out Voltage with BOD_VL [1:0] = 00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out Voltage with BOD_VL [1:0] = 01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOD_VL [1:0] = 10b	$V_{BO3.7}$	3.5	3.7	3.9	V	
Brown-out Voltage with BOD_VL [1:0] = 11b	$V_{BO4.4}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V
Band-gap voltage	V_{BG}	1.175	1.20	1.225	V	V_{DD} = 2.5V - 5.5V

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD, PE and PF can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} = 5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

8.4.8 USB PHY Specification

8.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

8.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

8.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	VBUS Current (Steady State)	Standby		50		μA

8.4.8.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	uF