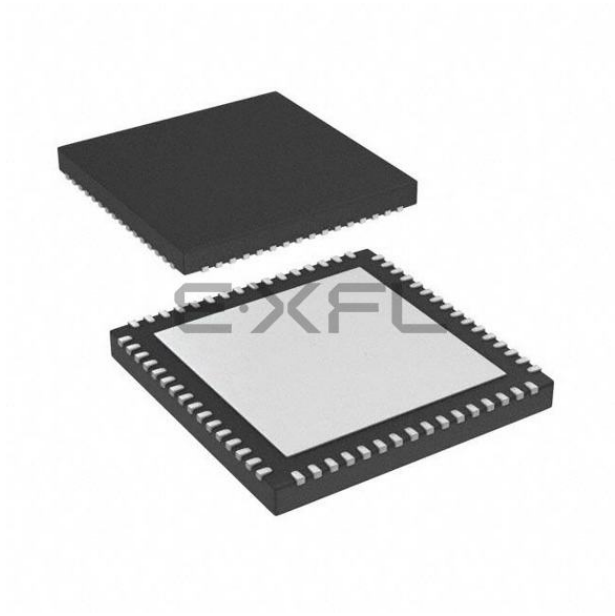

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpd064-i-mr

TABLE 1-17: MCPWM1 THROUGH MCPWM12 PINOUT I/O DESCRIPTIONS (MOTOR CONTROL DEVICES ONLY)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-Pin TQFP	64-Pin QFN/ TQFP			
PWM1H	4	2	O	CMOS	MCPWM1 High Side Output
PWM1L	5	3	O	CMOS	MCPWM1 Low Side Output (Only if PWMAPIN1 (CFGCON<18>) = 0, default)
PWM2H	98	62	O	CMOS	MCPWM2 High Side Output
PWM2L	99	63	O	CMOS	MCPWM2 Low Side Output (Only if PWMAPIN2 (CFGCON<19>) = 0, default)
PWM3H	93	60	O	CMOS	MCPWM3 High Side Output
PWM3L	94	61	O	CMOS	MCPWM3 Low Side Output (Only if PWMAPIN3 (CFGCON<20>) = 0, default)
PWM4H	100	64	O	CMOS	MCPWM4 High Side Output
PWM4L	3	1	O	CMOS	MCPWM4 Low Side Output (Only if PWMAPIN4 (CFGCON<21>) = 0, default)
PWM5H	7	52	O	CMOS	MCPWM5 High Side Output
PWM5L	6	55	O	CMOS	MCPWM5 Low Side Output (Only if PWMAPIN5 (CFGCON<22>) = 0, default)
PWM6H	9	50	O	CMOS	MCPWM6 High Side Output
PWM6L	8	51	O	CMOS	MCPWM6 Low Side Output (Only if PWMAPIN6 (CFGCON<23>) = 0, default)
PWM7H	5	3	O	CMOS	If PWMAPIN1 (CFGCON<18>) = 1), PWM1L is replaced by PWM7H.
PWM8H	99	63	O	CMOS	If PWMAPIN2 (CFGCON<19>) = 1), PWM2L is replaced by PWM8H.
PWM9H	94	61	O	CMOS	If PWMAPIN3 (CFGCON<20>) = 1), PWM3L is replaced by PWM9H.
PWM10H	3	1	O	CMOS	If PWMAPIN4 (CFGCON<21>) = 1), PWM4L is replaced by PWM10H.
PWM11H	87	55	O	CMOS	MCPWM11 High Side Output
	6	58	O	CMOS	If PWMAPIN5 (CFGCON<22>) = 1), PWM5L is replaced by PWM11H.
PWM11L	88	59	O	CMOS	MCPWM11 Low Side Output
PWM12H	82	51	O	CMOS	MCPWM12 High Side Output
	8	55	O	CMOS	If PWMAPIN6 (CFGCON<23>) = 1), PWM6L is replaced by PWM12H.
PWM12L	83	54	O	CMOS	MCPWM12 Low Side Output

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-Transistor Logic input buffer; PPS = Peripheral Pin Select

2.4 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS50001765
- *"MPLAB® ICD 3 Design Advisory"* DS50001764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) DS50001749

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.6 Trace

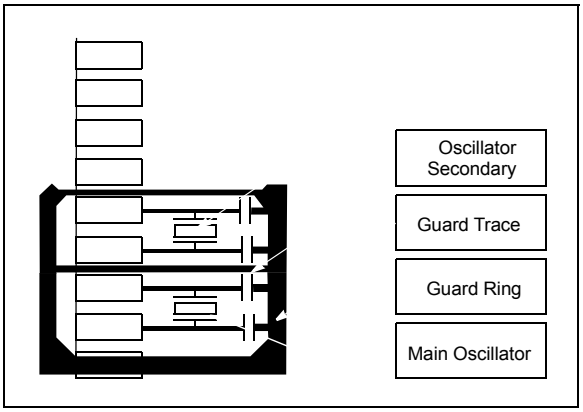
When present on select pin counts, the trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



REGISTER 8-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0 (default)

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0 (default)

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0 (default)

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0 (default)

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

TABLE 9-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION

Peripheral	Clock Source																	
	FRC	LPRC	SOSC	POSC	SYSCLK	SPLL	UPLL	PBCLK1(1)	PBCLK2	PBCLK3	PBCLK4	PBCLK5	PBCLK6	PBCLK7	REFCLKO1	REFCLKO2	REFCLKO3	REFCLKO4
ADC1-ADC7												X					X	
CAN1-CAN4												X						
CFG PMD								X										
CLKO								X										
Comparator 1-5									X									
CPU	X	X	X	X		X	X							X				
CRU								X										
CTMU									X									
CDAC1									X									
CDAC2-CDAC3										X								
DATAEE	X								X									
DMA					X													
DMT								X										
DSCTRL(5)		X											X					
EVIC					X													
Flash	X							X						X				
Input Capture 10-16										X								
Input Capture 1-9									X									
ICD								X										
Output Compare 10-16										X								
Output Compare 1-9									X									
Op amp 1-3, 5									X									
PMP									X									
PORTA-PORTG											X							
PPS								X							X	X	X	X
RTCC		X	X										X					
SPI1-SPI2									X						X			
SPI3-SPI6										X					X			
SSX Control					X													
Timer1		X	X						X									
Timer2-Timer9									X									
UART1-UART2	X				X				X						X			
UART3-UART6	X				X					X					X			
USB1-USB2	X			X			X					X						
WDT		X						X										

Note 1: PBCLK1 is used by system modules and cannot be turned off.

2: SYSCLK/PBCLK5 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.

3: Special Function Register (SFR) access only.

4: Timer1 only.

5: DSCTRL is the Deep Sleep Control Block.

10.0 PREFETCH MODULE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache Module"** (DS60001119), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Prefetch module is a performance enhancing module that is included in the PIC32MK GP/MC family of devices. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly. Although the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

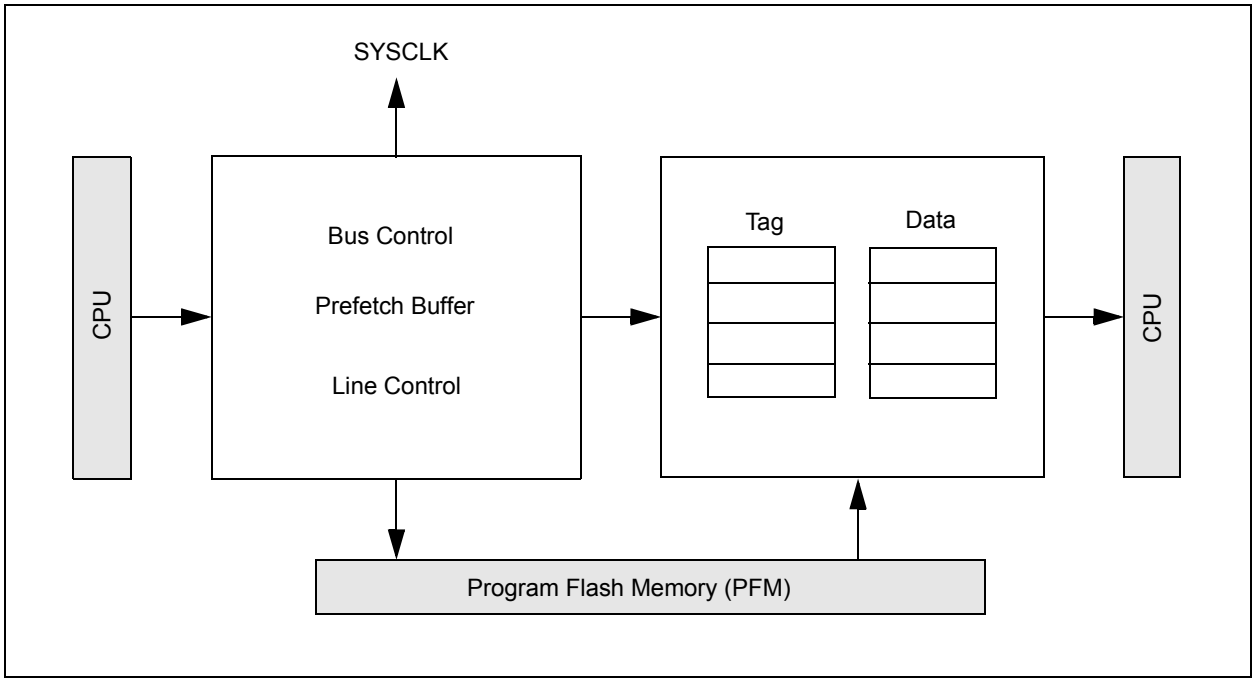
The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without Flash Wait states.

10.1 Prefetch Cache Features

- 36x16 byte fully-associative lines
- 16 lines for CPU instructions
- Four lines for CPU data
- Four lines for peripheral data
- 16-byte parallel memory fetch
- Configurable predictive prefetch

A simplified block diagram of the Prefetch module is shown in Figure 10-1.

FIGURE 10-1: PREFETCH MODULE BLOCK DIAGRAM



REGISTER 12-12: UxADDR: USB ADDRESS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low Speed Enable Indicator bit
1 = Next token command to be executed at Low Speed
0 = Next token command to be executed at Full Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 12-13: UxFRML: USB FRAME NUMBER LOW REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 16-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-y	R-y	R-y
	PSINTV<7:0>							

Legend:		y= Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

TABLE 19-3: OUTPUT COMPARE 10 THROUGH OUTPUT COMPARE 16 REGISTER MAP (CONTINUED)

Virtual Address BF84_#	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5C00	OC15CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5C10	OC15R	31:16	OC15R<31:0>																xxxx
		15:0																	xxxx
5C20	OC15RS	31:16	OC15RS<31:0>																xxxx
		15:0																	xxxx
5E00	OC16CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5E10	OC16R	31:16	OC16R<31:0>																xxxx
		15:0																	xxxx
5E20	OC16RS	31:16 15:0	OC16RS<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

20.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

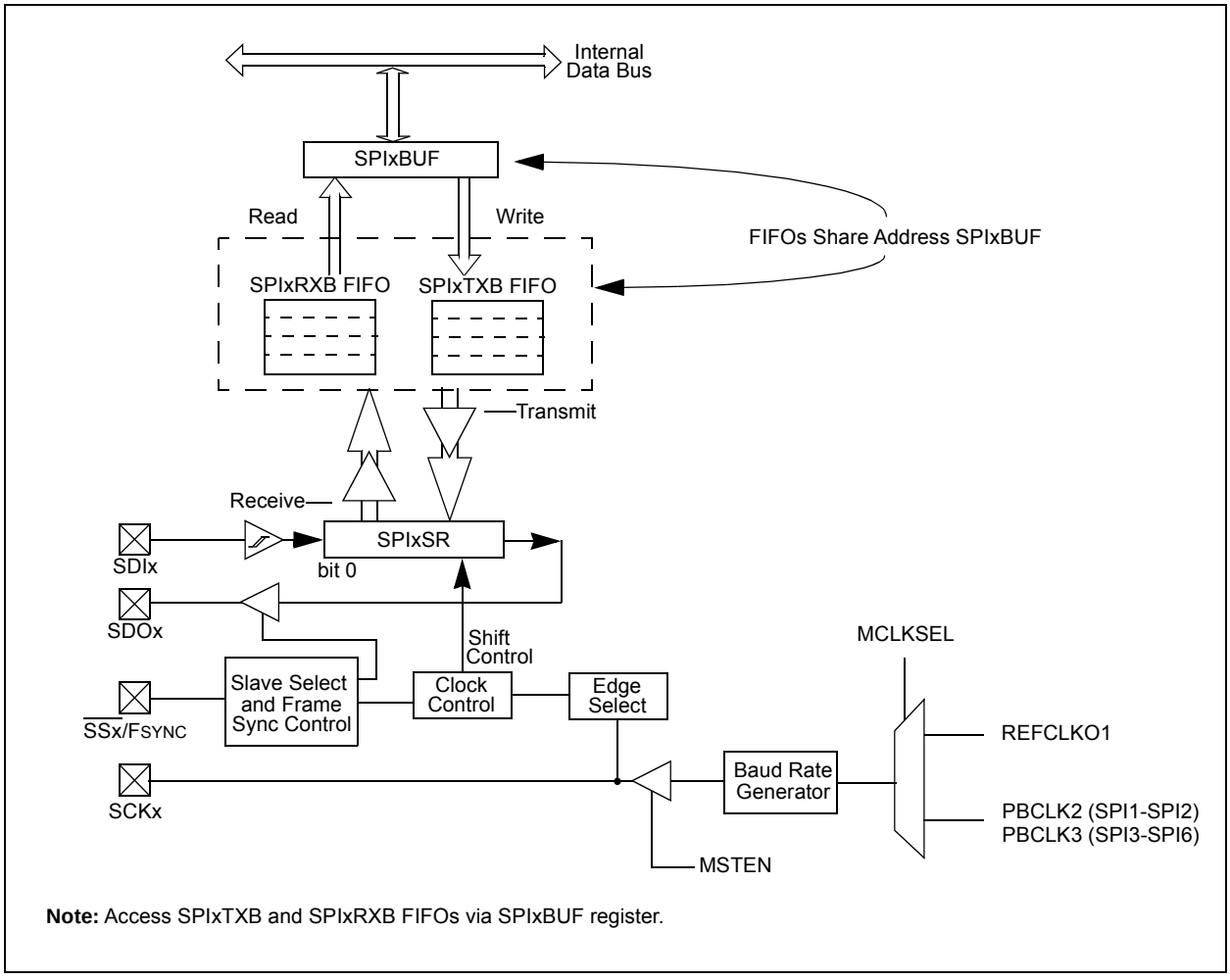
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, analog-to-digital converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 32/24/16/8-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/24/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio codec support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 20-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

21.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Inter-Integrated Circuit"** (DS00000000), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The I^2C software library is available in MPLAB Harmony. If the user application is to implement I^2C, for future device pin compatibility, it is recommended to assign software I^2C functions according to the details provided in the device pin tables (Table 3 through Table 6):

- For 64-pin packages, refer to Notes 6 and 7 in Table 3 and Table 4
- For 100-lead packages, refer to Notes 5 and 6 in Table 5 and Table 6.

21.1 Software I^2C Performance

Table 21-1 provides the performance details of the I^2C.

TABLE 21-1: I^2C PERFORMANCE

I^2C Baud Rate	I^2C Transactions/ Second	I^2C CPU Utilization
400 kHz	22070 (continuous)	50.76%
	16841	38.73%
	4079	9.38%
	429	0.99%
100 kHz	5581 (continuous)	12.84%
	4077	9.38%
	429	0.99%

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7840	ADCDATA36(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7850	ADCDATA37(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7860	ADCDATA38(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7870	ADCDATA39(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7880	ADCDATA40(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7890	ADCDATA41(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78D0	ADCDATA45(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78E0	ADCDATA46(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78F0	ADCDATA47(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7900	ADCDATA48	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7910	ADCDATA49	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7920	ADCDATA50(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7940	ADCDATA52(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7950	ADCDATA53(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7E00	ADCSYSCFG0	31:16	—	—	—	—	AN27	AN26	AN25	AN24	AN23(1)	AN22(1)	AN21(1)	AN20(1)	AN19	AN18	AN17	AN16	0FxF
		15:0	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	FFFF
7E10	ADCSYSCFG1	31:16	—	—	—	—	—	—	—	—	—	—	AN53(1)	AN52(1)	—	AN50(1)	AN49	AN48	00xx
		15:0	AN47(1)	AN46(1)	AN45(1)	—	—	—	AN41(1)	AN40(1)	AN39(1)	AN38(1)	AN37(1)	AN36(1)	AN35(1)	AN34(1)	AN33(1)	—	xxxx
7D00	ADC0CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 3 **STRGLVL:** Scan Trigger High Level/Positive Edge Sensitivity bit

1 = Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), the scan trigger will continue for all selected analog inputs, until the STRIG option is removed.

0 = Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), only a single scan trigger will be generated, which will complete the scan of all selected analog inputs.

bit 2-0 **DMABL<2:0>:** DMA to System RAM Buffer Length Size bits

These bits define the number of locations in system memory allocated per analog input for DMA interface use.

Because each output data is 16-bit wide, one location consists of 2 bytes. Therefore the actual size reserved in the System RAM follows the formula: RAM Buffer Length in bytes = 2(DMABL+1).

The DMABL field can also be thought of as a “Left Shift Amount +1” needed for the channel ID to create the DMA byte address offset to be added to the contents of ADDMAB in order to obtain the byte address of the beginning of the System RAM buffer area allocated for the given channel.

111 = Allocates 128 locations in system memory to each analog input, actually 256 bytes
110 = Allocates 64 locations in system memory to each analog input, actually 128 bytes
101 = Allocates 32 locations in system memory to each analog input, actually 64 bytes
100 = Allocates 16 locations in system memory to each analog input, actually 32 bytes
011 = Allocates 8 locations in system memory to each analog input, actually 16 bytes
010 = Allocates 4 locations in system memory to each analog input, actually 8 bytes
001 = Allocates 2 locations in system memory to each analog input, actually 4 bytes
000 = Allocates 1 location in system memory to each analog input, actually 2 bytes

REGISTER 25-24: ADCTRG7: ADC TRIGGER SOURCE 7 REGISTER

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC26<4:0>:** Trigger Source for Conversion of Analog Input AN26 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC25<4:0>:** Trigger Source for Conversion of Analog Input AN25 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC24<4:0>:** Trigger Source for Conversion of Analog Input AN24 Select bits
See bits 28-24 for bit value definitions.

Note:	This register is not available on 64-pin devices.

REGISTER 27-2: CMxCON: OP AMP/COMPARATOR 'x' CONTROL REGISTER ('x' = 1-5) (CONTINUED)

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12 **Unimplemented:** Read as '0'

bit 11 **OAO:** Op amp Output Enable bit(1)
1 = Op amp output is present on the OAxOUT pin
0 = Op amp output is not present on the OAxOUT pin

bit 10 **AMPMOD:** Op amp Mode Enable bit(1)
1 = Amplifier/Comparator operating in Dual mode (both Op amps and Comparators are enabled)
0 = Amplifier/Comparator operating in Comparator-only mode

bit 9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{TH+}$
0 = $V_{IN+} < V_{TH-}$

When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{TH-}$
0 = $V_{IN+} > V_{TH+}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event Polarity Select bits
11 = Trigger/Event generated on any change of the comparator output
10 = Trigger/Event generated only on high-to-low transition of the polarity-selected comparator output
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output
01 = Trigger/Event generated only on low-to-high transition of the polarity-selected comparator output
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output
00 = Trigger/Event generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Op amp/Comparator Reference Select bit
1 = V_{IN+} input connects to internal CDAC3 output voltage
0 = V_{IN+} input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

Note 1: Before attempting to initialize or enable any of the Op amp bit, the user application must clear the corresponding OPA5MD, OPA3MD, OPA2MD, and OPA1MD bits in the PMD register.

Note: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition is occurred. The IFSx bits are persistent, so they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLSRC<3:0>(2,4)				CLPOL(2,4)	CLMOD(2,4)
23:16	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
	—	FLTSRC<3:0>(2,4)				FLTPOL(2)	FLTMOD<1:0>(4)	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PENH(1)	PENL(1)	POLH(2)	POLL(2)	PMOD<1:0>(2)		OVRENH	OVRENL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	OVRDAT<1:0>(3)		FLTDAT<1:0>(2,3)		CLDAT<1:0>		SWAP	OSYNC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 31-19: TRIGx: PWM PRIMARY TRIGGER COMPARE VALUE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGCMP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGCMP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **TRGCMP<15:0>:** Trigger Compare Value bits

These bits specify the value to match against the local time base register PTMRx to generate a trigger to the ADC module, and an interrupt if the TRGIEN bit (PWMCONx<21>) is set.

Note: To generate a trigger at the PWM period boundary, set the compare value = 0.

34.0 INSTRUCTION SET

The PIC32MK GP/MC family instruction set complies with the MIPS32® Release 5 instruction set architecture. The PIC32MK GP/MC device family *does not* support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	10	—	—	ns	—

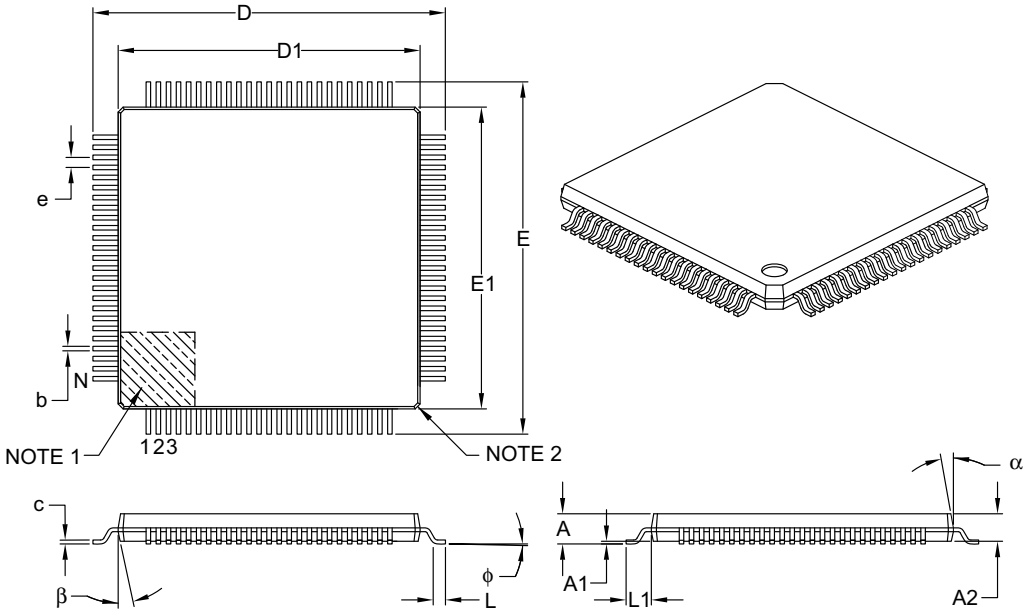
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
31.0 "Motor Control PWM Module"	Updated first page bulleted list to "Nine Fault input pins are available for Faults and current limits." Updated pin table in Figure 31-1; updated **31.1.2 "WRITE-PROTECTED REGISTERS"** Updated label TMRx to PTMRx in Figure 31-2. Updated "All Resets" value from 0000 to 0078 for IOCONx<31:16> registers in Table 31-1. Updated bit 15-0 descriptions in Register 31-6.and Register 31-10 Updated note in Register 31-10. Updated bit 11-10 description in Register 31-11. Updated Notes 1 and 4 in Register 31-12. Added Note 2 and added Note 2 markers in COMP<13:8> and DTCOMP<7:0> in Register 31-18.
	Updated major features list Table 31-1, Register 31-5, Register 31-13, Register 31-15, Register 31-21, replaced SCLKSEL with SCLKDIV. Register 31-1 through Register 31-9, Register 31-18, Table 36-13, replaced SYSCLK with FSYSCLK and LSB = 1/SYSCLK with Min LSB = 1/FSYSCLK. Register 31-11, replaced PWM Resolution with PWM(min) Resolution. Register 31-16, replaced PWMxL with PWMxH,
32.0 "High/Low Voltage Detect (HLVD)"	Removed this entire section.
32.0 "Power-Saving Features"	Removed I^2C and HLVD references (see Table 32-3).
33.0 "Special Features"	Updated bit 7-0 definition and added appropriate table (see Register 33-9). replaced SYSCLK with FSYSCLK and updated table under note.
36.0 "Electrical Characteristics"	Removed original Figure 37-16, Figure 37-17, Figure 37-18, Figure 37-19, Table 37-6, Table 37-38, and Table 37-39. Removed I^2C references (see Table 36-9). Removed I^2C references (see Table 36-14). Updated Read Access Time and Program Time values (see Table 36-19). Updated typical ENOB value (see Table 36-38). Removed references to "AC CHARACTERISTICS" in table titles, and so on. Table 36-13, replaced SYSCLK with FSYSCLK. Table 36-19, added table under Note 1. Table 36-20, updated CM36 typical value from 30 to 140 mV.
	Updated DI20 Min. V_{DD} value in Table 36-9 and OS13 Max. MHz value in Table 36-15. Updated Note 2 equation value from PBCLK2 to PBCLKx in Table 36-16. Updated Table 36-28 to include parameters OA14 through OA17. Updated Table 36-30 title to "Unity Gain Op amp Timing Requirements". Updated Min. ADC Clock Period for parameter AD50 in Table 36-39. Updated Max. Sample Throughput Rates for parameter AD51 in Table 36-39. Updated Table 36-42 to include parameter CTMU0.