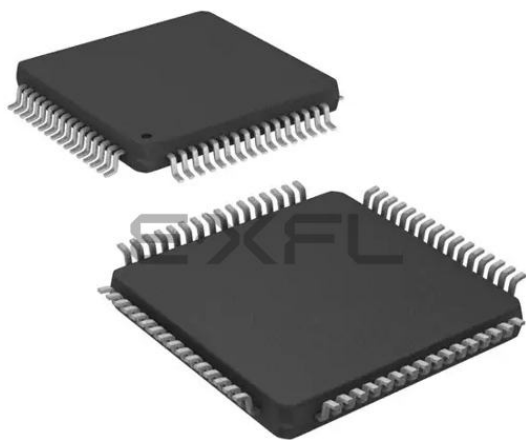




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpd064-i-pt

PIC32MK GP/MC Family

TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW) PIC32MK0512MCF100 PIC32MK1024MCF100 100 1			
Pin #	Full Pin Name	Pin #	Full Pin Name
71	DAC2/AN48/CVD48/RPC10/PMPA14/PSPCS/RC10	86	VDD
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7	87	RPF0/PWM11H/PMPD11/RF0
73	SOSCI/RPC13 ⁽⁴⁾ /RC13 ⁽⁴⁾	88	RPF1/PWM11L/PMPD10/RF1
74	SOSCO/RPB8 ⁽⁴⁾ /RB8 ⁽⁴⁾	89	RPG1/PMPD9/RG1
75	Vss	90	RPG0/PMPD8/RG0
76	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9	91	TRCLK/PMPA18/RF6
77	RPC6/USBID2/PMPA16/RC6	92	TRD3/PMPA19/RF7
78	RPC7/PMPA17/RC7	93	RPB10/PWM3H/PMPD0/RB10
79	PMPD12/RD12	94	RPB11/PWM9H/PWM3L/PMPD1/RB11
80	PMPD13/RD13	95	TRD2/PMPA20/RG14
81	RPC8/PMPWR/PSPWR/RC8	96	TRD1/RPG12/PMPA21/RG12
82	RPD5/PWM12H/PMPRD/PSPRD/RD5	97	TRD0/PMPA22/RG13
83	RPD6/PWM12L/PMPD14/RD6	98	RPB12/PWM2H/PMPD2/RB12
84	RPC9/PMPD15/RC9	99	RPB13/PWM8H/PWM2L/CTPLS/PMPD3/RB13
85	Vss	100	TDO/PWM4H/PMPD4/RA10

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 “Peripheral Pin Select (PPS)”** for restrictions.
 - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAX-CNGx). See **13.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
 - 5: The I²C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I²C master/slave clock. (i.e., SCL).
 - 6: The I²C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I²C data I/O. (i.e., SDA).

PIC32MK GP/MC Family

TABLE 1-10: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/TQFP			
PMA0	44	30	O	TTL/CMOS	Parallel Master Port Address (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA1	43	29	O	TTL/CMOS	
PMA2	14	8	O	TTL/CMOS	
PMA3	12	6	O	TTL/CMOS	
PMA4	11	5	O	TTL/CMOS	
PMA5	10	4	O	TTL/CMOS	
PMA6	29	16	O	TTL/CMOS	
PMA7	28	22	O	TTL/CMOS	
PMA8	50	32	O	TTL/CMOS	
PMA9	49	31	O	TTL/CMOS	
PMA10	42	28	O	TTL/CMOS	
PMA11	41	27	O	TTL/CMOS	
PMA12	35	24	O	TTL/CMOS	
PMA13	34	23	O	TTL/CMOS	
PMA14	71	45	O	TTL/CMOS	
PMA15	70	44	O	TTL/CMOS	
PMA16	77	—	O	TTL/CMOS	
PMA17	78	—	O	TTL/CMOS	
PMA18	91	—	O	TTL/CMOS	
PMA19	92	—	O	TTL/CMOS	
PMA20	95	—	O	TTL/CMOS	
PMA21	96	—	O	TTL/CMOS	
PMA22	97	—	O	TTL/CMOS	
PMA23	1	—	O	TTL/CMOS	
PMCS1	71	45	O	TTL/CMOS	Parallel Master Port Chip Select 1 for PMA(13:0)
PMCS2	70	44	O	TTL/CMOS	Parallel Master Port Chip Select 2 for PMA(14:0)
PMPRD	82	53	O	TTL/CMOS	Parallel Master Port Read Strobe
PMWR	81	52	O	TTL/CMOS	Parallel Master Port Write Strobe
PMCS1A	97	—	O	TTL/CMOS	Parallel Master Port Chip Select 1 for PMA(21:0)
PMCS2A	1	—	O	TTL/CMOS	Parallel Master Port Chip Select 2 for PMA(22:0)

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Reserved	—	29	—	—	—	—	—	—
Real Time Clock	_RTCC_VECTOR	30	OFF030<17:1>	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	Yes
Flash Control Event	_FLASH_CONTROL_VECTOR	31	OFF031<17:1>	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Comparator 1 Interrupt	_COMPARATOR_1_VECTOR	32	OFF032<17:1>	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
Comparator 2 Interrupt	_COMPARATOR_2_VECTOR	33	OFF033<17:1>	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	Yes
USB1 Interrupts	_USB_1_VECTOR	34	OFF034<17:1>	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	Yes
SPI1 Fault	_SPI1_FAULT_VECTOR	35	OFF035<17:1>	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
SPI1 Receive Done	_SPI1_RX_VECTOR	36	OFF036<17:1>	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	No
SPI1 Transfer Done	_SPI1_TX_VECTOR	37	OFF037<17:1>	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
UART1 Fault	_UART1_FAULT_VECTOR	38	OFF038<17:1>	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
UART1 Receive Done	_UART1_RX_VECTOR	39	OFF039<17:1>	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
UART1 Transfer Done	_UART1_TX_VECTOR	40	OFF040<17:1>	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
Reserved	—	41	—	—	—	—	—	—
Reserved	—	42	—	—	—	—	—	—
Reserved	—	43	—	—	—	—	—	—
PORTA Input Change Interrupt	_CHANGE_NOTICE_A_VECTOR	44	OFF044<17:1>	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
PORTB Input Change Interrupt	_CHANGE_NOTICE_B_VECTOR	45	OFF045<17:1>	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
PORTC Input Change Interrupt	_CHANGE_NOTICE_C_VECTOR	46	OFF046<17:1>	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
PORTD Input Change Interrupt	_CHANGE_NOTICE_D_VECTOR	47	OFF047<17:1>	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
PORTE Input Change Interrupt	_CHANGE_NOTICE_E_VECTOR	48	OFF048<17:1>	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
PORTF Input Change Interrupt	_CHANGE_NOTICE_F_VECTOR	49	OFF049<17:1>	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
PORTG Input Change Interrupt	_CHANGE_NOTICE_G_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
Parallel Master Port	_PMP_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes
Parallel Master Port Error	_PMP_ERROR_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MK General Purpose (GP) Family Features”** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
01B0	IPC7	31:16	—	—	—	FCEIP<2:0>			FCEIS<1:0>			—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
01C0	IPC8	31:16	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>			—	—	—	USB1IP<2:0>			USB1IS<1:0>		0000
		15:0	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>			—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
01D0	IPC9	31:16	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>			—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
		15:0	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>			—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
01E0	IPC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000	
01F0	IPC11	31:16	—	—	—	CNDIP<2:0>			CNDIS<1:0>			—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>			—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
0200	IPC12	31:16	—	—	—	PMPIP<2:0>			PMPIS<1:0>			—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
		15:0	—	—	—	CNFIP<2:0>			CNFIS<1:0>			—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
0210	IPC13	31:16	—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>			—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		0000
		15:0	—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>			—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		0000
0220	IPC14	31:16	—	—	—	—	—	—	—	—	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		0000	
		15:0	—	—	—	U2RXIP<2:0>			U2RXIS<1:0>			—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
0230	IPC15	31:16	—	—	—	U3RXIP<2:0>			U3RXIS<1:0>			—	—	—	U3EIP<2:0>			U3EIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
0240	IPC16	31:16	—	—	—	U4TXIP<2:0>			U4TXIS<1:0>			—	—	—	U4RXIP<2:0>			U4RXIS<1:0>		0000
		15:0	—	—	—	U4EIP<2:0>			U4EIS<1:0>			—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		0000
0250	IPC17	31:16	—	—	—	CTMUIP<2:0>			CTMUIS<1:0>			—	—	—	U5TXIP<2:0>			U5TXIS<1:0>		0000
		15:0	—	—	—	U5RXIP<2:0>			U5RXIS<1:0>			—	—	—	U5EIP<2:0>			U5EIS<1:0>		0000
0260	IPC18	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
0270	IPC19	31:16	—	—	—	OC6IP<2:0>			OC6IS<1:0>			—	—	—	IC6IP<2:0>			IC6IS<1:0>		0000
		15:0	—	—	—	IC6EIP<2:0>			IC6EIS<1:0>			—	—	—	T6IP<2:0>			T6IS<1:0>		0000
0280	IPC20	31:16	—	—	—	OC7IP<2:0>			OC7IS<1:0>			—	—	—	IC7IP<2:0>			IC7IS<1:0>		0000
		15:0	—	—	—	IC7EIP<2:0>			IC7EIS<1:0>			—	—	—	T7IP<2:0>			T7IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See 13.2 “CLR, SET, and INV Registers” for more information.
- 2: This bit is not available on 64-pin devices.
- 3: This bit is not available on devices without a CAN module.
- 4: This bit is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.
- 7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

PIC32MK GP/MC Family

TABLE 9-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION

Peripheral	Clock Source																	
	FRC	LPRC	SOSC	POSC	SYSCLK	SPLL	UPLL	PBCLK1 ⁽¹⁾	PBCLK2	PBCLK3	PBCLK4	PBCLK5	PBCLK6	PBCLK7	REFCLK01	REFCLK02	REFCLK03	REFCLK04
ADC1-ADC7												X					X	
CAN1-CAN4												X						
CFG PMD								X										
CLKO								X										
Comparator 1-5									X									
CPU	X	X	X	X		X	X							X				
CRU								X										
CTMU									X									
CDAC1									X									
CDAC2-CDAC3										X								
DATAEE	X								X									
DMA					X													
DMT								X										
DSCTRL ⁽⁵⁾		X											X					
EVIC					X													
Flash	X							X						X				
Input Capture 10-16										X								
Input Capture 1-9									X									
ICD								X										
Output Compare 10-16										X								
Output Compare 1-9									X									
Op amp 1-3, 5									X									
PMP									X									
PORTA-PORTG											X							
PPS								X							X	X	X	X
RTCC		X	X										X					
SPI1-SPI2									X						X			
SPI3-SPI6										X					X			
SSX Control					X													
Timer1		X	X						X									
Timer2-Timer9									X									
UART1-UART2	X				X				X						X			
UART3-UART6	X				X					X					X			
USB1-USB2	X			X			X					X						
WDT		X						X										

- Note** 1: PBCLK1 is used by system modules and cannot be turned off.
2: SYSClk/PBCLK5 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.
3: Special Function Register (SFR) access only.
4: Timer1 only.
5: DSCTRL is the Deep Sleep Control Block.

TABLE 12-1: USB1 AND USB2 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A310	U2EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A320	U2EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A330	U2EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A340	U2EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A350	U2EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A360	U2EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A370	U2EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A380	U2EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A390	U2EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3A0	U2EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3B0	U2EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3C0	U2EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3D0	U2EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3E0	U2EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3F0	U2EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.
- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET, and INV registers.
- 4: Reset value for this bit is undefined.

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REGISTER 12-2: UxOTGIE: USB OTG INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVIE	SESENDIE	—	VBUSVDIE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit

1 = ID interrupt is enabled

0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit

1 = 1 millisecond timer interrupt is enabled

0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit

1 = Line state interrupt is enabled

0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit

1 = ACTIVITY interrupt is enabled

0 = ACTIVITY interrupt is disabled

bit 3 **SESVIE:** Session Valid Interrupt Enable bit

1 = Session valid interrupt is enabled

0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit

1 = B-session end interrupt is enabled

0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit

1 = A-VBUS valid interrupt is enabled

0 = A-VBUS valid interrupt is disabled

TABLE 13-7: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	—	—	—	TRISD8 ⁽²⁾	—	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	—	F1FE
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	—	—	—	RD8 ⁽²⁾	—	RD6	RD5	RD4	RD3	RD2	RD1	—	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	—	—	—	LATD8 ⁽²⁾	—	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	—	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	—	—	—	ODCD8 ⁽²⁾	—	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	—	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	—	—	—	CNPUD8 ⁽²⁾	—	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	—	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	—	—	—	CNPDD8 ⁽²⁾	—	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	—	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	—	—	—	CNIED8 ⁽²⁾	—	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	—	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	—	—	—	CN STATD8 ⁽²⁾	—	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	—	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	—	—	—	CNNED8 ⁽²⁾	—	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	—	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	—	—	—	CNFD8 ⁽²⁾	—	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	—	0000
03C0	SRCON0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR0D8 ⁽²⁾	—	SR0D6	SR0D5	SR0D4	SR0D3	SR0D2	SR0D1	—	0000
03D0	SRCON1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR1D8 ⁽²⁾	—	SR1D6	SR1D5	SR1D4	SR1D3	SR1D2	SR1D1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See 13.2 “CLR, SET, and INV Registers” for more information.

2: This bit is not available on general purpose devices.

TABLE 13-14: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

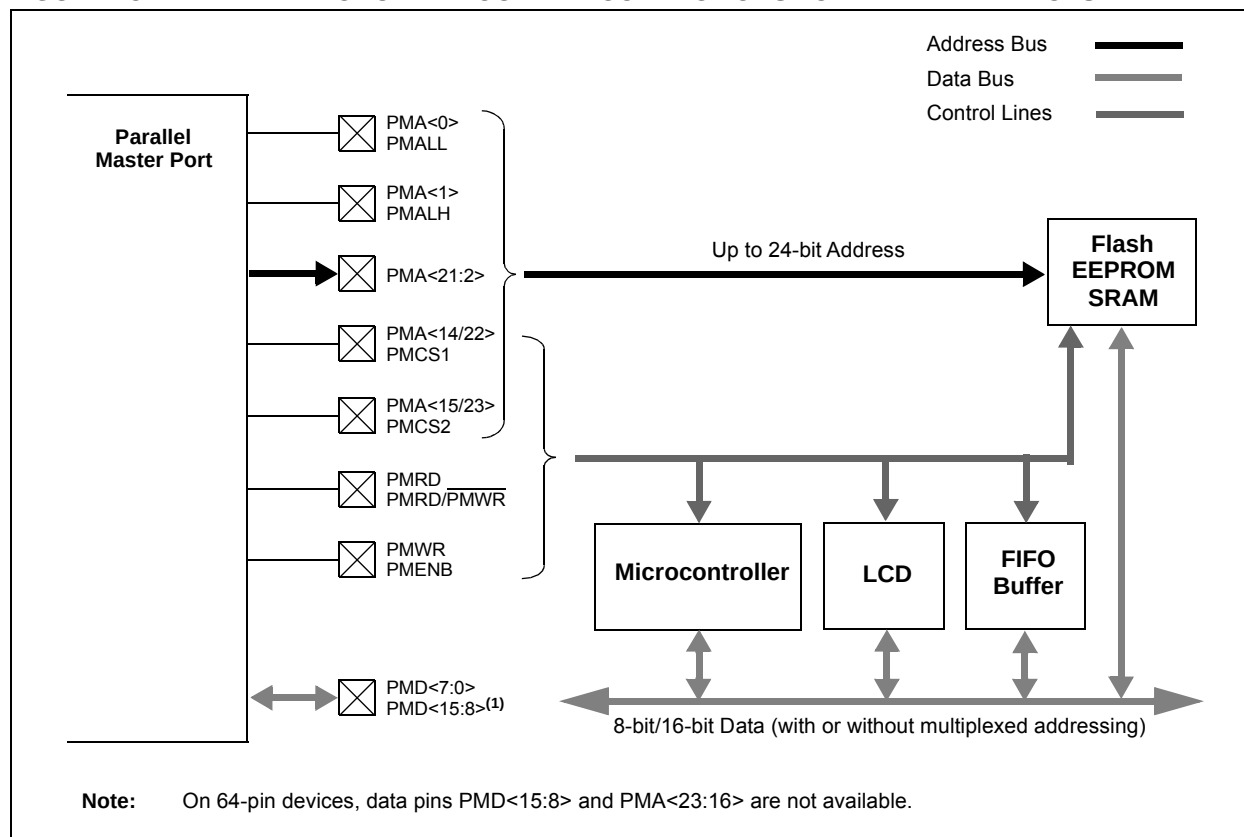
Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See 13.2 “CLR, SET, and INV Registers” for more information.

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NOTES:

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FIGURE 23-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

- bit 7 **GLSWTRG:** Global Level Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion
- bit 6 **GSWTRG:** Global Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion
- Note:** This bit is automatically cleared in the next ADC clock cycle.

- Note 1:** The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.
- 2:** The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.
- 3:** The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.
- 4:** Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 25-19: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

bit 20-16 **TRGSRC6<4:0>**: Trigger Source for Conversion of Analog Input AN6 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented**: Read as '0'

bit 12-8 **TRGSRC5<4:0>**: Trigger Source for Conversion of ADC5 Module Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented**: Read as '0'

bit 4-0 **TRGSRC4<4:0>**: Trigger Source for Conversion of ADC4 Module Select bits
See bits 28-24 for bit value definitions.

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REGISTER 25-40: ADCSYSCFG0: ADC SYSTEM CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	—	—	—	—	AN27	AN26	AN25	AN24
23:16	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN23 ⁽¹⁾	AN22 ⁽¹⁾	AN21 ⁽¹⁾	AN20 ⁽¹⁾	AN19	AN18	AN17	AN16
15:8	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8
7:0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Legend:	HS = Hardware Set	HC = Cleared by Software
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AN27:AN0>:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<31:0>: Reflects the presence or absence of the respective analog input (AN31-AN0).

Note 1: This bit is not available on 64-pin devices.

REGISTER 26-2: CxCFG: CAN BAUD RATE CONFIGURATION REGISTER ('x' = 1-4) (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64) / PBCLK5

111110 = T_Q = (2 x 63) / PBCLK5

•
•
•

000001 = T_Q = (2 x 2) / PBCLK5

000000 = T_Q = (2 x 1) / PBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

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REGISTER 26-7: CxRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVF<15:0>:** FIFOx Receive Overflow Interrupt Pending bit

1 = FIFO has overflowed

0 = FIFO has not overflowed

REGISTER 26-8: CxTMR: CAN TIMER REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits

This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CxCON<20>) is set.

Note 1: CxTMR will be paused when CANCAP = 0.

2: The CxTMR prescaler count will be reset on any write to CxTMR (CANTSPRE will be unaffected).

28.1 Control Registers

TABLE 28-1: CTMU REGISTER MAP

Virtual Address (BF82_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
D000	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>						IRNG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 “CLR, SET, and INV Registers”** for more information.

REGISTER 33-3: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 14-12 **DBGPER<2:0>**: Debug Mode CPU Access Permission bits

1xx = Allow CPU access to Permission Group 2 permission regions
x1x = Allow CPU access to Permission Group 1 permission regions
xx1 = Allow CPU access to Permission Group 0 permission regions
0xx = Deny CPU access to Permission Group 2 permission regions
x0x = Deny CPU access to Permission Group 1 permission regions
xx0 = Deny CPU access to Permission Group 0 permission regions

Note: When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

bit 10 **FSLEEP:** Flash Sleep Mode bit

1 = Flash is powered down when the device is in Sleep mode
0 = Flash power down is controlled by the VREGS bit (PWRCON<0>)

bit 9-7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit

1 = Boot code and Exception code is MIPS32
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit

1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>**: In-Circuit Emulator/Debugger Communication Channel Select bits

11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit⁽¹⁾

1 = JTAG is enabled
0 = JTAG is disabled

Note: On Reset, this Configuration bit is copied into JTAGEN (CFGCON<3>). If JTAGEN (DEVCFG0<2>) = 0, the JTAGEN bit cannot be set to '1' by the user application at run-time, as JTAG is always disabled. However, if JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time as by simply writing JTAGEN (CFGCON<3> as required.

bit 1-0 **DEBUG<1:0>**: Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Disabled
10 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Enabled
01 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Disabled
00 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Enabled

Note: When the FJTAGEN or JTAGEN bits are equal to '0', this prevents 4-wire JTAG debugging, but not PGECx/PGEDx debugging.

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

PIC32MK GP/MC Family

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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ISBN: 978-1-5224-2855-8