

Welcome to **E-XFL.COM** 

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	77
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpd100-e-pt

**TABLE 1-7: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS** 

	Pin N	umber			
Pin Name	100-pin TQFP	64-pin QFN/ TQFP	Pin Type	Buffer Type	Description
			Univ	ersal Asyr	nchronous Receiver Transmitter 1
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	0	_	UART1 Transmit
U1CTS	PPS	PPS	- 1	ST	UART1 Clear to Send
U1RTS	PPS	PPS	0	_	UART1 Ready to Send
			Univ	ersal Asyr	nchronous Receiver Transmitter 2
U2RX	PPS	PPS	- 1	ST	UART2 Receive
U2TX	PPS	PPS	0	_	UART2 Transmit
U2CTS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	0	_	UART2 Ready To Send
			Univ	ersal Asyr	nchronous Receiver Transmitter 3
U3RX	PPS	PPS	- 1	ST	UART3 Receive
U3TX	PPS	PPS	0	_	UART3 Transmit
U3CTS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	0	_	UART3 Ready to Send
			Univ	ersal Asyr	nchronous Receiver Transmitter 4
U4RX	PPS	PPS	- 1	ST	UART4 Receive
U4TX	PPS	PPS	0	_	UART4 Transmit
U4CTS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	0	_	UART4 Ready to Send
			Univ	ersal Asyr	nchronous Receiver Transmitter 5
U5RX	PPS	PPS	- 1	ST	UART5 Receive
U5TX	PPS	PPS	0	_	UART5 Transmit
U5CTS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	0	_	UART5 Ready to Send
	•		Univ	ersal Asyr	nchronous Receiver Transmitter 6
U6RX	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	0	_	UART6 Transmit
U6CTS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	0	_	UART6 Ready to Send
	01400				A 1 A 1 : ( B B

CMOS = CMOS-compatible input or output Legend:

ST = Schmitt Trigger input with CMOS levels

TTL = Transistor-transistor Logic input buffer

Analog = Analog input

O = Output

PPS = Peripheral Pin Select

P = Power I = Input

#### TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

SS				Bits															
Virtual Address (BFC4_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
3FC0	BF1DEVCFG3	31:0																	xxxx
3FC4	BF1DEVCFG2	31:0																	xxxx
3FC8	BF1DEVCFG1	31:0							Note: So	e Table 33-	1 for the h	it description	one						xxxx
3FCC	BF1DEVCFG0	31:0							Note. Se	e lable 55	יו וטו נוופ ט	ii uescripiii	JIIS.						xxxx
3FDC	BF1DEVCP	31:0																	xxxx
3FEC	BF1DEVSIGN	31:0																	xxxx
2EE0	BF1SEQ	31:16		CSEQ<15:0> xxxxx															
3550	DI IOLQ	15:0		TSEQ<15:0> xxxx															

**Legend:** x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

#### TABLE 4-3: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

SS				Bits															
Virtual Address (BFC6_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3FC0	BF2DEVCFG3	31:0																	xxxx
3FC4	BF2DEVCFG2	31:0																	xxxx
3FC8	BF2DEVCFG1	31:0							Note: Se	e Table 33	1 for the h	it description	nne						xxxx
3FCC	BF2DEVCFG0	31:0							11010. 00	ic lable oo	1 101 1110 0	it description	J113.						xxxx
3FDC	BF2DEVCP	31:0																	xxxx
3FEC	BF2DEVSIGN	31:0																	xxxx
3EE0	BF2SEQ	31:16		CSEQ<15:0> xxxx															
3550	BF23EQ	15:0		TSEQ<15:0> xxxx															

**Legend:** x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

0540   0570				MITERIO I REGIOTER MAI (GORTHROED)																
Second   S	ress !)		<u>e</u>								В	its								ts
Second   S	Virtual Add (BF81_#	Registe Name <sup>(1</sup>	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Rese
15.0		OEE003		_		_	_	_	_	_	_	_	_	_	_	_	_	VOFF<	17:16>	0000
0560   0570	0540	OFF003	15:0								VOFF<15:1	>							_	0000
150	0550	OFF004	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	VOFF<	17:16>	0000
0550   05700	0330	011004	15:0								VOFF<15:1	>							_	0000
15:0	0554	OFF005	31:16	_	-	_	_	_	·	_	_	_	_	_	_	_	1	VOFF<	17:16>	0000
0550   0570	0004	011000	15:0								VOFF<15:1	>							_	0000
15.0	0558	OFFOOR	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	-	VOFF<	17:16>	0000
15.0   VOFF<15:1>	0330	011000	15:0								VOFF<15:1	>							_	0000
15.0	0550	OFFOOT	31:16	_	-	_	_	_	_	_	_	_	_	_	_	_	-	VOFF<	17:16>	0000
OFFOID   O	0550	OFF007	15:0								VOFF<15:1	>							_	0000
15.0   VOFF<17:16>   0.000	0560	055000	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	VOFF<	17:16>	0000
OFFO19   15:0	0300	OFF006	15:0								VOFF<15:1	>							_	0000
15:0	0564	OEEOOO	31:16	_	1	_	_	_	_		_	1	_	_	_	_	1	VOFF<	17:16>	0000
OFFO11   15:0   OFFO12   15:0   OFFO13   15:0   OFFO14   15:0   OFFO15	0304	OFF009	15:0				ā.	_			VOFF<15:1	>				a.			_	0000
15:0	0568	OEE010	31:16	_	-	_	_	_	_	_	_	_	_	_	_	_	-	VOFF<	17:16>	0000
OFFO12   15:0   VOFF<15:1>   O000   OFFO12   15:0   VOFF<17:16>   O000   OFFO12   15:0   VOFF<15:1>   O000   OFFO13   15:0   VOFF<17:16>   O000   OFFO13   15:0   VOFF<15:1>   O000   OFFO13   15:0   VOFF<15:1>   O000   OFFO13   15:0   VOFF<15:1>   O000   OFFO13	0300	011010	15:0								VOFF<15:1	>							_	0000
15:0	0560	OEE011	31:16	_	1	_	_	_	_		_	1	_	_	_	_	1	VOFF<	17:16>	0000
VOFF<15:1>         VOFF<15:1>         OFF           0574         0FF013         31:16         -         -         -         -         -         -         0000           0578         0FF014         15:0         VOFF<15:1>         -         -         -         -         0000           057C         0FF015         31:16         - <t< td=""><td>0300</td><td>011011</td><td>15:0</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>VOFF&lt;15:1</td><td>&gt;</td><td></td><td></td><td></td><td></td><td></td><td></td><td>_</td><td>0000</td></t<>	0300	011011	15:0								VOFF<15:1	>							_	0000
15:0	0570	OEE012	31:16	_	-	_	_	_	_	_	_	_	_	_	_	_	-	VOFF<	17:16>	0000
VOFF<15:1>         VOFF<15:1>         OFF014         15:0         VOFF<15:1>         DOFF         VOFF<15:1>         DOFF         OFF015         31:16         —         OFF         OFF015         31:16         —         OFF<17:16>         OOO           0580         0FF016         31:16         —         <	0370	011012	15:0								VOFF<15:1	>							_	0000
15:0	0574	OEE013	31:16	_	-	_	_	_	_	_		_	_	_	_	_	-	VOFF<	17:16>	0000
0578         0FF014         15:0         VOFF<15:1>         — 0000           057C         0FF015         31:16         — — — — — — — — — — VOFF<17:16>         0000           0580         0FF016         31:16         — — — — — — — — — — VOFF<17:16>         0000           0580         0FF016         31:16         — — — — — — — — — VOFF<17:16>         0000	0374	011013	15:0			•	•	•	•		VOFF<15:1	>	•	•	•	•		•	_	0000
15:0	0578	OFF014	31:16	_	_	_	_	_	_	_			_	_	_	_	_	VOFF<	17:16>	0000
057C	0076	OFF014	15:0								VOFF<15:1	>							_	0000
15:0 VOFF<15:1>	057C	OFF015		_	_	_	_	_	_	_	_	_	_	_	_	_	_	VOFF<	17:16>	0000
0580   OFF016	0070	OFF015	15:0								VOFF<15:1	>							_	0000
VOFF<15:1> — 0000	0580	OEE016	31:16		_		_	_	_	_	_	_		_	_	_	_	VOFF<	17:16>	0000
	0360	0-1016	15:0								VOFF<15:1	>							_	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See 13.2 "CLR, SET, and INV Registers" for more information.
  - 2: This bit is not available on 64-pin devices.
  - 3: This bit is not available on devices without a CAN module.
  - 4: This bit is not available on 100-pin devices.
  - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
  - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.
  - 7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

# 9.0 OSCILLATOR CONFIGURATION

Note:

This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MK GP/MC oscillator system has the following modules and features:

- Five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated FRC
- · Dedicated On-Chip PLL for USB modules
- · Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

A block diagram of the oscillator system is provided in Figure 9-1. The clock distribution is shown in Table 9-1.

DS60001402E-page 271

TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

SS										В	its								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1664	RPB9R	31:16 15:0		_	_	_	_	_	_	_		_	_	_	F	— RPB9R<4:0		_	0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1668	RPB10R	15:0	_	_	_	_	_	_	_	_	_	_	_		R	PB10R<4:0	)>		0000
4000	55545	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
166C	RPB11R	15:0	_	_	_	_	_	_	_	_	_	_	_		R	PB11R<4:0	)>		0000
4070	DDD40D	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1670	RPB12R	15:0	_	_	_	_	_	_	_	_	_	_	_		R	PB12R<4:0	)>		0000
1674	RPB13R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1674	RPBISK	15:0	_	_	_	_	_	_	_	_	_	_	_		R	PB13R<4:0	)>		0000
1678	RPB14R	31:16	1	_	_	_	_	_	_	_	1	_	_	_	_	_	-	_	0000
1076	KFD14K	15:0	1	_	_	_	_	_	_	_	1	_	_		R	:PB14R<4:(	)>		0000
167C	RPB15R	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	-	_	0000
1070	KFBIJK	15:0	_	_	_	_	_	_	_	_	_	_	_		R	PB15R<4:0	)>		0000
1680	RPC0R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1000	IN COIN	15:0	_	_	_	_	_	_	_	_	_	_	_		F	RPC0R<4:0	>		0000
1684	RPC1R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1004	THE OTHER	15:0	_	_	_	_	_	_	_	_	_	_	_		F	RPC1R<4:0	>		0000
1688	RPC2R	31:16		_	_					_		_	_	_	_	_	_	_	0000
.000	02.1	15:0		_						_		_	_			RPC2R<4:0			0000
1690	RPC4R	31:16		_	_					_		_	_	_	_	_		_	0000
	•	15:0	_	_	_	_	_	_	_	_	_	_	_		F	RPC4R<4:0	>		0000
1698	RPC6R	31:16		_	_					_		_	_	_		<u> </u>	_	_	0000
		15:0	_	_	_	_	_		_	_	_	_	_			RPC6R<4:0			0000
169C	RPC7R	31:16		_				_		_		_		_			_	_	0000
		15:0		_	_	_	_	_	_	_	_	_	_			RPC7R<4:0			0000
16A0	RPC8R	31:16		_								_		_	<u> </u>	PC8R<4:0		_	0000
		15:0				_	_	<del></del>	_			_	_			RPC6R<4.0			0000
16A4	RPC9R	31:16 15:0		_	_	_	_	_	_	_		_	_	_		RPC9R<4:0		_	0000
			_											_	T	RFC9R\4.0	_	_	0000
16A8	RPC10R	31:16 15:0			-		<del></del>	<del></del>	_			_		_		PC10R<4:0		_	0000
-		31:16			<del>-</del>			<del>  -</del>	<del>  -</del>			_		_	I _	F 0 10K \4.0	_	_	0000
16B0	RPC12R	15:0			$+ \equiv$									_		PC12R<4:(		_	0000
-		31:16												_			_		0000
16BC	RPC15R	15:0						<del>-</del>	<del></del>			_		_		PC15R<4:(		_	0000
<del></del>		31:16												_			_	_	0000
16CC	RPD3R	15:0														RPD3R<4:0			0000
Legen	<u> </u>			set: — = 11									_	<u> </u>		\\ D\\\\\ <del>\</del>	-		0000

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

REGISTER 13-1: [pin name]R: PERIPHERAL PIN SELECT INPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	-	-	-	-	-	_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	-	_	-		_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0					[pin name	₂]R<3:0>		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

bit 3-0 [pin name]R<3:0>: Peripheral Pin Select Input bits

Where [pin name] refers to the pins that are used to configure peripheral input mapping. See Table 13-1 for input pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

#### REGISTER 13-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_		_	_
22:46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_			RPnR<4:0>		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-5 Unimplemented: Read as '0'

bit 4-0 RPnR<4:0>: Peripheral Pin Select Output bits

See Table 13-2 for output pin selection values.

**Note:** Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

NOTES:

#### REGISTER 25-10: ADCGIRQEN2: ADC GLOBAL INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0							
31.24	-	_	_	-	_	-	_	
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	-	_	AGIEN53	AGIEN52	AGIEN51	AGIEN50	AGIEN49	AGIEN48
15.0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	AGIEN47 <sup>(1)</sup>	AGIEN46 <sup>(1)</sup>	AGIEN45 <sup>(1)</sup>	_	_	_	AGIEN41 <sup>(1)</sup>	AGIEN40 <sup>(1)</sup>
7:0	R/W-0	U-0						
7:0	AGIEN39 <sup>(1)</sup>	AGIEN38 <sup>(1)</sup>	AGIEN37 <sup>(1)</sup>	AGIEN36 <sup>(1)</sup>	AGIEN35 <sup>(1)</sup>	AGIEN34 <sup>(1)</sup>	AGIEN33 <sup>(1)</sup>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-22 Unimplemented: Read as '0'

bit 21-13 AGIEN53: AGIEN45 ADC Global Interrupt Enable bits

- 1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDYx bit of the ADCDSTAT2 register)
- 0 = Interrupts are disabled
- bit 12-10 Unimplemented: Read as '0'
- bit 9-1 AGIEN41:AGIEN33 ADC Global Interrupt Enable bits
  - 1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT2 register)
  - 0 = Interrupts are disabled
- bit 0 Unimplemented: Read as '0'

Note 1: This bit is not available on 64-pin devices.

#### REGISTER 25-25: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC					
31.24				CVDDAT	A<15:8>			
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC					
23.10				CVDDA	ΓA<7:0>			
15:8	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
15.6	_	_			AINID	<5:0>		
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 CVDDATA<15:0>: CVD Data Status bits

In CVD mode, these bits obtain the CVD differential output data (subtraction of CVD positive and negative measurement), whenever a Digital Comparator interrupt is generated. The value in these bits is compliant with the FRACT bit (ADCCON1<23>) and is always signed.

bit 15-14 Unimplemented: Read as '0'

#### REGISTER 25-37: ADCEISTAT2: ADC EARLY INTERRUPT STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0							
31.24	_	_	-	_	-	-	-	-
23:16	U-0	U-0	R-0, HS, HC					
23.10	_	_	EIRDY53	EIRDY52	EIRDY51	EIRDY50	EIRDY49	EIRDY48
15.0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
15:8	EIRDY47 <sup>(1)</sup>	EIRDY46 <sup>(1)</sup>	EIRDY45 <sup>(1)</sup>	_	_	_	EIRDY41 <sup>(1)</sup>	EIRDY40 <sup>(1)</sup>
7:0	R-0, HS, HC	U-0						
7.0	EIRDY39 <sup>(1)</sup>	EIRDY38 <sup>(1)</sup>	EIRDY37 <sup>(1)</sup>	EIRDY36 <sup>(1)</sup>	EIRDY35 <sup>(1)</sup>	EIRDY34 <sup>(1)</sup>	EIRDY33 <sup>(1)</sup>	

Legend:	HS = Hardware Set	HC = Cleared by hardwa	re
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-22 Unimplemented: Read as '0'

#### bit 21-13 EIRDY53:EIRDY45: Early Interrupt for Corresponding Analog Input Ready bits

- 1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCXTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.
- 0 = Interrupts are disabled

#### bit 12-10 Unimplemented: Read as '0'

- bit 9-1 EIRDY41:EIRDY33: Early Interrupt for Corresponding Analog Input Ready bits
  - 1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCXTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.
  - 0 = Interrupts are disabled
    Unimplemented: Read as '0'

bit 0

Note 1: This bit is not available on 64-pin devices.

#### TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)

ess										Bits									
Virtual Address (BF82_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
B420	QEI2STAT	31:16	_	_	_	_		_	_		_				_		-		0000
D420	QLIZSTAT	15:0	_	_	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ			PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
B430	POS2CNT	31:16								DSCNT<31:1									0000
		15:0		POSCNT<15:0> 0000									<del>                                     </del>						
B440	POS2HLD	31:16								OSHLD<31:1									0000
		15:0								OSHLD<15: ELCNT<31:1									0000
B450	VEL2CNT	31:16 15:0								'ELCNT<31:1									0000
		31:16								ELHLD<31:1									0000
B460	VEL2HLD	15:0								/ELHLD<31.1									0000
		31:16								ITTMR<31:1									-
B470	INT2TMR	15:0		INTTMR<31:16> 0000 INTTMR<15:0> 0000															
		31:16		INTHLD<31:16> 0000															
B480	INT2HLD	15:0										0000							
		31:16		INDXCNT<31:16> 00									0000						
B490	INDX2CNT	15:0											0000						
D 4 4 0	INDVOLUD	31:16							IN	DXHLD<31:	16>								0000
B4A0	INDX2HLD	15:0							IN	IDXHLD<15:	0>								0000
B4B0	QEI2ICC	31:16							C	EIICC<31:1	6>								0000
D4DU	QEIZICC	15:0							(	QEIICC<15:0	)>								0000
B4C0	QEI2CMPL	31:16							QE	EICMPL<31:	16>								0000
D-100	QLIZOWII L	15:0							Q	EICMPL<15	:0>								0000
B600	QEI3CON	31:16	_	_	_	_	_	_	_	_	_	-	_	_	_	_	_	_	0000
	QLIOCOIT	15:0	QEIEN		QEISIDL	ı	PIMOD<2:0>		IMV<	1:0>			INTDIV<2:0		CNTPOL	GATEN	CCM		0000
B610	QEI3IOC	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_		HCAPEN	+ -
			QCAPEN	FLTREN		QFDIV<2:0>		OUTFN	VC<1:0>	SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
B620	QEI3STAT	31:16		_		_			_						_		_		0000
		15:0	_	_	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN DSCNT<31:1		PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
B630	POS3CNT	31:16																	0000
		15:0 31:16								OSCNT<15: OSHLD<31:1									0000
B640	POS3HLD	15:0								OSHLD<31:1									0000
l egen	<b></b>		ا مه میامید	Ponet: -	- unimpleme	tad raad aa	'o' Desetua	luca ara ah	own in hexade		U-								0000

PIC32MK GP/MC Family

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 13.2 "CLR, SET, and INV Registers" for

#### REGISTER 30-10: QEIXICC: QEIX INITIALIZE/CAPTURE/COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	ICCH<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16	ICCH<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	ICCH<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				ICCH	<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 ICCH<31:0>: 32-bit Initialize/Capture/Compare High bits

#### REGISTER 30-11: QEIXCMPL: CAPTURE LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	CMPL<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16	CMPL<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CMPL<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				CMPL	_<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 CMPL<31:0>: 32-bit Compare Low Value bits

#### REGISTER 31-2: PTPER: PRIMARY MASTER TIME BASE PERIOD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24	_	_	_	_	_	_	_	_		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	_	_	_	_	_	_	_	_		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15.6	PTPER<15:8> <sup>(1,2)</sup>									
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>		
7.0				PTPER•	<7:0> <sup>(1,2)</sup>					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 PTPER<15:0>: Primary Master Time Base Period Value bits<sup>(1,2,4)</sup>

Note 1: Minimum LSb = 1 / FSYSCLK.

2: Minimum value is 0x0008.

**3:** If a period value is lesser than 0x0008 is chosen, the internal hardware forcefully sets the period to a minimum value of 0x0008.

**4:** PTPER = (FSYSCLK / (FPWM \* PCLKDIV<2:0> bits (PTCON<6:4>)). FPWM = User-desired PWM Frequency.

## REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

- bit 25 **CLPOL:** Current-Limit Polarity bits for PWM Generator 'x'(2,4)
  - 1 = The selected current-limit source is active-low
  - 0 = The selected current-limit source is active-high
- bit 24 **CLMOD:** Current-Limit Mode Enable bit for PWM Generator 'x'(2,4)
  - 1 = Current-limit function is enabled
  - 0 = Current-limit function is disabled, current-limit overrides disabled (current-limit interrupts can still be generated). If Faults are enabled, FLTMOD will override the CLMOD bit.

Changes take effect on the next PWM cycle boundary following PWM being enabled, and subsequently on each PWM cycle boundary. When updating CLMOD from '1' to '0', if the current-limit input is still active, the current-limit override condition will not be removed.

- bit 23 Unimplemented: Read as '0'
- Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).
  - 2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).
  - 3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs
  - 4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

#### Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

#### **Undesirable Example: PWM1:** (DTCMP1 = Current Limit = Fault = FLT3 pin)

#### REGISTER 32-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER<sup>(3)</sup>

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	-	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	-	_	_	_	_	_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
15:8	_	_	_	_	_	_	_	DSINT0
7.0	R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0
7:0	DSFLT			DSWDT	DSRTC	DSMCLR		_

**Legend:** HS = Hardware Set

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-9 Unimplemented: Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit

1 = Interrupt-on-change was asserted during Deep Sleep

0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 DSFLT: Deep Sleep Fault Detected bit

1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted

0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 DSWDT: Deep Sleep Watchdog Timer Time-out bit

1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep

0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 DSRTC: Real-Time Clock and Calendar Alarm bit

1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep

0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 DSMCLR: MCLR Event bit

1 = The  $\overline{\text{MCLR}}$  pin was active and was asserted during Deep Sleep

 $0 = \text{The } \overline{\text{MCLR}}$  pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 Unimplemented: Read as '0'

Note 1: All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

2: To ensure a successful write, this register must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

**3:** After waking from deep sleep, writes to the DSWAKE register are ignored until the RELEASE bit (DSCON<0>) is cleared.

TABLE 32-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)

Peripheral	PMDx Bit Name <sup>(3)</sup>	Register Name and Bit Location
Output Compare 9	OC9MD	PMD3<24>
Output Compare 10	OC10MD	PMD3<25>
Output Compare 11	OC11MD	PMD3<26>
Output Compare 12	OC12MD	PMD3<27>
Output Compare 13	OC13MD	PMD3<28>
Output Compare 14	OC14MD	PMD3<29>
Output Compare 15	OC15MD	PMD3<30>
Output Compare 16	OC16MD	PMD3<31>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
PWM1	PWM1MD	PMD4<16>
PWM2	PWM2MD	PMD4<17>
PWM3	PWM3MD	PMD4<18>
PWM4	PWM4MD	PMD4<19>
PWM5	PWM5MD	PMD4<20>
PWM6	PWM6MD	PMD4<21>
PWM7	PWM7MD	PMD4<22>
PWM8	PWM8MD	PMD4<23>
PWM9	PWM9MD	PMD4<24>
PWM10	PWM10MD	PMD4<25>
PWM11	PWM11MD	PMD4<26>
PWM12	PWM12MD	PMD4<27>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

<sup>2:</sup> This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

**<sup>3:</sup>** For any associated PMDx bit, 0 = clocks enabled to the peripheral; 1 = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

#### REGISTER 33-6: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/P	R/P	R/P	R/P	R/P	r-1	r-1	r-1
31:24	FVBUSIO1	FUSBIDIO1	IOL1WAY	PMDL1WAY	PGL1WAY	_	_	_
00.40	R/P	R/P	r-1	R/P	r-1	r-1	r-1	r-1
23:16	FVBUSIO2	FUSBIDIO2	_	PWMLOCK	_	_	_	_
15:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
15:8				USERID<	<15:8>			
7.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
7:0				USERID	<7:0>		•	

Legend:r = Reserved bitP = Programmable bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31 FVBUSIO1: USB1 VBUSON Selection bit

1 = VBUSON pin is controlled by the USB1 module 0 = VBUSON pin is controlled by the port function

bit 30 FUSBIDIO1: USB1 USBID Selection bit

1 = USBID pin is controlled by the USB module 0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit

1 = Allow only one reconfiguration0 = Allow multiple reconfigurations

bit 28 PMDL1WAY: Peripheral Module Disable Configuration bit

1 = Allow only one reconfiguration0 = Allow multiple reconfigurations

bit 27 PGL1WAY: Permission Group Lock One Way Configuration bit

1 = Allow only one reconfiguration0 = Allow multiple reconfigurations

bit 26-24 Reserved: Write as '1'

bit 23 FVBUSIO2: USB2 VBUSON Selection bit

1 = VBUSON pin is controlled by the USB2 module0 = VBUSON pin is controlled by the port function

bit 22 FUSBIDIO2: USB2 USBID Selection bit

1 = USBID pin is controlled by the USB2 module 0 = USBID pin is controlled by the port function

bit 21 Reserved: Write as '1'

bit 20 PWMLOCK: PWM Write Access Select bit

1 = Write accesses to the PWM IOCONx register are not locked or protected

0 = Write accesses to the PWM IOCONx register must use the PWMKEY unlock procedure

bit 19-16 Reserved: Write as '1'

bit 15-0 USERID<15:0>: This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

Parallel Slave Port Requirements	667	UART1 and UART2	326
PIC32MK Family USB Interface Diagram		UART3-UART6	327
PICkit 3 In-Circuit Debugger/Programmer		USB1 and USB2	215
Pinout I/O Descriptions		Registers	
MCPWM Fault, Current Limit and Dead-Tin	ne Compen-	[pin name]R (Peripheral Pin Select Input)	273
sation		AD1CON1 (A/D Control 1)	
MCPWM Generators 1 through 12	29	AD1CON1 (ADC Control 1)	
Quadrature Encoders 1 through 6	31	ADCANCON (ADC Analog Warm-up Con	
Pinout I/O Descriptions (table) . 15, 16, 17, 18, 21		436	,
26, 27, 28, 32, 33		ADCBASE (ADC Base)	425
PORTB Register Map (64-pin and 100-pin Device	es)254	ADCCMP1CON (ADC Digital Compara	
Power-on Reset (POR)	,	Register)	
and On-Chip Voltage Regulator	611	ADCCMPENx (ADC Digital Comparator ')	
Power-Saving Features		ister ('x' = 1 through 4))	•
with CPU Running		ADCCMPx (ADC Digital Comparator 'x' Lin	
Prefetch Cache SFR Summary		ister ('x' = 1 through 4))	
Prefetch Module		ADCCMPxCON (ADC Digital Comparat	
Total Maddia		Register ('x' = 2 through 4))	
Q		ADCCNTB (ADC Channel Sample Count I	
Quadrature Encoder Interface (QEI)	505	427	Jaco Madress
addutatore Encoder interiore (QEI)		ADCCON1 (ADC Control Register 1)	276
R		ADCCON1 (ADC Control Register 1)	
Real-Time Clock and Calendar (RTCC)	355	,	
Register Map		ADCCON3 (ADC Control Register 3)	
CTMU4	88 496 502	ADCCSS1 (ADC Common Scan Select R	
Device ADC Calibration Summary		ADCCSS2 (ADC Common Scan Select R	•
Device Configuration Word Summary		ADCDATAx (ADC Output Data Register (	
<u> </u>		41, and 45-53))	
Device EEDATA Calibration Summary		ADCDMAB (ADC Channel Sample count I	3ase Address
Device Serial Number Summary		427	
DMA Channel 0-3		ADCDSTAT1 (ADC Data Ready Status Re	
DMA CRC		ADCDSTAT2 (ADC Data Ready Status Re	•
DMA Global		ADCEIEN1 (ADC Early Interrupt Enable F	,
Flash Controller		ADCEIEN2 (ADC Early Interrupt Enable F	tegister 2) 433
Input Capture 10-16		ADCEISTAT2 (ADC Early Interrupt Status	Register 2)
Input Capture 1-9		435	
Interrupt		ADCFLTRx (ADC Digital Filter 'x' Reg	ister (' $x$ ' = 1
Op amp/Comparator		through 6))	404
Oscillator Configuration		ADCGIRQEN1 (ADC Interrupt Enable Reg	gister 1) 397
Output Compare 10-16		ADCIMCON1 (ADC Input Mode Control R	egister 1) 389
Output Compare1-9		ADCIMCON2 (ADC Input Mode Control R	egister 2) 392
Parallel Master Port		ADCIMCON3 (ADC Input Mode Control R	egister 3) 394
Peripheral Pin Select Input		ADCIMCON4 (ADC Input Mode Control R	
Peripheral Pin Select Output	270	ADCIRQEN2 (ADC Interrupt Enable Regis	ster 2) 398
PORTA (100-pin Devices)	252	ADCSYSCFG0 (ADC System Configuration	on Register 0)
PORTA (64-pin Devices)		439	
PORTB	254	ADCSYSCFG1 (ADC System Configuration	on Register 1)
PORTC (64-pin and 100-pin Devices)	255	440	,
PORTD	257	ADCTRG1 (ADC Trigger Source 1 Regist	er) 406
PORTD (100-pin Devices)	256	ADCTRG2 (ADC Trigger Source 2 Regist	,
PORTE (100-pin Devices)	258	ADCTRG3 (ADC Trigger Source 3 Regist	
PORTE (64-pin Devices)		ADCTRG4 (ADC Trigger Source 4 Regist	
PORTF (100-pin Devices)		ADCTRG5 (ADC Trigger Source 5 Regist	
PORTF (64-pin Devices)		ADCTRG6 (ADC Trigger Source 6 Regist	
PORTG (100-pin Devices)		ADCTRG7 (ADC Trigger Source 7 Regist	
PORTG (64-pin Devices)			
Prefetch		ADCTRGMODE (ADC Triggering Mode	
RTCC		ADC)	
SPI1 andSPI2		ADCTRGSNS (ADC Trigger Level/Edge S	
SPI3 through SPI6		ADCxCFG (ADCx Configuration Register	
		through 5 and 7))	
System Bus Target 0		ADCxTIME (Dedicated ADCx Timing Reg	
System Bus Target 0		through 5))	
System Bus Target 1		ALRMDATE (Alarm Date Value)	
System Bus Target 2		ALRMDATECLR (ALRMDATE Clear)	
System Bus Target 3		ALRMDATESET (ALRMDATE Set)	
System Control		ALRMTIME (Alarm Time Value)	363
Timer1-Timer9	277. 282		

SPIx Slave Mode (CKE = 1) Requirements	656
SPIx Slave Mode Requirements (CKE = 0)	652
U	
UART	325
USB On-The-Go (OTG)	213
V	
Voltage Regulator (On-Chip)	611
W	
Watchdog Timer and Power-up Timer SFR Summary	578
WWW Address	697
WWW. On-Line Support	10

NOTES: