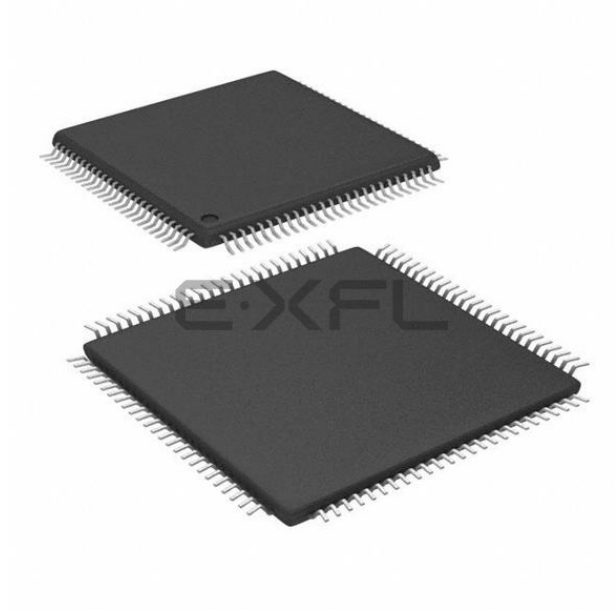

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, WDT |
| Number of I/O | 77 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 3.6V |
| Data Converters | A/D 42x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpd100t-i-pt |

**TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES**

**100-PIN TQFP (TOP VIEW)**

**PIC32MK0512MCF100**
**PIC32MK1024MCF100**

100

1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN23/CVD23/PMPA23/RG15 | 36 | VSS |
| 2 | VDD | 37 | VDD |
| 3 | TCK/RPA7/PWM10H/PWM4L/PMPD5/RA7 | 38 | AN35/CVD35/RG11 |
| 4 | RPB14/PWM1H/VBUSON1/PMPD6/RB14 | 39 | AN36/CVD36/RF13 |
| 5 | RPB15/PWM7H/PWM1L/PMPD7/RB15 | 40 | AN37/CVD37/RF12 |
| 6 | PWM11H/PWM5L/RD1 | 41 | AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMPA11/RE12(6) |
| 7 | PWM5H/RD2 | 42 | AN13/CVD13/C3IN2-/FLT6/PMPA10/RE13(5) |
| 8 | RPD3/PWM12H/PWM6L/RD3 | 43 | AN14/CVD14/RPE14/FLT7/PMPA1/PSPA1/RE14 |
| 9 | RPD4/PWM6H/RD4 | 44 | AN15/CVD15/RPE15/FLT8/PMPA0/PSPA0/RE15 |
| 10 | AN19/CVD19/RPG6/VBUSON2/PMPA5/RG6 | 45 | VSS |
| 11 | AN18/CVD18/RPG7/PMPA4/RG7(5) | 46 | VDD |
| 12 | AN17/CVD17/RPG8/PMPA3/RG8(6) | 47 | AN38/CVD38/RD14 |
| 13 | $\overline{\text{MCLR}}$ | 48 | AN39/CVD39/RD15 |
| 14 | AN16/CVD16/RPG9/PMPA2/RG9 | 49 | TDI/DAC3/AN26/CVD26/RPA8/PMPA9/RA8(6) |
| 15 | VSS | 50 | FLT15/RPB4/PMPA8/RB4(5) |
| 16 | VDD | 51 | OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/T1G/RA4 |
| 17 | AN22/CVD22/RG10 | 52 | AN40/CVD40/RPE0/RE0 |
| 18 | AN21/CVD21/RE8 | 53 | AN41/CVD41/RPE1/RE1 |
| 19 | AN20/CVD20/RE9 | 54 | VBUS |
| 20 | AN10/CVD10/RPA12/USBOEN2/RA12 | 55 | VUSB3V3 |
| 21 | AN9/CVD9/RPA11/USBOEN1/RA11 | 56 | D1- |
| 22 | OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0 | 57 | D1+ |
| 23 | OA2IN+/AN1/C2IN1+/RPA1/RA1 | 58 | VBUS2 |
| 24 | PGED3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0 | 59 | D2- |
| 25 | PGEC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1 | 60 | D2+ |
| 26 | PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2 | 61 | AN45/CVD45/RF5 |
| 27 | PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3 | 62 | VDD |
| 28 | VREF-/AN33/CVD33/PMPA7/RF9 | 63 | OSCI/CLKI/AN49/CVD49/RPC12/RC12 |
| 29 | VREF+/AN34/CVD34/PMPA6/RF10 | 64 | OSCO/CLKO/RPC15/RC15 |
| 30 | AVDD | 65 | VSS |
| 31 | AVss | 66 | AN46/CVD46/RPA14/RA14 |
| 32 | OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0 | 67 | AN47/CVD47/RPA15/RA15 |
| 33 | OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1 | 68 | RD8 |
| 34 | OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMPA13/RC2 | 69 | PGED2/RPB5/USBID1/RB5(6) |
| 35 | AN11/CVD11/C1IN2-/FLT4/PMPA12/RC11 | 70 | PGEC2/RPB6/SCK2/PMPA15/RB6(5) |

**Note**
**1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
**3:** Shaded pins are 5V tolerant.
**4:** Functions are restricted to input functions only and inputs will be slower than standard inputs.
**5:** The $I^2C$ library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the $I^2C$ master/slave clock. (i.e., SCL).
**6:** The $I^2C$ library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the $I^2C$ data I/O, (i.e., SDA).

**REGISTER 4-8: SBTxREGy: SYSTEM BUS TARGET 'x' REGION 'y' REGISTER ('x' = 0-3; 'y' = 0-2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W0 | R/W-0 | R/W0 | R/W-0 | R/W0 | R/W-0 | R/W0 | R/W-0 |
| | BASE<21:14> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BASE<13:6> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | U-0 |
| | BASE<5:0> | | | | | | PRI | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | SIZE<4:0> | | | | | — | — | — |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 31-10 **BASE<21:0>:** Region Base Address bits

bit 9 **PRI:** Region Priority Level bit
1 = Level 2
0 = Level 1

bit 8 **Unimplemented:** Read as '0'

bit 7-3 **SIZE<4:0>:** Region Size bits
Permissions for a region are only active is the SIZE is non-zero.
11111 = Region size = $2^{(SIZE - 1)}$ x 1024 (bytes)
•
•
•
00001 = Region size = $2^{(SIZE - 1)}$ x 1024 (bytes)
00000 = Region is not present

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** Refer to Table 4-6 for the list of available targets and their descriptions.
**2:** For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

**REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NMIKEY<7:0> | | | | | | | |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **NMIKEY<7:0>:** Software Generated NMI Key Register bits
Software NMI event when the correct key (4Eh) is written.
Software NMI event not generated when any other value (not the key) is written.

bit 23-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit
1 = Interrupt controller configured for multi vectored mode
0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
001 = Interrupts of group priority 1 start the Interrupt Proximity timer
000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

**REGISTER 8-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER 'x' ('x' = 0-63) (CONTINUED)**

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 9-8 **IS1<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP0<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 8-3 for the exact bit definitions.

**REGISTER 12-5: UxPWRC: USB POWER CONTROL REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | UACTPND | — | — | USLPGRD | USBBUSY(1) | — | USUSPEND | USBPWR |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB hardware has detected a change in link status; however, an interrupt is pending and has not yet been generated. Software should not put the device into Sleep mode.
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

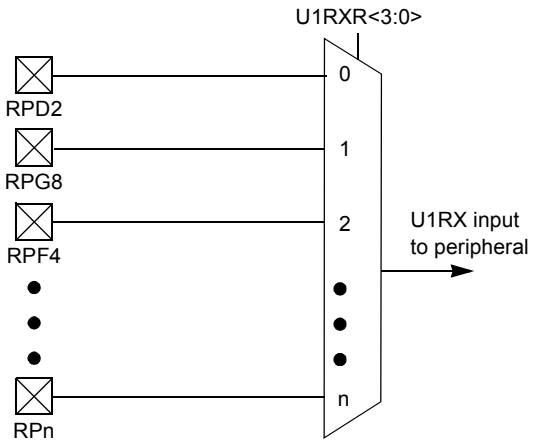
**Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

**FIGURE 13-2: REMAPPABLE INPUT EXAMPLE FOR U1RX**




**Note:** For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

**TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 153C | INDX3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INDX3R<3:0> | | | | 0000 |
| 1540 | HOME3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | HOME3R<3:0> | | | | 0000 |
| 1544 | QEA4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | QEA4R<3:0> | | | | 0000 |
| 1548 | QEB4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | QEB4R<3:0> | | | | 0000 |
| 154C | INDX4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INDX4R<3:0> | | | | 0000 |
| 1550 | HOME4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | HOME4R<3:0> | | | | 0000 |
| 1554 | QEA5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | QEA5R<3:0> | | | | 0000 |
| 1558 | QEB5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | QEB5R<3:0> | | | | 0000 |
| 155C | INDX5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INDX5R<3:0> | | | | 0000 |
| 1560 | HOME5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | HOME5R<3:0> | | | | 0000 |
| 1564 | QEA6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | QEA6R<3:0> | | | | 0000 |
| 1568 | QEB6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | QEB6R<3:0> | | | | 0000 |
| 156C | INDX6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INDX6R<3:0> | | | | 0000 |
| 1570 | HOME6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | HOME6R<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available on 64-pin devices.

**2:** This register is not available on devices without a CAN module.

**3:** This register is only available on PIC32MKXXXGPEXXX devices.

## 18.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following factors:

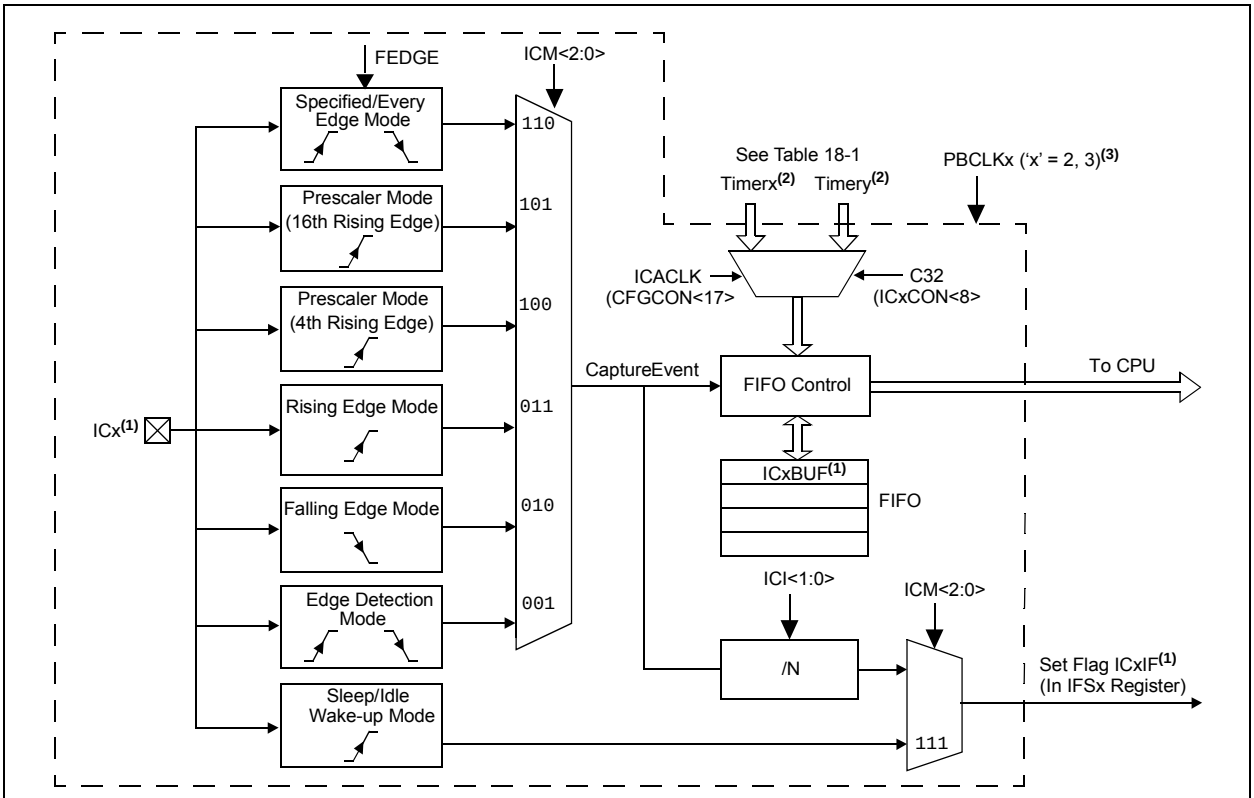
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between either four 16-bit time bases or two 32-bit time base. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

**FIGURE 18-1: INPUT CAPTURE BLOCK DIAGRAM**




**Note 1:** An 'x' in a signal, register or bit name denotes the number of the capture channel.
**2:** See Table 18-1 for Timerx and Timery selections.
**3:** PBCLK2 = Input Capture 1 through Input Capture 9; PBCLK3 = Input Capture 10 through Input Capture 16.

**TABLE 25-2: ADC REGISTER MAP (CONTINUED)**

| Virtual Address | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 76E0 | ADCDATA14 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 76F0 | ADCDATA15 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7700 | ADCDATA16 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7710 | ADCDATA17 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7720 | ADCDATA18 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7730 | ADCDATA19 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7740 | ADCDATA20(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7750 | ADCDATA21(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7760 | ADCDATA22(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7770 | ADCDATA23(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7780 | ADCDATA24 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7790 | ADCDATA25 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 77A0 | ADCDATA26 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 77B0 | ADCDATA27 | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7810 | ADCDATA33(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7820 | ADCDATA34(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7830 | ADCDATA35(1) | 31:16 | DATA<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DATA<15:0> | | | | | | | | | | | | | | | | 0000 |

**Note 1:** This bit or register is not available on 64-pin devices.
**2:** This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
**3:** Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

**REGISTER 25-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | SH5ALT<1:0> | | SH4ALT<1:0> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SH3ALT<1:0> | | SH2ALT<1:0> | | SH1ALT<1:0> | | SH0ALT<1:0> | |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | STRGEN5 | STRGEN4 | STRGEN3 | STRGEN2 | STRGEN1 | STRGEN0 |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | SSAMPEN5 | SSAMPEN4 | SSAMPEN3 | SSAMPEN2 | SSAMPEN1 | SSAMPEN0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27-26 **SH5ALT<1:0>:** ADC5 Analog Input Select bit
- 11 = AN25(1)
- 10 = AN6(1)
- 01 = AN2(1)
- 00 = AN5

bit 25-24 **SH4ALT<1:0>:** ADC4 Analog Input Select bit
- 11 = AN0(1)
- 10 = AN9(1)
- 01 = AN1(1)
- 00 = AN4

bit 23-22 **SH3ALT<1:0>:** ADC3 Analog Input Select bit
- 11 = AN26(1)
- 10 = AN8(1)
- 01 = AN0(1)
- 00 = AN3

bit 21-20 **SH2ALT<1:0>:** ADC2 Analog Input Select bit
- 11 = AN25(1)
- 10 = AN6(1)
- 01 = AN5(1)
- 00 = AN2

bit 19-18 **SH1ALT<1:0>:** ADC1 Analog Input Select bit
- 11 = AN0(1)
- 10 = AN7(1)
- 01 = AN4(1)
- 00 = AN1

bit 17-16 **SH0ALT<1:0>:** ADC0 Analog Input Select bit
- 11 = AN24(1)
- 10 = AN5(1)
- 01 = AN3(1)
- 00 = AN0

bit 15-14 **Unimplemented:** Read as '0'

**Note 1:** Regardless of which alternate input is selected by SHxALT, for ADC0-ADC5 only, all control and results are handled by the native SHxALT = '0b00 input. For example, SH0ALT = '0b11 = AN24. However, from a software and silicon hardware control and results register perspective, the user must initialize the ADC0 module as if AN24 were actually AN0.

**REGISTER 25-11: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | CSS27 | CSS26 | CSS25 | CSS24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSS23(1) | CSS22(1) | CSS21(1) | CSS20(1) | CSS19 | CSS18 | CSS17 | CSS16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSS15 | CSS14 | CSS13 | CSS12 | CSS11 | CSS10 | CSS9 | CSS8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSS7 | CSS6 | CSS5 | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **CSS27:CSS0:** Analog Common Scan Select bits

Analog inputs AN27-AN6 are always Class 3 shared ADC7.

1 = Select AN*x* for input scan (i.e., ANx = CSSx and scan is sequential starting with the lowest to highest enabled CSSx analog input pin)
0 = Skip AN*x* for input scan

**Note 1:** This bit is not available on 64-pin devices.

**Note 1:** In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

**2:** If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRCx<4:0> bits to STRIG mode ('0b11), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

**REGISTER 25-13: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | — | — | — | — | AIRDY27 | AIRDY26 | AIRDY25 | AIRDY24 |
| 23:16 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | AIRDY23(1) | AIRDY22(1) | AIRDY21(1) | AIRDY20(1) | AIRDY19 | AIRDY18 | AIRDY17 | AIRDY16 |
| 15:8 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | AIRDY15 | AIRDY14 | AIRDY13 | AIRDY12 | AIRDY11 | AIRDY10 | AIRDY9 | AIRDY8 |
| 7:0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | AIRDY7 | AIRDY6 | AIRDY5 | AIRDY4 | AIRDY3 | AIRDY2 | AIRDY1 | AIRDY0 |

| **Legend:** | HS = Hardware Set | HC = Hardware Cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AIRDY27:AIRDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

**Note 1:** This bit is not available on 64-pin devices.

**REGISTER 25-14: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | — | — | AIRDY53 | AIRDY52 | AIRDY51 | AIRDY50 | AIRDY49 | AIRDY48 |
| 15:8 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC |
| | AIRDY47(1) | AIRDY46(1) | AIRDY45(1) | — | — | — | AIRDY41(1) | AIRDY40(1) |
| 7:0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | U-0 |
| | AIRDY39(1) | AIRDY38(1) | AIRDY37(1) | AIRDY36(1) | AIRDY35(1) | AIRDY34(1) | AIRDY33(1) | — |

| **Legend:** | HS = Hardware Set | HC = Hardware Cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-22 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY53:AIRDY45:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

bit 12-10 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY41:AIRDY33:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

**Note 1:** This bit is not available on 64-pin devices.

**TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5020 | C4INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 |
| 5030 | C4VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| 5040 | C4TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| 5050 | C4FSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 |
| 5060 | C4RXOVF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| 5070 | C4TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 |
| 5080 | C4RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 5090 | C4RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 50A0 | C4RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 50B0 | C4RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 50C0 | C4FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | | 0000 |
| 50D0 | C4FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | | 0000 |
| 50E0 | C4FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | | 0000 |
| 50F0 | C4FLTCON3 | 31:16 | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | | 0000 |
| 5140 | C4RXFn (n = 0-15) | 31:16 | SID<10:0> | | | | | | | | | | | -— | EXID | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 5340 | C4FIFOBA | 31:16 | C4FIFOBA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5350 | C4FIFOCONn (n = 0-15) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | FSIZE<4:0> | | | | | 0000 |
| | | 15:0 | — | FRESET | UINC | DONLY | — | — | — | — | TXEN | TXABAT | TXLARB | TXERR | TXREQ | RTREN | TXPRI<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

**REGISTER 26-2: CxCFG: CAN BAUD RATE CONFIGURATION REGISTER ('x' = 1-4) (CONTINUED)**

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits(3)
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits
111111 = TQ = (2 x 64) / PBCLK5
111110 = TQ = (2 x 63) / PBCLK5
•
•
•
000001 = TQ = (2 x 2) / PBCLK5
000000 = TQ = (2 x 1) / PBCLK5

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
**2:** 3 Time bit sampling is not allowed for BRP < 2.
**3:** SJW ≤ SEG2PH.
**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

**REGISTER 26-17: CxFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('x' = 1-4); n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXNEMPTYIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | TXNFULLIF(1) | TXHALFIF | TXEMPTYIF(1) |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RXOVFLIF | RXFULLIF(1) | RXHALFIF(1) | RXNEMPTYIF(1) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

**Note 1:** This bit is read-only and reflects the status of the FIFO.

**REGISTER 26-17: CxFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('x' = 1-4); n' = 0 THROUGH 15) (CONTINUED)**

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

**Note 1:** This bit is read-only and reflects the status of the FIFO.

**REGISTER 31-2: PTPER: PRIMARY MASTER TIME BASE PERIOD REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTPER<15:8>(1,2) | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0(3) | R/W-0(3) | R/W-0(3) |
| | PTPER<7:0>(1,2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PTPER<15:0>:** Primary Master Time Base Period Value bits(1,2,4)

**Note 1:** Minimum LSb = 1 / FSYSCLK.

**2:** Minimum value is 0x0008.

**3:** If a period value is lesser than 0x0008 is chosen, the internal hardware forcefully sets the period to a minimum value of 0x0008.

**4:** PTPER = (FSYSCLK / (FPWM * PCLKDIV<2:0> bits (PTCON<6:4>)).
FPWM = User-desired PWM Frequency.

### 32.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MK GP/MC devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

#### 32.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

#### 32.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

**FIGURE 36-14: QEI MODULE EXTERNAL CLOCK TIMING CHARACTERISTICS**

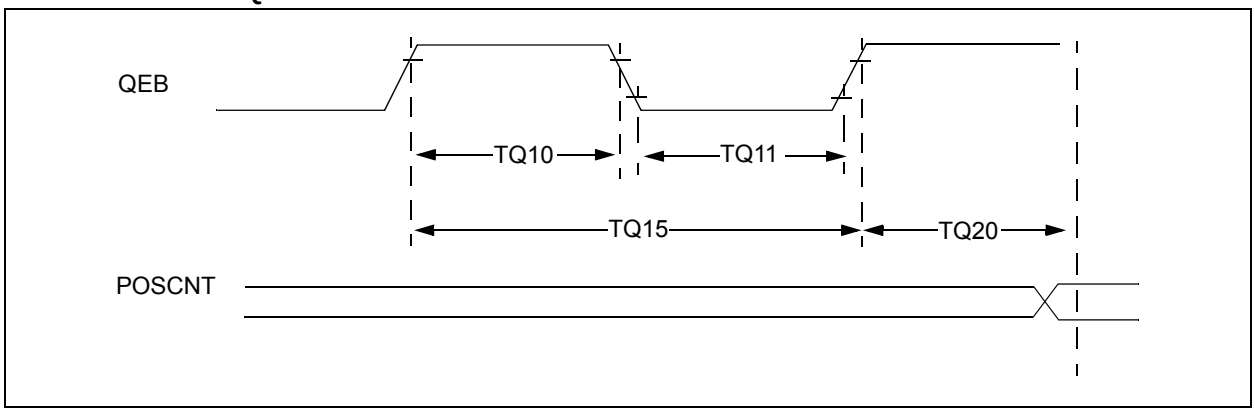



**TABLE 36-36: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TQ10 | TtQH | TQCK High Time | Synchronous, with prescaler | [(12.5 or 0.5 TCY) / N] + 25 | — | — | ns | Must also meet parameter TQ15.<br><br>N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ11 | TtQL | TQCK Low Time | Synchronous, with prescaler | [(12.5 or 0.5 TCY) / N] + 25 | — | — | ns | Must also meet parameter TQ15.<br><br>N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ15 | TtQP | TQCP Input Period | Synchronous, with prescaler | [(25 or TCY) / N] + 50 | — | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | 1 | TCY | — | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** N = Index Channel Digital Filter Clock Divide Select bits.

# APPENDIX A: REVISION HISTORY

## Revision A (April 2016)

This is the initial released version of the document.

## Revision B (September 2016)

This revision of the document was updated to include information for PIC32MK Motor Control (MC) devices.

## Revision C (December 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps** | Removed $I^2C$ and HLVD references (see Table 1 and Table 2). Updated pin names to remove references to $I^2C$ and HLVD, added Notes 6 and 7 for 64-pin devices, and Notes 5 and 6 for 100-pin devices (see Table 3, Table 4, Table 5, and Table 6). Removed references to FRM Section 24 and Section 38 (see Referenced Sources). |
| **1.0 "Device Overview"** | Removed original Table 1-9. Removed HLVD reference and added a new Note 1 (see Table 1-20). |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | **2.1 "Basic Connection Requirements"** - removed bullet point discussing $V_{CAP}$. In Figure 2-4, reversed direction OSC1 and OSC2 arrows. |
| **6.0 "Data EEPROM"** | **6.0 "Data EEPROM"** - updated Note 2. Updated table under Note 2. |
| **7.0 "Resets"** | Removed HLVD references (see Table 7-1 and Register 7-3). |
| **8.0 "CPU Exceptions and Interrupt Controller"** | Added Note 2 (see Table 8-1). Removed $I^2C$ references (see Table 8-3). Added Note 7 (see Table 8-4). |
| **9.0 "Oscillator Configuration"** | Corrected typo to "POSCMOD", added PWM block to connect to SYSCLK (see Figure 9-1). Removed $I^2C$ and HLVD references (see Table 9-1). |
| **21.0 "Inter-Integrated Circuit ($I^2C$)"** | **21.0 "Inter-Integrated Circuit ($I^2C$)"** - Removed original chapter contents and added an intro that points to MPLAB Harmony, Notes 5 and 6 for 100-pin devices, and Notes 6 and 7 for 64-pin devices. |
| **22.0 "Universal Asynchronous Receiver Transmitter (UART)"** | Corrected the label for bit 19-0 (see Register 22-5). |
| **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** | Updated the definition list for bit 20-16 (see Register 25-17).<br>Added Note 1 to Register 25-4. |
| **27.0 "Op Amp/Comparator Module"** | Removed $I^2C$ reference (see Figure 27-2). Removed $I^2C$ and HLVD references (see Figure 27-5). Updated CDAC1 to CDAC3, and added Note 3 (see Figure 27-1, Figure 27-2, Figure 27-3, Figure 27-4, and Figure 27-5). Removed CEVT labels from bit 9. Changed bit 9 definition to "unimplemented" (see Table 27-2). Removed CEVT references, changed bit 9 definition to "unimplemented", and added two notes (see Register 27-2). |