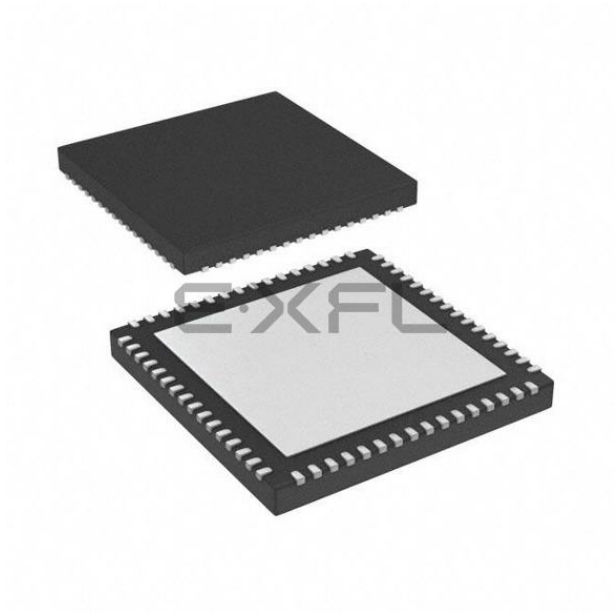

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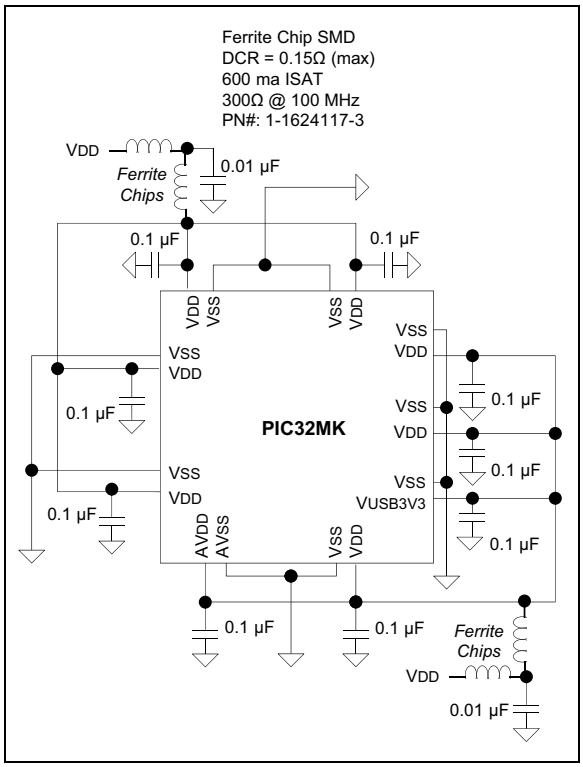
Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpe064-i-mr

2.10.1.3 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/Boost regulators as the local power source for PIC32MK GP devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-9. In addition to a more stable power source, use of this type of T-Filter can greatly reduce susceptibility to EMI sources and events.

FIGURE 2-9: EMI/EMC/EFT SUPPRESSION CIRCUIT



REGISTER 7-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI reset counter.
11111111-00000001 = Number of SYSCLK cycles before a device Reset occurs(1)
00000000 = No delay between NMI assertion and device Reset event

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered the NMICNT will start decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit is written. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 12-2: UxOTGIE: USB OTG INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = ID interrupt is enabled
0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = 1 millisecond timer interrupt is enabled
0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
1 = Line state interrupt is enabled
0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = ACTIVITY interrupt is enabled
0 = ACTIVITY interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Session valid interrupt is enabled
0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
1 = B-session end interrupt is enabled
0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
1 = A-VBUS valid interrupt is enabled
0 = A-VBUS valid interrupt is disabled

13.4 I/O Ports Control Registers

TABLE 13-3: PORTA REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSA15	ANSA14	—	ANSA12	ANSA11	—	—	ANSA8	—	—	—	ANSA4	—	—	ANSA1	ANSA0	D813
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	TRISA12	TRISA11	TRISA10	—	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	DD93
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	RA12	RA11	RA10	—	RA8	RA7	—	—	RA4	—	—	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	LATA12	LATA11	LATA10	—	LATA8	LATA7	—	—	LATA4	—	—	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	ODCA12	ODCA11	ODCA10	—	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA15	CNPUA14	—	CNPUA12	CNPUA11	CNPUA10	—	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA15	CNPDA14	—	CNPDA12	CNPDA11	CNPDA10	—	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEA15	CNIEA14	—	CNIEA12	CNIEA11	CNIEA10	—	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATA15	CN STATA14	—	CN STATA12	CN STATA11	CN STATA10	—	CN STATA8	CN STATA7	—	—	CN STATA4	—	—	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEA15	CNNEA14	—	CNNEA12	CNNEA11	CNNEA10	—	CNNEA8	CNNEA7	—	—	CNNEA4	—	—	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFA15	CNFA14	—	CNFA12	CNFA11	CNFA10	—	CNFA8	CNFA7	—	—	CNFA4	—	—	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR0A10	—	SR0A8	SR0A7	—	—	—	—	—	—	—	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR1A10	—	SR1A8	SR1A7	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 16-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R-0
	BAD1	BAD2	DMTEVENT					WINOPN

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Bad STEP1<7:0> Value Detect bit
1 = Incorrect STEP1<7:0> value was detected
0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Bad STEP2<7:0> Value Detect bit
1 = Incorrect STEP2<7:0> value was detected
0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
1 = Deadman timer event was detected (counter expired or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
0 = Deadman timer even was not detected

Note: This bit is cleared only on a Reset.

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
1 = Deadman timer clear window is open
0 = Deadman timer clear window is not open

REGISTER 22-3: UxRXREG: UARTx RECEIVE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	RX<8>
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RX<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **RX<8>:** Data bit 8 of the received character (in 9-bit mode)

bit 7-0 **RX<7:0>:** Data bits 7-0 of the received character

REGISTER 22-4: UxTXREG: UARTx TRANSMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-x	U-x	U-x	U-x	U-x	U-x	U-x	U-x
	—	—	—	—	—	—	—	—
23:16	U-x	U-x	U-x	U-x	U-x	U-x	U-x	U-x
	—	—	—	—	—	—	—	—
15:8	U-x	U-x	U-x	U-x	U-x	U-x	U-x	W-x
	—	—	—	—	—	—	—	TX<8>
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	TX<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as initialized data

bit 8 **TX<8>:** Data bit 8 of the transmitted character (in 9-bit mode)

bit 7-0 **TX<7:0>:** Data bits 7-0 of the transmitted character

22.2 UART Broadcast Mode Example

As shown in Table 22-4, the group hardware address identifier bit was arbitrarily chosen as bit 7 with bit 4 chosen as the software group or individual UART target ID. Therefore, the collective group address assigned for all UARTs (i.e, [w, x, y, z]) is ‘0b100100xx, while the individual addresses are ‘0b10000000 through ‘0b10000011, respectively.

Any MASK register bit = 0 means the corresponding ADDR<7:0> bit is a “don't care” from a hardware address matching point of view. Using this scheme, multiple UART subnet groups could be created within a network. If not using address match with a broadcast mode, set the ADDRMSK<7:0> bits (UxSTAT<31:24) = 0x00, which is the default.

To send a broadcast message to all UARTs in the group identified by bit 7 = 1, send UxTXREG = (0x190), address bit 9 set. All the UARTs in that group, bit 7 = 1, would generate an interrupt for an address match because of the bit <7:5>,<3:2> match, Logic AND of MASK and ADDR registers equal “true”. User software would check if bit 4 = 1, and if true, the RX<7:0> bits register value is valid for all UARTS.

To send a specific message to UARTy within the group, the user would send UxTXREG = (0x182), address bit 9 set. All of the UARTs in that group identified with bit 7 = 1 would still generate an interrupt for an address match because of the bit <7:5>,<3:2> address match, Logic AND of MASK and ADDR registers equal True. In this case, user software would check if bit 4 = 0, and if true, the RX<7:0> bits register value would be intended only for UARTy, with all others ignored.

TABLE 22-4: PDSEL<1:0> (UxMODE<2:1>) = ‘0b11 AND ADM_EN (UxSTA<24>) = 1

Networked UARTS	Register Bit	7	6	5	4	3	2	1	0	Individual/ Group Addresses
UARTx	ADDRMSK	1	1	1	0	1	1	0	0	0xBC
UARTw	ADDR	1	0	0	1 = Group 0 = Individual	0	0	0	0	0x80/0x9X
UARTx	ADDR	1	0	0	1 = Group 0 = Individual	0	0	0	1	0x81/0x9X
UARTy	ADDR	1	0	0	1 = Group 0 = Individual	0	0	1	0	0x82/0x9X
UARTz	ADDR	1	0	0	1 = Group 0 = Individual	0	0	1	1	0x83/0x9X

REGISTER 25-28: ADCDSTAT: ADC DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAEN	---	RBFIE5	RBFIE4	RBFIE3	RBFIE2	RBFIE1	RBFIE0
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	WOVERR	---	RBF5	RBF4	RBF3	RBF2	RBF1	RBF0
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMACEN	---	RAFIE5	RAFIE4	RAFIE3	RAFIE2	RAFIE1	RAFIE0
7:0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	---	---	RAF5	RAF4	RAF3	RAF2	RAF1	RAF0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DMAEN:** Global ADC DMA Enable bit
1 = DMA interface is enabled
0 = DMA interface is disabled
When DMAEN = 0, no data is being saved into internal SRAM, no SRAM Writes occur and the DMA interface logic is being kept in reset state.

Note: Before setting the DMAEN bit to '1', the user application must ensure that the BCHEN bit (ADCxTIME<23>) is configured as needed.

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **RBFIE5:RBFIE0:** RAM DMA Buffer B Full Interrupt Enable bits for ADC5-ADC0
1 = Enable ping-pong DMA Buffer B interrupt requests for ADC5-ADC0
0 = Disable ping-pong DMA Buffer B interrupt requests for ADC5-ADC0

bit 23 **WOVERR:** DMA FIFO Write Overflow Error bit
This bit is set by hardware and cleared by hardware after a software read of the ADCDSTAT register. The write always occurs and the old data is replaced with the new data because the software missed reading the old data on time.

bit 22 **Unimplemented:** Read as '0'

bit 21-16 **RBF5:RBF0:** RAM DMA Buffer B Full Status bits for ADC5-ADC0
1 = RAM DMA ping-pong Buffer B is full
0 = RAM DMA pin-pong Buffer B is not full

These bits are self-clearing upon being read by software. When RBFIEx = 1 and the RBFx bit status is set, the individual ADCx DMA interrupt request is generated.

bit 15 **DMACEN:** ADC DMA Buffer Sample Count Enable bit
The DMA interface will save the current sample count for each buffer in the table starting at the ADCCNTB address after each sample write into the corresponding buffer in the SRAM.

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **RAFIE5:RAFIE0:** RAM DMA Buffer A Full Interrupt Enable bits for ADC5-ADC0
1 = Enable ping-pong DMA Buffer A interrupt requests for ADC5-ADC0
0 = Disable ping-pong DMA Buffer A interrupt requests for ADC5-ADC0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RAF5:RAF0:** RAM DMA Ping-Pong Buffer A Full Status bits for ADC5-ADC0
1 = RAM DMA ping-pong Buffer A is full
0 = RAM DMA ping-pong Buffer A is not full

These bits are self-clearing upon being read by software. When RAFIEx = 1 and the RAFx bit status is set, the individual ADCx DMA interrupt request is generated.

Note: The individual Class 1 High-Speed ADC5-ADC0 modules have an independent DMA bus master and are completely separate from the assignable general purpose DMA channels.

REGISTER 25-40: ADCSYSCFG0: ADC SYSTEM CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	—	—	—	—	AN27	AN26	AN25	AN24
23:16	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN23(1)	AN22(1)	AN21(1)	AN20(1)	AN19	AN18	AN17	AN16
15:8	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8
7:0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Legend:	HS = Hardware Set	HC = Cleared by Software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AN27:AN0>:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<31:0>: Reflects the presence or absence of the respective analog input (AN31-AN0).

Note 1: This bit is not available on 64-pin devices.

29.0 CONTROL DIGITAL-TO-ANALOG CONVERTER (CDAC)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MK GP/MC Family Control Digital-to-Analog Converter (CDAC) generates analog voltage corresponding to the digital inputs. The voltage can be used as a reference source for comparators or can be used as an offset to an Op amp. This module is targeted for control applications, as opposed to other DAC modules, which are used for audio applications.

The following are key features of the CDAC module:

- Wide voltage range (1.8V to 3.6V)
- 12-bit resolution
- Fast conversion times, 1 Msps
- Buffered output for comparator use

Note: For additional information on conversion time, sampling rate, module turn-on time and glitch reduction circuit characteristics, refer to **Section 36.0 "Electrical Characteristics"**.

Figure 29-1 illustrates the functional block diagram of the CDAC module.

FIGURE 29-1: CDAC BLOCK DIAGRAM

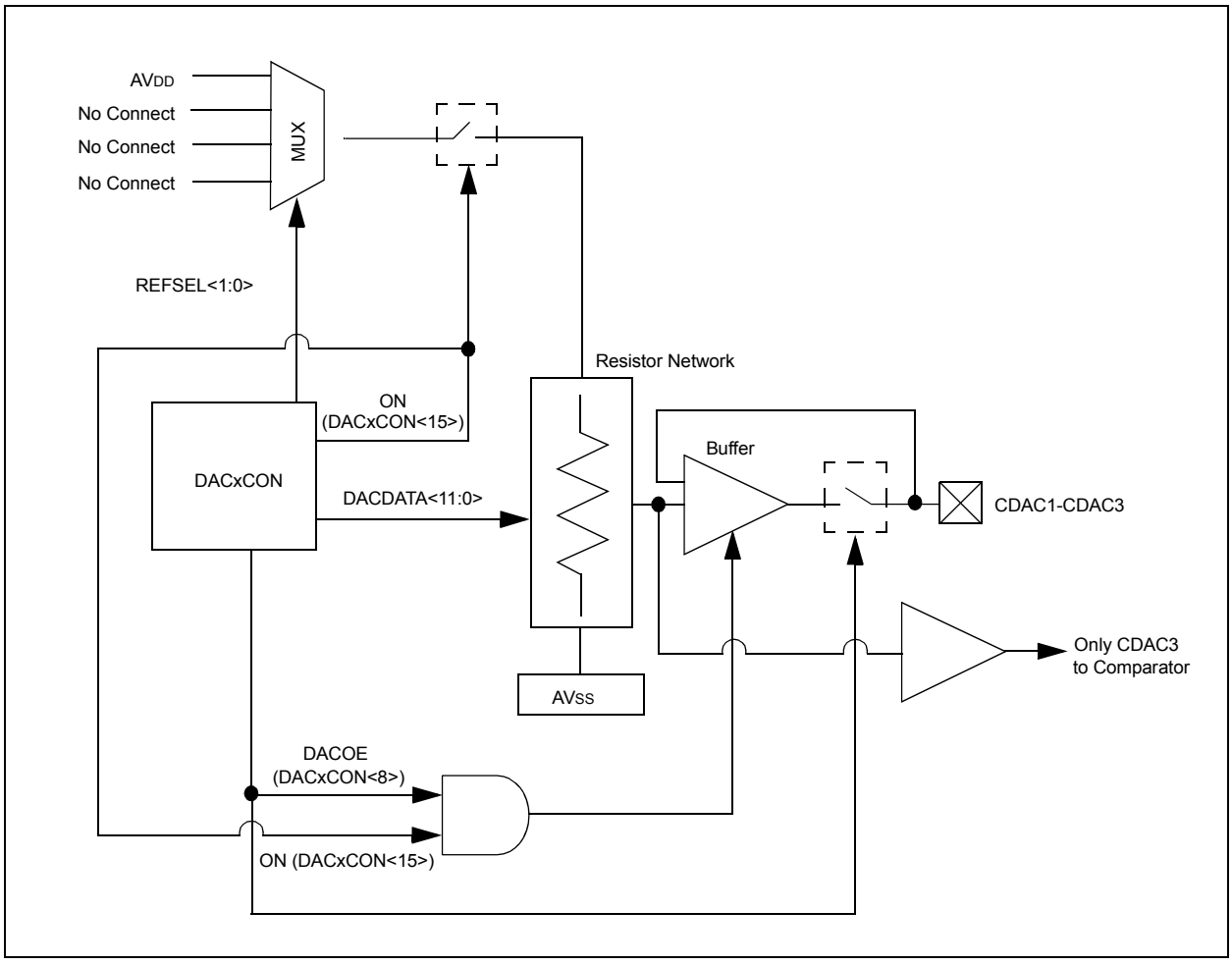


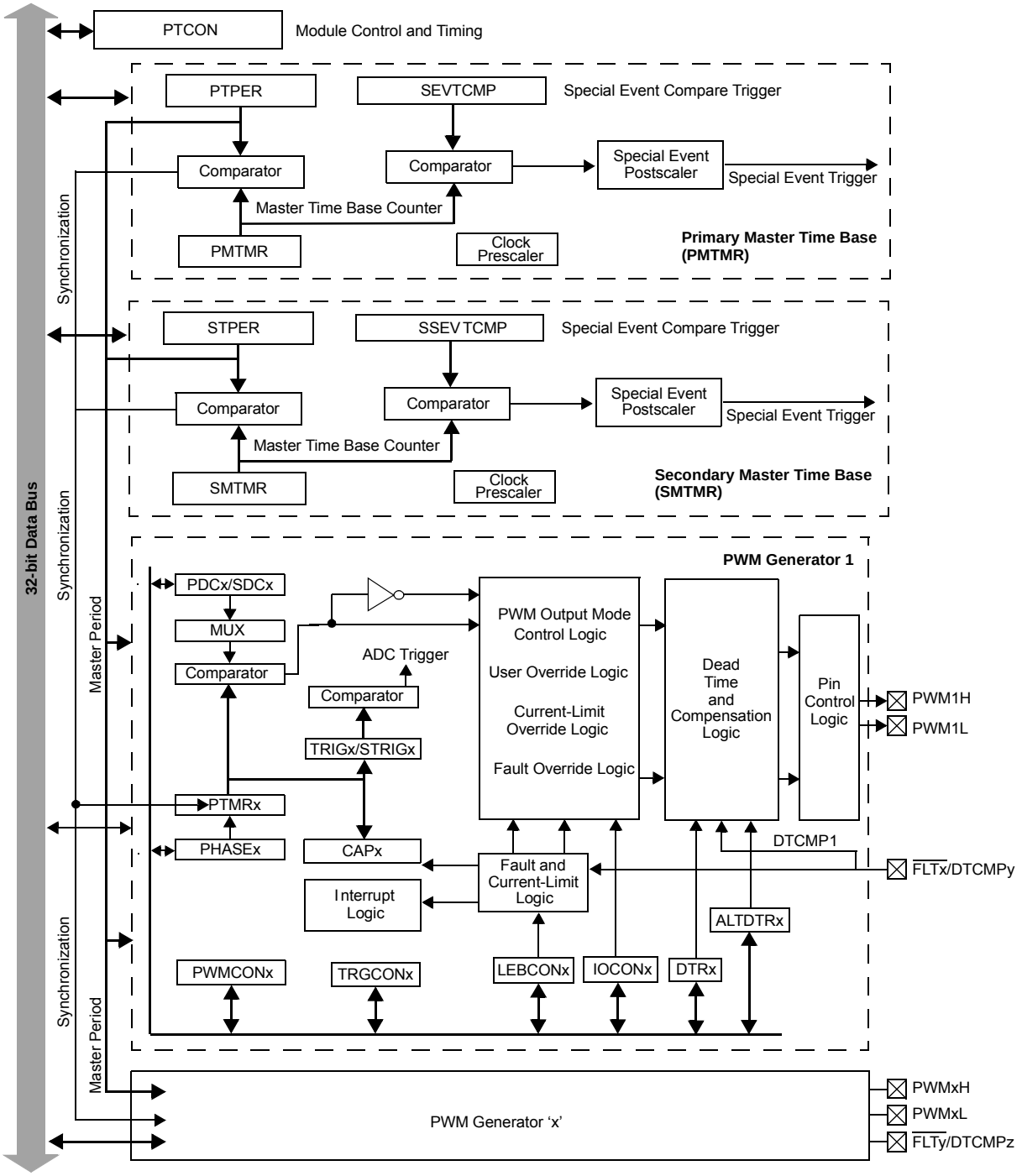
TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
BAB0	QEI5ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
BAC0	QEI5CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000
BC00	QEI6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
BC10	QEI6IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
BC20	QE6STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
BC30	POS6CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
BC40	POS6HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000
BC50	VEL6CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
BC60	VEL6HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
BC70	INT6TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000
BC80	INT6HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
BC90	INDX6CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
BCA0	INDX6HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000
BCB0	QEI6ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
BCC0	QEI6CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

FIGURE 31-2: MOTOR CONTROL PWM MODULE REGISTER INTERCONNECTION DIAGRAM



Legend:

'x' = 1 through 12.
'y' = 1 through 8 and 15.
'z' = 3 through 8.

Note: Since DTCMPx and $\overline{\text{FLTx}}$ share the same digital input pins, their availability is mutually exclusive.

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A890	LEBDLY8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A8A0	AUXCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A8B0	PTMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A8C0	PWMCON9	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A8D0	IOCON9	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A8E0	PDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A8F0	SDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A900	PHASE9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A910	DTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
A920	ALTDTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
A930	DTCOMP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A940	TRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A950	TRGCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A960	STRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A970	CAP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A980	LEBCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A990	LEBDLY9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000

Legend: '—' = unimplemented; read as '0'.

32.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes the power-saving features on the PIC32MK GP devices. These devices have multiple power domains and offer various methods and modes that allow the user to balance the power consumption with device performance.

32.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the speed of PBCLK7, or selecting a lower power clock source (i.e., LPRC or SOSC).

In addition, the Peripheral Bus Scaling mode is available for each peripheral bus where peripherals are clocked at reduced speed by selecting a higher divider for the associated PBCLKx, or by disabling the clock completely.

32.2 Power-Saving with CPU Halted

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

32.2.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted and the associated clocks are disabled. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the peripheral bus clocks will start running and the device will enter into Idle mode.

32.2.2 IDLE MODE

In Idle mode, the CPU is Halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

TABLE 32-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits															All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0280	DSGPR29	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0284	DSGPR30	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0288	DSGPR31	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
028C	DSGPR32	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice. In addition, to ensure the write is successful, these registers must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

TABLE 32-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

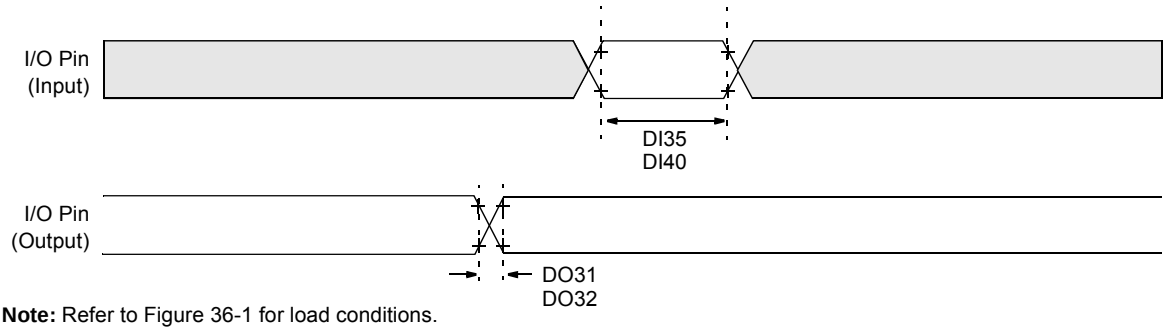
Peripheral	PMDx Bit Name(3)	Register Name and Bit Location
ADC1-ADC7	ADC1MD	PMD1<0>
CDAC1	DAC1MD	PMD1<4>
CDAC2	DAC2MD	PMD1<5>
CDAC3	DAC3MD	PMD1<6>
CTMU	CTMU1MD	PMD1<8>
Data EEPROM	EEMD	PMD1<9>
Comparator 1	C1MD	PMD2<0>
Comparator 2	C2MD	PMD2<1>
Comparator 3	C3MD	PMD2<2>
Comparator 4	C4MD	PMD2<3>
Comparator 5	C5MD	PMD2<4>
Op amp 1	OPA1MD	PMD2<16>
Op amp 2	OPA2MD	PMD2<17>
Op amp 3	OPA3MD	PMD2<18>
Op amp 5	OPA5MD	PMD2<20>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Input Capture 10	IC10MD	PMD3<9>
Input Capture 11	IC11MD	PMD3<10>
Input Capture 12	IC12MD	PMD3<11>
Input Capture 13	IC13MD	PMD3<12>
Input Capture 14	IC14MD	PMD3<13>
Input Capture 15	IC15MD	PMD3<14>
Input Capture 16	IC16MD	PMD3<15>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

3: For any associated PMDx bit, `0` = clocks enabled to the peripheral; `1` = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

FIGURE 36-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-22: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS		**Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	**Port Output Rise Time** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15, RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5-RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - Replace 8x Source Driver pins with: RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6-RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 36-43: CTMU CURRENT SOURCE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU CURRENT SOURCE							
CTMU0	RES	Resolution	-2	—	+2	ºC	3.3V @ -40ºC to 125ºC
CTMUI1	IOUT1	Base Range(1)	—	0.55	—	µA	CTMUCON<1:0> = 01
CTMUI2	IOUT2	10x Range(1)	—	5.5	—	µA	CTMUCON<1:0> = 10
CTMUI3	IOUT3	100x Range(1)	—	55	—	µA	CTMUCON<1:0> = 11
CTMUI4	IOUT4	1000x Range(1)	—	550	—	µA	CTMUCON<1:0> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage(1,2)	—	0.598	—	V	TA = +25ºC, CTMUCON<1:0> = 01
			—	0.658	—	V	TA = +25ºC, CTMUCON<1:0> = 10
			—	0.721	—	V	TA = +25ºC, CTMUCON<1:0> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change(1,2)	—	-1.92	—	mV/ºC	CTMUCON<1:0> = 01
			—	-1.74	—	mV/ºC	CTMUCON<1:0> = 10
			—	-1.56	—	mV/ºC	CTMUCON<1:0> = 11

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL