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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpe064-i-pt

PIC32MK GP/MC Family

TABLE 1-9: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Timer1 through Timer9					
T1CK	51	33	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar					
RTCC	27	18	O	—	Real-Time Clock Alarm/Seconds Output (not in VBAT power domain, requires VDD

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MK GP/MC Family

TABLE 1-21: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
JTAG					
TCK	3	1	I	ST	JTAG Test Clock Input Pin
TDI	49	31	I	ST	JTAG Test Data Input Pin
TDO	100	64	O	—	JTAG Test Data Output Pin
TMS	76	49	I	ST	JTAG Test Mode Select Pin
Trace					
TRCLK	91	50	O	CMOS	Trace Clock
TRD0	97	54	O	CMOS	Trace Data bits 0-3 Trace support is available through the MPLAB® REAL ICE™ In-circuit Emulator.
TRD1	96	53	O	CMOS	
TRD2	95	52	O	CMOS	
TRD3	92	51	O	CMOS	
Programming/Debugging					
PGED1	27	18	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	26	17	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	69	43	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	70	44	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	24	15	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
PGEC3	25	16	I	ST	Clock input pin for Programming/Debugging Communication Channel 3
MCLR	13	7	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0290	IPC21	31:16	—	—	—	OC8IP<2:0>			OC8IS<1:0>			—	—	—	IC8IP<2:0>			IC8IS<1:0>	0000
		15:0	—	—	—	IC8EIP<2:0>			IC8EIS<1:0>			—	—	—	T8IP<2:0>			T8IS<1:0>	0000
02A0	IPC22	31:16	—	—	—	OC9IP<2:0>			OC9IS<1:0>			—	—	—	IC9IP<2:0>			IC9IS<1:0>	0000
		15:0	—	—	—	IC9EIP<2:0>			IC9EIS<1:0>			—	—	—	T9IP<2:0>			T9IS<1:0>	0000
02B0	IPC23	31:16	—	—	—	AD1DC2IP<2:0>			AD1DC2IS<1:0>			—	—	—	AD1DC1IP<2:0>			AD1DC1IS<1:0>	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AD1IP<2:0>			AD1IS<1:0>	0000
02C0	IPC24	31:16	—	—	—	AD1DF4IP<2:0>			AD1DF4IS<1:0>			—	—	—	AD1DF3IP<2:0>			AD1DF3IS<1:0>	0000
		15:0	—	—	—	AD1DF2IP<2:0>			AD1DF2IS<1:0>			—	—	—	AD1DF1IP<2:0>			AD1DF1IS<1:0>	0000
02D0	IPC25	31:16	—	—	—	AD1RSIP<2:0>			AD1RSIS<1:0>			—	—	—	AD1ARIP<2:0>			AD1ARIS<1:0>	0000
		15:0	—	—	—	AD1EOSIP<2:0>			AD1EOSIS<1:0>			—	—	—	AD1F1IP<2:0>			AD1F1IS<1:0>	0000
02E0	IPC26	31:16	—	—	—	AD1D01IP<2:0>			AD1D01IS<1:0>			—	—	—	AD1D00IP<2:0>			AD1D00IS<1:0>	0000
		15:0	—	—	—	AD1G1IP<2:0>			AD1G1IS<1:0>			—	—	—	AD1FCBTIP<2:0>			AD1FCBTIS<1:0>	0000
02F0	IPC27	31:16	—	—	—	AD1D05IP<2:0>			AD1D05IS<1:0>			—	—	—	AD1D04IP<2:0>			AD1D04IS<1:0>	0000
		15:0	—	—	—	AD1D03IP<2:0>			AD1D03IS<1:0>			—	—	—	AD1D02IP<2:0>			AD1D02IS<1:0>	0000
0300	IPC28	31:16	—	—	—	AD1D09IP<2:0>			AD1D09IS<1:0>			—	—	—	AD1D08IP<2:0>			AD1D08IS<1:0>	0000
		15:0	—	—	—	AD1D07IP<2:0>			AD1D07IS<1:0>			—	—	—	AD1D06IP<2:0>			AD1D06IS<1:0>	0000
0310	IPC29	31:16	—	—	—	AD1D13IP<2:0>			AD1D13IS<1:0>			—	—	—	AD1D12IP<2:0>			AD1D12IS<1:0>	0000
		15:0	—	—	—	AD1D11IP<2:0>			AD1D11IS<1:0>			—	—	—	AD1D10IP<2:0>			AD1D10IS<1:0>	0000
0320	IPC30	31:16	—	—	—	AD1D17IP<2:0>			AD1D17IS<1:0>			—	—	—	AD1D16IP<2:0>			AD1D16IS<1:0>	0000
		15:0	—	—	—	AD1D15IP<2:0>			AD1D15IS<1:0>			—	—	—	AD1D14IP<2:0>			AD1D14IS<1:0>	0000
0330	IPC31	31:16	—	—	—	AD1D21IP<2:0>			AD1D21IS<1:0>			—	—	—	AD1D20IP<2:0>			AD1D20IS<1:0>	0000
		15:0	—	—	—	AD1D19IP<2:0>			AD1D19IS<1:0>			—	—	—	AD1D18IP<2:0>			AD1D18IS<1:0>	0000
0340	IPC32	31:16	—	—	—	AD1D25IP<2:0>			AD1D25IS<1:0>			—	—	—	AD1D24IP<2:0>			AD1D24IS<1:0>	0000
		15:0	—	—	—	AD1D23IP<2:0>			AD1D23IS<1:0>			—	—	—	AD1D22IP<2:0>			AD1D22IS<1:0>	0000
0350	IPC33	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AD1D27IP<2:0>			AD1D27IS<1:0>			—	—	—	AD1D26IP<2:0>			AD1D26IS<1:0>	0000
0360	IPC34	31:16	—	—	—	AD1D33IP<2:0>			AD1D33IS<1:0>			—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See 13.2 "CLR, SET, and INV Registers" for more information.
- 2: This bit is not available on 64-pin devices.
- 3: This bit is not available on devices without a CAN module.
- 4: This bit is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.
- 7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FRCDIV<2:0>		
23:16	R/W-0	U-0	R/W-y	U-0	U-0	U-0	U-0	U-0
	DRMEN	—	SLP2SPD	—	—	—	—	—
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0, HS	R/W-0	R/W-y	R/W-y
	CLKLOCK	—	—	SLPEN	CF	UFRGEN	SOSCEN	OSWEN ⁽¹⁾

Legend:	y = Value set from Configuration bits on POR	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2
- 000 = FRC divided by 1 (default setting)

bit 23 **DRMEN:** Dream Mode Enable bit

- 1 = Dream mode is enabled
- 0 = Dream mode is disabled

bit 22 **Unimplemented:** Read as '0'

bit 21 **SLP2SPD:** Sleep Two-speed Start-up Control bit

- 1 = Use FRC as SYSCLK until the selected clock is ready
- 0 = Use the selected clock directly

bit 20-15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

- 111 = Reserved
- 110 = Reserved
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (Sosc)
- 011 = USB PLL (UPLL) input clock and divider are set by UPLLCON
- 010 = Primary Oscillator (Posc) (HS or EC)
- 001 = System PLL (SPLL) input clock and divider set by SPLLCON
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV) supports FRN divided by N, where 'N' is 1, 2, 4, 8, 16, 32, 64, and 256

bit 11 **Unimplemented:** Read as '0'

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 11-16: DCHxCSIZ: DMA CHANNEL x CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event

.

.

.

0000000000000010 = 2 bytes transferred on an event

0000000000000001 = 1 byte transferred on an event

0000000000000000 = 65,536 bytes transferred on an event

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REGISTER 12-18: UxBDTP2: USB BDT PAGE 2 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 12-19: UxBDTP3: USB BDT PAGE 3 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

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TABLE 13-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPB14	RPB14R	RPB14R<4:0>	00000 = Off 00001 = U1RTS 00010 = U2TX 00011 = Reserved 00100 = SS2 00101 = OC3 00110 = OC6 00111 = C1OUT 01000 = Reserved 01001 = OC11 01010 = OC15 01011 = U5TX 01100 = C2TX 01101 = Reserved 01110 = SCK3 01111 = SDO4 10000 = SCK5 10001 = SDO6 10010 = CTPLS 10011 = Reserved 10100 = QEICMP4 10101 = Reserved . . . 11111 = Reserved
RPC12	RPC12R	RPC12R<4:0>	
RPB0	RPB0R	RPB0R<4:0>	
RPB10	RPB10R	RPB10R<4:0>	
RPB9	RPB9R	RPB9R<4:0>	
RPC9	RPC9R	RPC9R<4:0>	
RPC2	RPC2R	RPC2R<4:0>	
RPE15	RPE15R	RPE15R<4:0>	
RPC10	RPC10R	RPC10R<4:0>	
RPG9	RPG9R	RPG9R<4:0>	
RPG12 ⁽¹⁾	RPG12R ⁽¹⁾	RPG12R<4:0>	
RPG1 ⁽¹⁾	RPG1R ⁽¹⁾	RPG1R<4:0> ⁽¹⁾	
RPD3 ⁽¹⁾	RPD3R ⁽¹⁾	RPD3R<4:0> ⁽¹⁾	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP

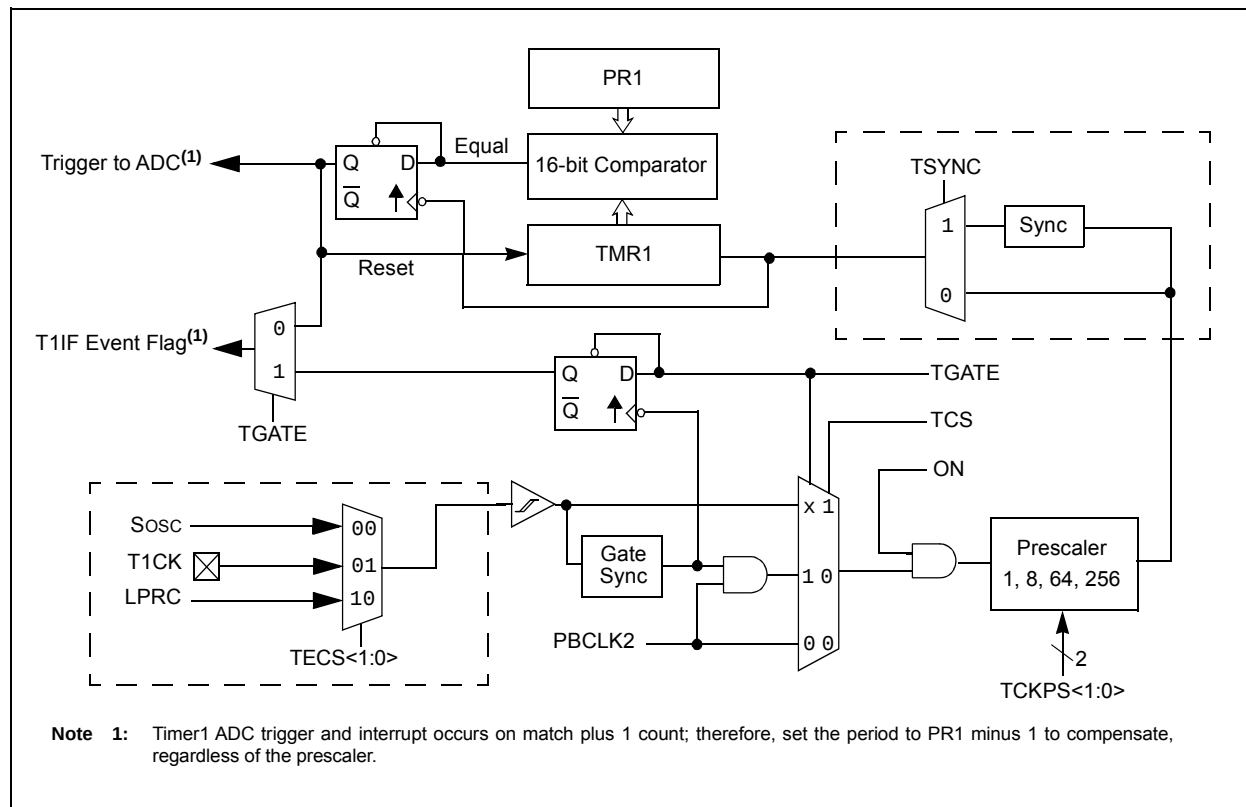
Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1404	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
1408	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
140C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
1410	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
1418	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
141C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
1420	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
1424	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
1428	T6CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T6CKR<3:0>				0000
142C	T7CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T7CKR<3:0>				0000
1430	T8CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T8CKR<3:0>				0000
1434	T9CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T9CKR<3:0>				0000
1438	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
143C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
1440	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: This register is not available on 64-pin devices.
 - 2: This register is not available on devices without a CAN module.
 - 3: This register is only available on PIC32MKXXGPEXXX devices.

PIC32MK GP/MC Family

FIGURE 14-1: TIMER1 BLOCK DIAGRAM



PIC32MK GP/MC Family

REGISTER 25-20: ADCTRG3: ADC TRIGGER SOURCE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC11<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC10<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC9<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC8<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC11<4:0>**: Trigger Source for Conversion of Analog Input AN11 Select bits

11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge Only)
10010 = Output Compare 3 (Rising Edge Only)
10001 = Output Compare 2 (Rising Edge Only)
10000 = Output Compare 1 (Rising Edge Only)
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary Special Event trigger (Motor Control only)
01000 = Primary Special Event trigger (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

30.0 QUADRATURE ENCODER INTERFACE (QEI)

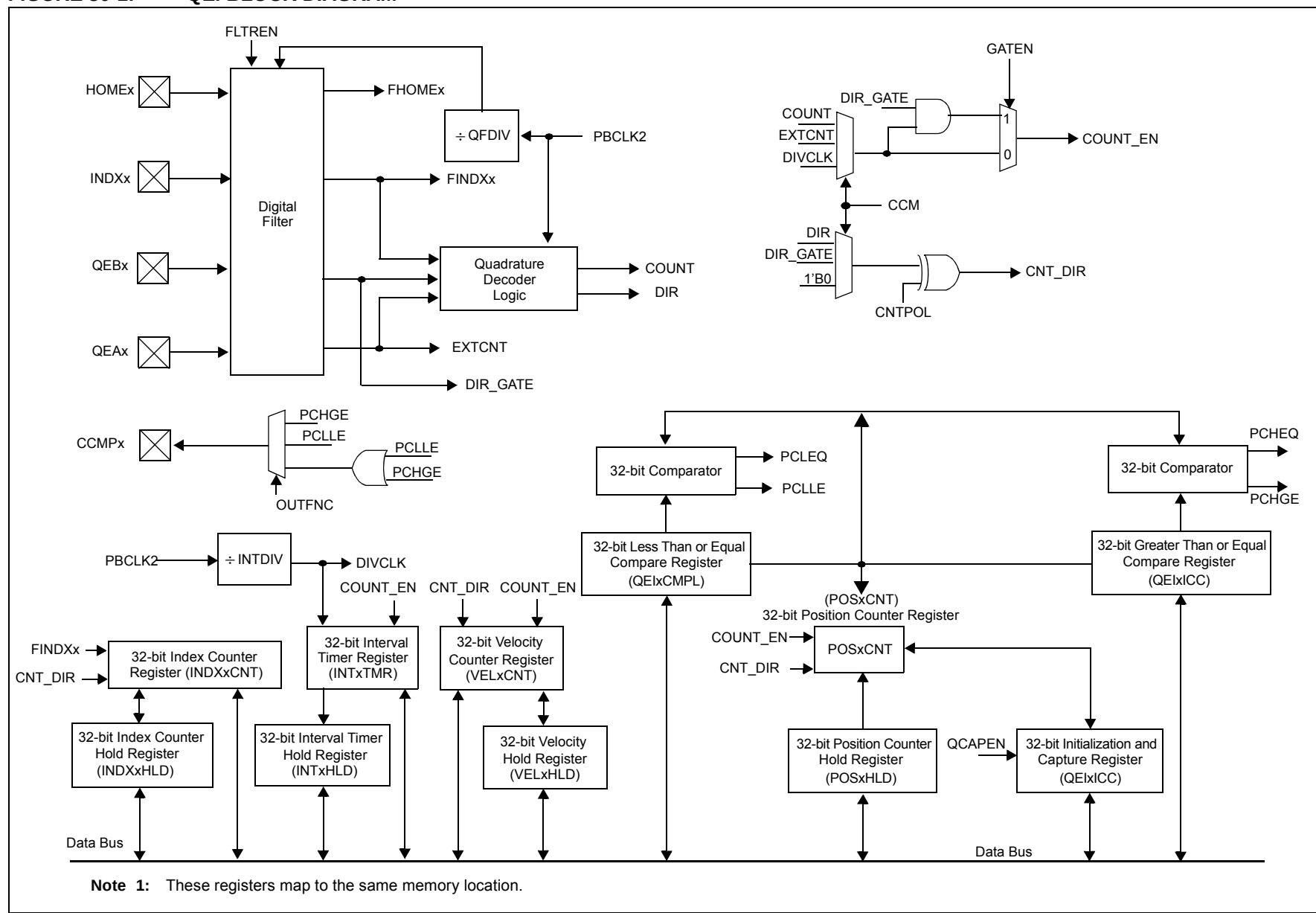
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 43. “Quadrature Encoder Interface (QEI)”** (DS60001346), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The QEI module consists of the following major features:

- Four input pins: two phase signals, an index pulse and a home pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- Count direction status
- 4x count resolution
- Index (INDX) pulse to reset the position counter
- General purpose 32-bit Timer/Counter mode
- Interrupts generated by QEI or counter events
- 32-bit velocity counter
- 32-bit position counter
- 32-bit index pulse counter
- 32-bit interval timer
- 32-bit position Initialization/Capture register
- 32-bit Compare Less Than and Greater Than registers
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Interval Timer mode

Figure 30-1 illustrates the QEI block diagram.

FIGURE 30-1: QEI BLOCK DIAGRAM

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REGISTER 30-10: QE1xICC: QE1x INITIALIZE/CAPTURE/COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **ICCH<31:0>**: 32-bit Initialize/Capture/Compare High bits

REGISTER 30-11: QE1xCMPL: CAPTURE LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CMPL<31:0>**: 32-bit Compare Low Value bits

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A890	LEBDLY8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A8A0	AUXCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000	
A8B0	PTMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A8C0	PWMCON9	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A8D0	IOCON9	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A8E0	PDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A8F0	SDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A900	PHASE9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A910	DTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
A920	ALTDTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
A930	DTCOMP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A940	TRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A950	TRGCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A960	STRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A970	CAP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A980	LEBCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A990	LEBDLY9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000

Legend: '—' = unimplemented; read as '0'.

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REGISTER 31-3: SEVTCMP: PWM PRIMARY SPECIAL EVENT COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEVTCMP<15:8> ⁽¹⁾							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEVTCMP<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits⁽¹⁾

The special event trigger allows analog-to-digital conversions to be synchronized to the master PWM time base. The analog-to-digital sampling and conversion time may be programmed to occur at any point within the PWM period.

Note 1: Minimum LSb = 1 / FSYSCLK.

REGISTER 31-4: PMTMR: PRIMARY MASTER TIME BASE TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PMTMR<15:8> ⁽¹⁾							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PMTMR<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMTMR<15:0>:** Primary Master Time Base Timer Value bits⁽¹⁾

This timer increments with each PWM clock until the PTPER value is reached.

Note 1: LSb = 1 / FSYSCLK.

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REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 29-26 **CLSRC<3:0>**: Current-Limit Control Signal Source select bit for PWM Generator 'x'^(2,4)

These bits specify the current-limit control signal source.

1111 = FLT15

1110 = Reserved

1101 = Reserved

1100 = Comparator 5

1011 = Comparator 4

1010 = Comparator 3

1001 = Comparator 2

1000 = Comparator 1

0111 = FLT8

0110 = FLT7

0101 = FLT6

0100 = FLT5

0011 = FLT4

0010 = FLT3

0001 = FLT2

0000 = FLT1

- Note 1:** During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).
- 2:** These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).
- 3:** State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.
- 4:** If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLT_x inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLT_x pin. In addition, DTCMP functions are fixed to specific FLT_x inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;           //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;              //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;         //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;             //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;        //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;           //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;              //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;         //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;             //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;        //Enable Fault for PWM1 on FLT3 pin
```

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REGISTER 31-25: AUXCONx: PWM AUXILIARY CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CHOPSEL<3:0> ⁽¹⁾				CHOPHEN	CHOPLEN

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWM Chop Clock Source Select bits⁽¹⁾

The selected signal will enable and disable (CHOP) the selected PWM outputs.

1111 = Reserved. Do not use

1110 = Reserved. Do not use

1101 = Reserved. Do not use

1100 = PWM12H selected as CHOP clock source

.

.

.

0111 = PWM7H selected as CHOP clock source

.

.

.

0001 = PWM1H selected as CHOP clock source

0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled

0 = PWMxH chopping function is disabled

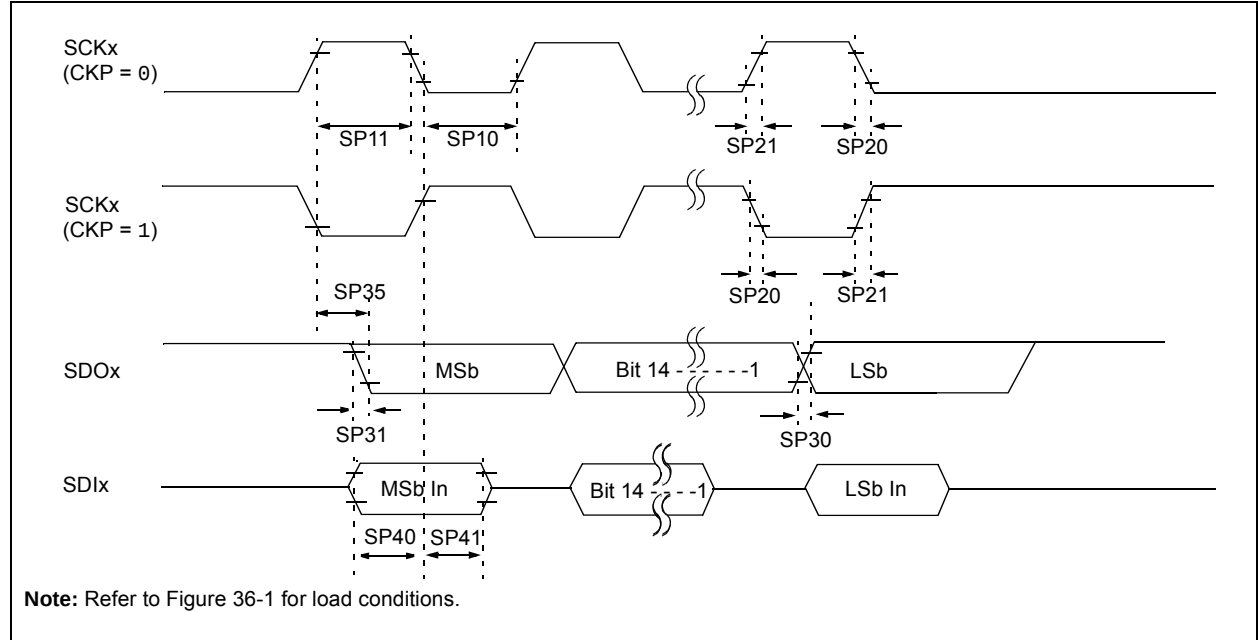
bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled

0 = PWMxL chopping function is disabled

Note 1: This bit should be changed only when the PTEN bit (PTCON<15>) = 0.

FIGURE 36-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



PIC32MK GP/MC Family

TABLE 36-35: SPIx MODULE SLAVE MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

TABLE 36-40: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS ⁽²⁾			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	16.667	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC5 (Class 1 Inputs)	—	—	3.75	Msp/s	12-bit resolution Source Impedance ≤ 200Ω
			—	—	4.284	Msp/s	10-bit resolution Source Impedance ≤ 200Ω
			—	—	4.992	Msp/s	8-bit resolution Source Impedance ≤ 200Ω
			—	—	6	Msp/s	6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	—	—	3.53	Msp/s	12-bit resolution Source Impedance ≤ 200Ω
			—	—	4.00	Msp/s	10-bit resolution Source Impedance ≤ 200Ω
			—	—	4.615	Msp/s	8-bit resolution Source Impedance ≤ 200Ω
			—	—	5.45	Msp/s	6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC5 (Class 1 Inputs)	3	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
			4				
			5				
			13				
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	4	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
			5				
Sample Time for ADC7 (Class 2 and Class 3 Inputs)	6	—	—	TAD	CVDEN (ADCCON1<11>) = 1		
	14						
AD62	TCONV	Conversion Time (after sample time is complete)	—	—	13	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
			—	—	11		
			—	—	9		
			—	—	7		
			—	—	—		
AD65	TWAKE	Wake-up time from Low-Power Mode	—	500	—	TAD	Lesser of 500 TAD or 20 μs
			—	20	—	μs	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.