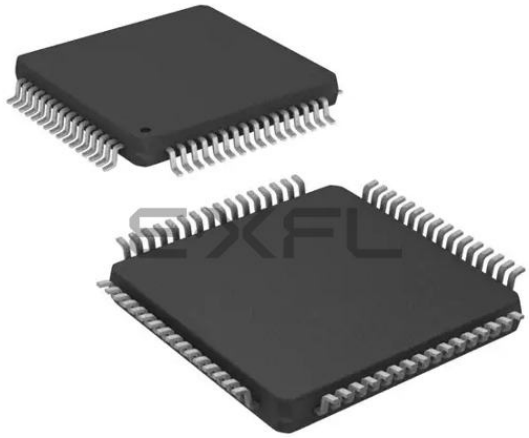
Microchip Technology - PIC32MK0512GPE064T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpe064t-i-pt

NOTES:

TABLE 1-7: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Universal Asynchronous Receiver Transmitter 1					
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2					
U2RX	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3					
U3RX	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4					
U4RX	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5					
U5RX	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6					
U6RX	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-3; 'y' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **GROUP3:** Group 3 Read Permissions bits
- 1 = Privilege Group 3 has read permission
- 0 = Privilege Group 3 does not have read permission

bit 2 **GROUP2:** Group 2 Read Permissions bits
- 1 = Privilege Group 2 has read permission
- 0 = Privilege Group 2 does not have read permission

bit 1 **GROUP1:** Group 1 Read Permissions bits
- 1 = Privilege Group 1 has read permission
- 0 = Privilege Group 1 does not have read permission

bit 0 **GROUP0:** Group 0 Read Permissions bits
- 1 = Privilege Group 0 has read permission
- 0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.
2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00D0	IEC1	31:16	U3RXIE	U3EIE	—	—	—	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	CNGIE	CNFIE	CNEIE	0000
		15:0	CNDIE	CNCIE	CNBIE	CNAIE	—	—	—	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USB1IE	CMP2IE	CMP1IE	0000
00E0	IEC2	31:16	AD1DC2IE	AD1DC1IE	-	AD1IE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
		15:0	OC6IE	IC6IE	IC6EIE	T6IE	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	U5TXIE	U5RXIE	U5EIE	U4TXIE	U4RXIE	U4EIE	U3TXIE	0000
00F0	IEC3	31:16	AD1D21IE	AD1D20IE	AD1D19IE	AD1D18IE	AD1D17IE	AD1D16IE	AD1D15IE	AD1D14IE	AD1D13IE	AD1D12IE	AD1D11IE	AD1D10IE	AD1D09IE	AD1D08IE	AD1D07IE	AD1D06IE	0000
		15:0	AD1D05IE	AD1D04IE	AD1D03IE	AD1D02IE	AD1D01IE	AD1D00IE	AD1G1IE	AD1FCBTIE	AD1RSIE	AD1ARIE	AD1EOSIE	AD1F1IE	AD1DF4IE	AD1DF3IE	AD1DF2IE	AD1DF1IE	0000
0100	IEC4	31:16	AD1D53IE	AD1D52IE	AD1D51IE	AD1D50IE	AD1D49IE	AD1D48IE	AD1D47IE	AD1D46IE	AD1D45IE	—	—	—	AD1D41IE	AD1D40IE	AD1D39IE	AD1D38IE	0000
		15:0	AD1D37IE	AD1D36IE	AD1D35IE	AD1D34IE	AD1D33IE	—	—	—	—	—	AD1D27IE	AD1D26IE	AD1D25IE	AD1D24IE	AD1D23IE	AD1D22IE	0000
0110	IEC5	31:16	QEI5IE	QEI4IE	QEI3IE	CAN4IE(3)	CAN3IE(3)	DATAEEIE	DMA7IE	DMA6IE	DMA5IE	DMA4IE	—	—	—	PWM6IE	PWM5IE	PWM4IE	0000
		15:0	PWM3IE	PWM2IE	PWM1IE	PWM SEVTIE	PWM PEVTIE	QEI2IE	QEI1IE	CAN2IE(3)	CAN1IE(3)	U6TXIE	U6RXIE	U6EIE	—	CMP5IE	CMP4IE	CMP3IE	0000
0120	IEC6	31:16	SPI4TXIE	SPI4RXIE	SPI4EIE	SPI3TXIE	SPI3RXIE	SPI3EIE	OC16IE	IC16IE	IC16EIE	OC15IE	IC15IE	IC15EIE	OC14IE	C14IE	IC14EIE	OC13IE	0000
		15:0	IC13IE	IC13EIE	OC12IE	IC12IE	IC12EIE	OC11IE	IC11IE	IC11EIE	OC10IE	IC10IE	IC10EIE	—	—	—	—	QEI6IE	0000
0130	IEC7	31:16	—	CPCIE	—	—	—	—	—	—	—	AD1DC4IE	AD1DC3IE	USB2IE(2)	PWM12IE	PWM11IE	PWM10IE	PWM9IE	0000
		15:0	—	—	—	—	—	—	—	—	—	SBIE	SPI6TXIE	SPI6RXIE	SPI6EIE	SPI5TXIE	SPI5RXIE	SPI5EIE	0000
0140	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
0150	IPC1	31:16	—	—	—	OC1IP<2:0>			OC1IS<1:0>		—	—	—	IC1IP<2:0>			IC1IS<1:0>		0000
		15:0	—	—	—	IC1EIP<2:0>			IC1EIS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
0160	IPC2	31:16	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	IC2EIP<2:0>			IC2EIS<1:0>		0000
		15:0	—	—	—	T2IP<2:0>			T2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
0170	IPC3	31:16	—	—	—	IC3EIP<2:0>			IC3EIS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
0180	IPC4	31:16	—	—	—	T4IP<2:0>			T4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	OC3IP<2:0>			OC3IS<1:0>		—	—	—	IC3IP<2:0>			IC3IS<1:0>		0000
0190	IPC5	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	IC4EIP<2:0>			IC4EIS<1:0>		0000
01A0	IPC6	31:16	—	—	—	OC5IP<2:0>			OC5IS<1:0>		—	—	—	IC5IP<2:0>			IC5IS<1:0>		0000
		15:0	—	—	—	IC5EIP<2:0>			IC5EIS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

TABLE 9-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1350	PB6DIV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB7DIV(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1380	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
1390	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	UPLLRDY	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
2: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
3: The PB7DIV register is read-only.

REGISTER 9-8: SLEWCON: OSCILLATOR SLEW CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SYSDIV<3:0>(1)			
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SLWDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-0, HS, HC
	—	—	—	—	—	UPEN	DNEN	BUSY

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-16 **SYSDIV<3:0>:** System Clock Divide Control bits(1)

1111 = SYSCLK is divided by 16
1110 = SYSCLK is divided by 15
.
.
.
0010 = SYSCLK is divided by 3
0001 = SYSCLK is divided by 2
0000 = SYSCLK is not divided

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **SLWDIV<2:0>:** Slew Divisor Steps Control bits

These bits control the maximum division steps used when slewing during a frequency change.
111 = Steps are divide by 128, 64, 32, 16, 8, 4, 2, and then no divisor
110 = Steps are divide by 64, 32, 16, 8, 4, 2, and then no divisor
101 = Steps are divide by 32, 16, 8, 4, 2, and then no divisor
100 = Steps are divide by 16, 8, 4, 2, and then no divisor
011 = Steps are divide by 8, 4, 2, and then no divisor
010 = Steps are divide by 4, 2, and then no divisor
001 = Steps are divide by 2, and then no divisor
000 = No divisor is used during slewing
The steps apply in reverse order (i.e., 2, 4, 8, etc.) during a downward frequency change.

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **UPEN:** Upward Slew Enable bit

1 = Slewing enabled for switching to a higher frequency
0 = Slewing disabled for switching to a higher frequency

bit 1 **DNEN:** Downward Slew Enable bit

1 = Slewing enabled for switching to a lower frequency
0 = Slewing disabled for switching to a lower frequency

bit 0 **BUSY:** Clock Switching Slewing Active Status bit

1 = Clock frequency is being actively slewed to the new frequency
0 = Clock switch has reached its final value

Note 1: The SYSDIV<3:0> bit settings are ignored if both UPEN and DNEN = 0, and SYSCLK will be divided by 1.

REGISTER 11-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO(1)	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>(1,2,3)				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP(1)	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1,2,3)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.
2: The maximum CRC length supported by the DMA module is 32.
3: This bit is unused when CRCTYP is equal to '1'.

18.1 Input Capture Control Registers

TABLE 18-2: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 9 REGISTER MAP

Virtual Address BF82_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx
2A00	IC6CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2A10	IC6BUF	31:16	IC6BUF<31:0>																xxxx
		15:0																	xxxx
2C00	IC7CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2C10	IC7BUF	31:16	IC7BUF<31:0>																xxxx
		15:0																	xxxx
2E00	IC8CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2E10	IC8BUF	31:16	IC8BUF<31:0>																xxxx
		15:0																	xxxx
3000	IC9CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3010	IC9BUF	31:16	IC9BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

21.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Inter-Integrated Circuit"** (DS00000000), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The I^2C software library is available in MPLAB Harmony. If the user application is to implement I^2C, for future device pin compatibility, it is recommended to assign software I^2C functions according to the details provided in the device pin tables (Table 3 through Table 6):

- For 64-pin packages, refer to Notes 6 and 7 in Table 3 and Table 4
- For 100-lead packages, refer to Notes 5 and 6 in Table 5 and Table 6.

21.1 Software I^2C Performance

Table 21-1 provides the performance details of the I^2C.

TABLE 21-1: I^2C PERFORMANCE

I^2C Baud Rate	I^2C Transactions/ Second	I^2C CPU Utilization
400 kHz	22070 (continuous)	50.76%
	16841	38.73%
	4079	9.38%
	429	0.99%
100 kHz	5581 (continuous)	12.84%
	4077	9.38%
	429	0.99%

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7840	ADCDATA36(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7850	ADCDATA37(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7860	ADCDATA38(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7870	ADCDATA39(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7880	ADCDATA40(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7890	ADCDATA41(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78D0	ADCDATA45(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78E0	ADCDATA46(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78F0	ADCDATA47(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7900	ADCDATA48	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7910	ADCDATA49	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7920	ADCDATA50(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7940	ADCDATA52(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7950	ADCDATA53(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7E00	ADCSYSCFG0	31:16	—	—	—	—	AN27	AN26	AN25	AN24	AN23(1)	AN22(1)	AN21(1)	AN20(1)	AN19	AN18	AN17	AN16	0FxF
		15:0	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	FFFF
7E10	ADCSYSCFG1	31:16	—	—	—	—	—	—	—	—	—	—	AN53(1)	AN52(1)	—	AN50(1)	AN49	AN48	00xx
		15:0	AN47(1)	AN46(1)	AN45(1)	—	—	—	AN41(1)	AN40(1)	AN39(1)	AN38(1)	AN37(1)	AN36(1)	AN35(1)	AN34(1)	AN33(1)	—	xxxx
7D00	ADC0CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 5-0 **ADINSEL<5:0>:** Analog Input Select bits

These bits select the analog input to be converted when the RQCNVRT bit is set.

111111 = Reserved
.
.
.
110110 = Reserved
110101 = CTMU Temperature Sensor (internal AN53)
110100 = VBAT/2 (internal AN52)
110011 = Reserved
110010 = IVREF 1.2V (internal AN50)
110001 = AN49
.
.
.
101101 = AN45
101100 = Reserved
.
.
.
101010 = Reserved
101001 = AN41
.
.
.
100001 = AN33
100000 = Reserved
.
.
.
011100 = Reserved
011011 = AN27
.
.
.
000000 = AN0

Note: AN20-AN23, AN33-AN41, and AN45-AN47 are not available on 64-pin devices. Refer to **TABLE 1-1: "ADC1 Pinout I/O Descriptions"** for details.

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 25-13: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	AIRDY27	AIRDY26	AIRDY25	AIRDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY23(1)	AIRDY22(1)	AIRDY21(1)	AIRDY20(1)	AIRDY19	AIRDY18	AIRDY17	AIRDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY15	AIRDY14	AIRDY13	AIRDY12	AIRDY11	AIRDY10	AIRDY9	AIRDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY7	AIRDY6	AIRDY5	AIRDY4	AIRDY3	AIRDY2	AIRDY1	AIRDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AIRDY27:AIRDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-14: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AIRDY53	AIRDY52	AIRDY51	AIRDY50	AIRDY49	AIRDY48
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	AIRDY47(1)	AIRDY46(1)	AIRDY45(1)	—	—	—	AIRDY41(1)	AIRDY40(1)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0
	AIRDY39(1)	AIRDY38(1)	AIRDY37(1)	AIRDY36(1)	AIRDY35(1)	AIRDY34(1)	AIRDY33(1)	—

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY53:AIRDY45:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

bit 12-10 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY41:AIRDY33:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-26: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 4) (CONTINUED)

bit 5 **DCMPED:** Digital Comparator 'x' "Output True" Event Status bit

The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI and IELOLO bits.

This bit is cleared by reading the AINID<5:0> bits (ADCCMPCONx<13:8>) or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator 'x' output true event has occurred (output of Comparator is '1')
0 = Digital Comparator 'x' output is false (output of Comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator 'x' Event bit

1 = Generate a digital comparator event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DCMPHI<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate an event

bit 1 **IELOHI:** Low/High Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 0 **IELOLO:** Low/Low Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPLO<15:0> bits
0 = Do not generate an event

Note 1: This setting is not available on 64-pin devices.

REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 must occur before Edge 2 can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current (i.e., 55 µA Typical(6))
10 = 10 times base current (i.e., 5.5 µA Typical(5))
01 = Base current level (i.e., 0.55 µA Typical(4))
00 = 1000 times base current (i.e., 550 µA Typical(4))

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1101' to select C1OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 36-43) in **Section 36.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

5: For CTMU temperature measurements on this range, ADC sampling time ≥ 1.6 µs.

6: For CTMU temperature measurements on this range, ADC sampling time ≥ 300 ns.

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A890	LEBDLY8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A8A0	AUXCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A8B0	PTMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A8C0	PWMCON9	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A8D0	IOCON9	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A8E0	PDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A8F0	SDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A900	PHASE9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A910	DTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
A920	ALTDTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
A930	DTCOMP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A940	TRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A950	TRGCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A960	STRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A970	CAP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A980	LEBCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A990	LEBDLY9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000

Legend: '—' = unimplemented; read as '0'.

REGISTER 33-5: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 25-21 **DSWDTPS<4:0>:** Deep Sleep Watchdog Timer Postscale Select bits
The DS WDT prescaler is 32; this creates an approximate base time unit of 1 ms.
11111 = 1:236 (25.7 days)
11110 = 1:235 (12.8 days)
11101 = 1:234 (6.4 days)
11100 = 1:233 (77.0 hours)
11011 = 1:232 (38.5 hours)
11010 = 1:231 (19.2 hours)
11001 = 1:230 (9.6 hours)
11000 = 1:229 (4.8 hours)
10111 = 1:228 (2.4 hours)
10110 = 1:227 (72.2 minutes)
10101 = 1:226 (36.1 minutes)
10100 = 1:225 (18.0 minutes)
10011 = 1:224 (9.0 minutes)
10010 = 1:223 (4.5 minutes)
10001 = 1:222 (135.3 s)
10000 = 1:221 (67.7 s)
01111 = 1:220 (33.825 s)
01110 = 1:219 (16.912 s)
01101 = 1:218 (8.456 s)
01100 = 1:217 (4.228 s)
01011 = 1:65536 (2.114 s)
01010 = 1:32768 (1.057 s)
01001 = 1:16384 (528.5 ms)
01000 = 1:8192 (264.3 ms)
00111 = 1:4096 (132.1 ms)
00110 = 1:2048 (66.1 ms)
00101 = 1:1024 (33 ms)
00100 = 1:512 (16.5 ms)
00011 = 1:256 (8.3 ms)
00010 = 1:128 (4.1 ms)
00001 = 1:64 (2.1 ms)
00000 = 1:32 (1 ms)

bit 20 **DSBOREN:** Deep Sleep Zero-Power BOR Enable bit
1 = Enable ZPBOR during deep sleep
0 = Disable ZPBOR during deep sleep

bit 19 **VBATBOREN:** VBAT Zero-Power BOR Enable bit
1 = Enable ZPBOR during VBAT mode
0 = Disable ZPBOR during VBAT mode

bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits
111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2

bit 15 **Reserved:** Write as ‘1’

35.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

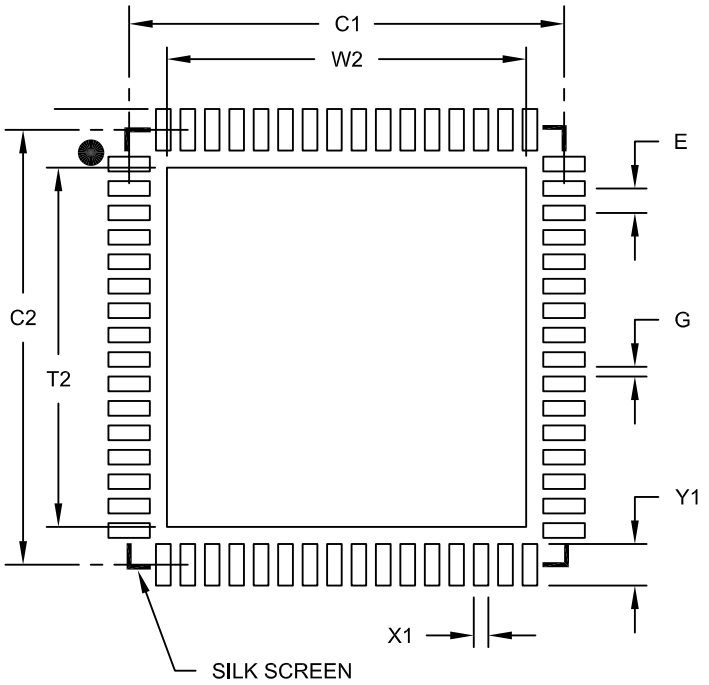
35.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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ISBN: 978-1-5224-2855-8