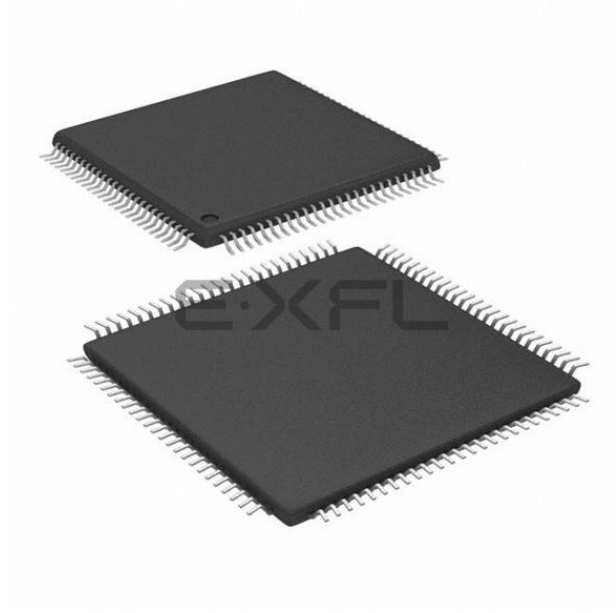
# Microchip Technology - PIC32MK0512GPE100T-I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, WDT |
| Number of I/O | 77 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 3.6V |
| Data Converters | A/D 42x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512gpe100t-i-pt |

**REGISTER 3-9: FEXR: FLOATING POINT EXCEPTIONS STATUS REGISTER; CP1 REGISTER 26**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x |
| | — | — | — | — | — | — | CAUSE<5:4> | |
| | | | | | | | E | V |
| 15:8 | R/W-x | R/W-x | R/W-x | U-0 | U-0 | U-0 | U-0 | U-0 |
| | CAUSE<3:0> | | | | — | — | — | — |
| | Z | O | U | I | | | | |
| 7:0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | U-0 | U-0 |
| | — | FLAGS<4:0> | | | | | — | — |
| | | V | Z | O | U | I | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-18 **Unimplemented:** Read as '0'

bit 17-12 **CAUSE<5:0>:** FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

bit 17 **E:** Unimplemented Operation bit

bit 16 **V:** Invalid Operation bit

bit 15 **Z:** Divide-by-Zero bit

bit 14 **O:** Overflow bit

bit 13 **U:** Underflow bit

bit 12 **I:** Inexact bit

bit 11-7 **Unimplemented:** Read as '0'

bit 6-2 **FLAGS<4:0>:** FPU Flags bits
These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.

bit 6 **V:** Invalid Operation bit

bit 4 **Z:** Divide-by-Zero bit

bit 4 **O:** Overflow bit

bit 3 **U:** Underflow bit

bit 2 **I:** Inexact bit

bit 1-0 **Unimplemented:** Read as '0'

**REGISTER 4-1: BFxSEQ: BOOT FLASH 'x' SEQUENCE REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | CSEQ<15:8> | | | | | | | |
| 23:16 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | CSEQ<7:0> | | | | | | | |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | TSEQ<15:8> | | | | | | | |
| 7:0 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | TSEQ<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

**TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0370 | IPC35 | 31:16 | — | — | — | AD1D37IP<2:0> | | | AD1D37IS<1:0> | | — | — | — | AD1D36IP<2:0> | | | AD1D36IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | AD1D35IP<2:0> | | | AD1D35IS<1:0> | | — | — | — | AD1D34IP<2:0> | | | AD1D34IS<1:0> | | 0000 |
| 0380 | IPC36 | 31:16 | — | — | — | AD1D41IP<2:0> | | | AD1D41IS<1:0> | | — | — | — | AD1D40IP<2:0> | | | AD1D40IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | AD1D39IP<2:0> | | | AD1D39IS<1:0> | | — | — | — | AD1D38IP<2:0> | | | AD1D38IS<1:0> | | 0000 |
| 0390 | IPC37 | 31:16 | — | — | — | AD1D45IP<2:0> | | | AD1D45IS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 03A0 | IPC38 | 31:16 | — | — | — | AD1D49IP<2:0> | | | AD1D49IS<1:0> | | — | — | — | AD1D48IP<2:0> | | | AD1D48IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | AD1D47IP<2:0> | | | AD1D47IS<1:0> | | — | — | — | AD1D46IP<2:0> | | | AD1D46IS<1:0> | | 0000 |
| 03B0 | IPC39 | 31:16 | — | — | — | AD1D53IP<2:0> | | | AD1D53IS<1:0> | | — | — | — | AD1D52IP<2:0> | | | AD1D52IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | AD1D51IP<2:0> | | | AD1D51IS<1:0> | | — | — | — | AD1D50IP<2:0> | | | AD1D50IS<1:0> | | 0000 |
| 03C0 | IPC40 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | CMP5IP<2:0> | | | CMP5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CMP4IP<2:0> | | | CMP4IS<1:0> | | — | — | — | CMP3IP<2:0> | | | CMP3IS<1:0> | | 0000 |
| 03D0 | IPC41 | 31:16 | — | — | — | CAN1IP<2:0>(3) | | | CAN1IS<1:0>(3) | | — | — | — | U6TXIP<2:0> | | | U6TXIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U6RXIP<2:0> | | | U6RXIS<1:0> | | — | — | — | U6EIP<2:0> | | | U6EIS<1:0> | | 0000 |
| 03E0 | IPC42 | 31:16 | — | — | — | PWMPEVTIP<2:0> | | | PWMSEVTIP<1:0> | | — | — | — | QEI2IP<2:0> | | | QEI2SIP<1:0> | | 0000 |
| | | 15:0 | — | — | — | QEI1IP<2:0> | | | QEI1SIP<1:0> | | — | — | — | CAN2IP<2:0>(3) | | | CAN2IS<1:0>(3) | | 0000 |
| 03F0 | IPC43 | 31:16 | — | — | — | PWM3IP<2:0> | | | PWM3SIP<1:0> | | — | — | — | PWM2IP<2:0> | | | PWM2SIP<1:0> | | 0000 |
| | | 15:0 | — | — | — | PWM1IP<2:0> | | | PWM1SIP<1:0> | | — | — | — | PWMSEVTIP<2:0> | | | PWMSEVTSIP<1:0> | | 0000 |
| 0400 | IPC44 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | PWM6IP<2:0> | | | PWM6SIP<1:0> | | 0000 |
| | | 15:0 | — | — | — | PWM5IP<2:0> | | | PWM5SIP<1:0> | | — | — | — | PWM4IP<2:0> | | | PWM4SIP<1:0> | | 0000 |
| 0410 | IPC45 | 31:16 | — | — | — | DMA5IP<2:0> | | | DMA5IS<1:0> | | — | — | — | DMA4IP<2:0> | | | DMA4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 0420 | IPC46 | 31:16 | — | — | — | CAN3IP<2:0>(3) | | | CAN3IS<1:0>(3) | | — | — | — | DATAEEIP<2:0> | | | DATAEEIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA7IP<2:0> | | | DMA7IS<1:0> | | — | — | — | DMA6IP<2:0> | | | DMA6IS<1:0> | | 0000 |
| 0430 | IPC47 | 31:16 | — | — | — | QEI5IP<2:0> | | | QEI5SIP<1:0> | | — | — | — | QEI4IP<2:0> | | | QEI4SIP<1:0> | | 0000 |
| | | 15:0 | — | — | — | QEI3IP<2:0> | | | QEI3SIP<1:0> | | — | — | — | CAN4IP<2:0>(3) | | | CAN4IS<1:0>(3) | | 0000 |
| 0440 | IPC48 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | QEI6IP<2:0> | | | QEI6SIP<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

**2:** This bit is not available on 64-pin devices.

**3:** This bit is not available on devices without a CAN module.

**4:** This bit is not available on 100-pin devices.

**5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

**6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

**7:** The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

**TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 063C | OFF063 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0640 | OFF064 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0644 | OFF065 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0648 | OFF066 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 064C | OFF067 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0650 | OFF068 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0654 | OFF069 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0658 | OFF070 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 065C | OFF071 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0660 | OFF072 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0664 | OFF073 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0668 | OFF074 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 066C | OFF075 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0670 | OFF076 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0674 | OFF077 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0678 | OFF078 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 067C | OFF079 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0680 | OFF080 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0684 | OFF081 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0688 | OFF082 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 068C | OFF083 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0690 | OFF084 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0694 | OFF085 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0698 | OFF086 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 069C | OFF087 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06A0 | OFF088 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06A4 | OFF089 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06A8 | OFF090 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**7:** The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

**REGISTER 12-9: UxEIE: USB ERROR INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE(1) / EOFEE(2) | PIDEE |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

**EOFEE:** EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

**Note 1:** Device mode.
**2:** Host mode.

**Note:** For an interrupt to propagate USBIF, the UERRIE bit (UxIE<1>) must be set.

**REGISTER 12-10: UxSTAT: USB STATUS REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | U-0 | U-0 |
| | ENDPT<3:0> | | | | DIR | PPBI | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)

1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last BD Direction Indicator bit

1 = Last transaction was a transmit transfer (TX)
0 = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit

1 = The last transaction was to the ODD BD bank
0 = The last transaction was to the EVEN BD bank

bit 1-0 **Unimplemented:** Read as '0'

**Note:** The UxSTAT register is a window into a 4-byte FIFO maintained by the USB module. UxSTAT value is only valid when the TRNIF bit (UxIR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

**REGISTER 12-16: UxSOF: USB SOF THRESHOLD REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

**REGISTER 12-17: UxBDTP1: USB BDT PAGE 1 REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | BDTPTRL<15:9> | | | | | | | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

**TABLE 13-1: INPUT PIN SELECTION (CONTINUED)**

| Peripheral Pin | [*pin name*]R SFR | [*pin name*]R bits | [*pin name*]R Value to RPn Pin Selection |
|---|---|---|---|
| INT3 | INT3R<3:0> | INT3R | 0000 = RPA1 |
| T3CK | T3CKR<3:0> | T3CKR | 0001 = RPB5 |
| T7CK | T7CKR<3:0> | T7CKR | 0010 = RPB1 |
| IC3 | IC3R<3:0> | IC3R | 0011 = RPB11 |
| IC8 | IC8R<3:0> | IC8R | 0100 = RPB8 |
| IC11 | IC11R<3:0> | IC11R | 0101 = RPA8 |
| IC16 | IC16R<3:0> | IC16R | 0110 = RPC8 |
| $\overline{\text{U1CTS}}$ | U1CTSR<3:0> | U1CTSR | 0111 = RPB12 |
| U2RX | U2RXR<3:0> | U2RXR | 1000 = RPA12 |
| $\overline{\text{U5CTS}}$ | U5CTSR<3:0> | U5CTSR | 1001 = RPD6 |
| SDI2 | SDI2R<3:0> | SDI2R | 1010 = RPG7 |
| SDI4 | SDI4R<3:0> | SDI4R | 1011 = RPG0(1) |
| SCK6 | SCK6R<3:0> | SCK6R | 1100 = RPE1(1) |
| QEB1 | QEB1R<3:0> | QEB1R | 1101 = RPA14(1) |
| INDX2 | INDX2R<3:0> | INDX2R | 1110 = Reserved |
| QEB3 | QEB3R<3:0> | QEB3R | 1111 = Reserved |
| INDX4 | INDX4R<3:0> | INDX4R | |
| QEB5 | QEB5R<3:0> | QEB5R | |
| INDX6 | INDX6R<3:0> | INDX6R | |
| C2RX | C2RXR<3:0> | C2RXR | |
| FLT2 | FLT2R<3:0> | FLT2R | |

**Note 1:** This selection is not available on 64-pin devices.

**REGISTER 24-5: ALRMTIME: ALARM TIME VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | HR10<3:0> | | | | HR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MIN10<3:0> | | | | MIN01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SEC10<3:0> | | | | SEC01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 25-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)**

bit 5 **DIFF2:** AN2 Mode bit
1 = Selects AN2 differential input pair as AN2+ and AN8-
0 = AN2 is using Single-ended mode

bit 4 **SIGN2:** AN2 Signed Data Mode bit
1 = AN2 is using Signed Data mode
0 = AN2 is using Unsigned Data mode

bit 3 **DIFF1:** AN1 Mode bit
1 = Selects AN1 differential input pair as AN1+ and AN7-
0 = AN1 is using Single-ended mode

bit 2 **SIGN1:** AN1 Signed Data Mode bit
1 = AN1 is using Signed Data mode
0 = AN1 is using Unsigned Data mode

bit 1 **DIFF0:** AN0 Mode bit
1 = Selects AN0 differential input pair as AN0+ and AN6-
0 = AN0 is using Single-ended mode

bit 0 **SIGN0:** AN0 Signed Data Mode bit
1 = AN0 is using Signed Data mode
0 = AN0 is using Unsigned Data mode

**REGISTER 25-36: ADCEISTAT1: ADC EARLY INTERRUPT STATUS REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | — | — | — | — | EIRDY27 | EIRDY26 | EIRDY25 | EIRDY24 |
| 23:16 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | EIRDY23(1) | EIRDY22(1) | EIRDY21(1) | EIRDY20(1) | EIRDY19 | EIRDY18 | EIRDY17 | EIRDY16 |
| 15:8 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | EIRDY15 | EIRDY14 | EIRDY13 | EIRDY12 | EIRDY11 | EIRDY10 | EIRDY9 | EIRDY8 |
| 7:0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | EIRDY7 | EIRDY6 | EIRDY5 | EIRDY4 | EIRDY3 | EIRDY2 | EIRDY1 | EIRDY0 |

| Legend: | HS = Hardware Set | HC = Cleared by hardware | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **EIRDY27:EIRDY0:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN1 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

**Note 1:** This bit is not available on 64-pin devices.

**TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)**

| Virtual Address (BF82_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| BAB0 | QEI5ICC | 31:16 | QEIICC<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | QEIICC<15:0> | | | | | | | | | | | | | | | | 0000 |
| BAC0 | QEI5CMPL | 31:16 | QEICMPL<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | QEICMPL<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC00 | QEI6CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | QEIEN | — | QEISIDL | PIMOD<2:0> | | | IMV<1:0> | | — | INTDIV<2:0> | | | CNTPOL | GATEN | CCM<1:0> | | 0000 |
| BC10 | QEI6IOC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | HCAPEN | 0000 |
| | | 15:0 | QCAPEN | FLTREN | QFDIV<2:0> | | | OUTFNC<1:0> | | SWPAB | HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA | 0000 |
| BC20 | QE6STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | PCHEQIRQ | PCHEQIEN | PCLEQIRQ | PCLEQIEN | POSOVIRQ | POSOVIEN | PCIIRQ | PCIIEN | VELOVIRQ | VELOVIEN | HOMIRQ | HOMIEN | IDXIRQ | IDXIEN | 0000 |
| BC30 | POS6CNT | 31:16 | POSCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | POSCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC40 | POS6HLD | 31:16 | POSHLD<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | POSHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC50 | VEL6CNT | 31:16 | VELCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | VELCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC60 | VEL6HLD | 31:16 | VELHLD<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | VELHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC70 | INT6TMR | 31:16 | INTTMR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | INTTMR<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC80 | INT6HLD | 31:16 | INTHLD<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | INTHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| BC90 | INDX6CNT | 31:16 | INDXCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | INDXCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| BCA0 | INDX6HLD | 31:16 | INDXHLD<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | INDXHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| BCB0 | QEI6ICC | 31:16 | QEIICC<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | QEIICC<15:0> | | | | | | | | | | | | | | | | 0000 |
| BCC0 | QEI6CMPL | 31:16 | QEICMPL<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | QEICMPL<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

**TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)**

| Virtual Address (BF82_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| A9A0 | AUXCON9 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |
| A9B0 | PTMR9 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR<15:0> | | | | | | | | | | | | | | | | 0000 |
| A9C0 | PWMCON10 | 31:16 | FLTIF | CLIF | TRGIF | PWMLIF | PWMHIF | — | — | — | FLTIEN | CLIEN | TRGIEN | PWMLIEN | PWMHIEN | — | — | — | 0000 |
| | | 15:0 | FLTSTAT | CLTSTAT | — | — | ECAM<1:0> | | ITB | — | DTC<1:0> | | DTCP | PTDIR | MTBS | — | XPRES | — | 0000 |
| A9D0 | IOCON10 | 31:16 | — | — | CLSRC<3:0> | | | | CLPOL | CLMOD | — | FLTSRC<3:0> | | | | FLTPOL | FLTMOD<1:0> | | 0078 |
| | | 15:0 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| A9E0 | PDC10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PDC<15:0> | | | | | | | | | | | | | | | | 0000 |
| A9F0 | SDC10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SDC<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA00 | PHASE10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PHASE<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA10 | DTR10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | DTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA20 | ALTDTR10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ALTDTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA30 | DTCOMP10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | COMP<13:0> | | | | | | | | | | | | | | 0000 |
| AA40 | TRIG10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA50 | TRGCON10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRGDIV<3:0> | | | | TRGSEL<1:0> | | STRGSEL<1:0> | | DTM | STRGIS | — | — | — | — | — | — | 0000 |
| AA60 | STRIG10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | STRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA70 | CAP10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CAP<15:0> | | | | | | | | | | | | | | | | 0000 |
| AA80 | LEBCON10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | — | — | — | — | — | — | 0000 |
| AA90 | LEBDLY10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AAA0 | AUXCON10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** '—' = unimplemented; read as '0'.

**REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)**

bit 0 **OSYNC:** Output Override Synchronization bit

1 = Output overrides through the OVRDAT<1:0> bits are synchronized to the PWM time base

0 = Output overrides through the OVRDAT<1:0> bits occur on next CPU clock boundary

**Note 1:** During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

**2:** These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

**3:** State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

**4:** If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

**Note:** Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

**Desirable Example PWM1:** (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

**Undesirable Example: PWM1:** (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

**REGISTER 31-18: DTCOMPx: DEAD TIME COMPENSATION REGISTER 'x' ('x' = 1 THROUGH 12)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | COMP<13:8>(1,2) | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | COMP<7:0>(1,2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **COMP<13:0>:** Dead Time Compensation Value bits(1,2)

Dead time compensation value if Dead Time compensation mode is enabled.

**Note 1:** COMP<13:0> Min LSb = 1 / FSYSCLK for ECAM<1:0> bits (PWMCONx<11:10>) = '0b00 Edge-Aligned mode; COMP<13:0> Min LSb = 2 / FSYSCLK for ECAM<1:0> bits (PWMCONx<11:10>)> '0b00 Center-Aligned mode.

**2:** When Dead Time compensation mode is selected through the DTC<1:0> bits in the PWMCONx register, an external pin, CMPx (i.e., FLTx) connected to the Dead Time Compensation module input signals, cause the value in the COMPx register to be added to or subtracted from the PWMx duty cycle. The dead time compensation input signals are sampled at the end of a PWM cycle for use in the next PWM cycle. The modification of the duty cycle duration through the CMPx registers occurs during the end (trailing edge) of the duty cycle. Dead time compensation is available only for Positive Dead Time mode. The CMPx value must be less than one-half the value of the duty cycle register, PDCx; otherwise, unpredictable behavior will result. Dead time compensation will not apply for a duty cycle of zero. In this case, the PWM output will remain zero regardless of the state of the CMPx input pin.

**REGISTER 32-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER(3)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS |
| | — | — | — | — | — | — | — | DSINT0 |
| 7:0 | R/W-0, HS | U-0 | U-0 | R/W-0, HS | R/W-0, HS | R/W-0, HS | U-0 | U-0 |
| | DSFLT | — | — | DSWDT | DSRTC | DSMCLR | — | — |

| **Legend:** | | HS = Hardware Set | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit
1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

**2:** To ensure a successful write, this register must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

**3:** After waking from deep sleep, writes to the DSWAKE register are ignored until the RELEASE bit (DSCON<0>) is cleared.

**REGISTER 33-7: CFGCON: CONFIGURATION CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | r-0 | U-0 |
| | — | — | — | — | — | ADCPRI(1) | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PWMAPIN6 | PWMAPIN5 | PWMAPIN4 | PWMAPIN3 | PWMAPIN2 | PWMAPIN1 | ICACLK(1) | OCACLK(1) |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | r-0 | r-0 | U-0 |
| | — | — | IOLOCK(1) | PMDLOCK(1) | PGLOCK(1) | — | — | — |
| 7:0 | R/W-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | U-0 | R/W-1 |
| | IOANCPEN(1) | — | — | — | JTAGEN | TROEN | — | TDOEN |

| Legend: | r = Reserved bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **ADCPRI:** ADC Arbitration Priority to SRAM bit(1)
- 1 = ADC gets High Priority access to SRAM
- 0 = ADC uses Least Recently Serviced Arbitration (same as other initiators)

bit 25 **Reserved:** Write as '0'

bit 24 **Unimplemented:** Read as '0'

bit 23-18 **PWMAPIN6:PWMAPIN1:** PWM Alternate I/O Pin Selection bit
- 1 = PWMxL ('x' = 1-6) functionality is replaced by PWMxH(x+6) functionality. Provides independent PWMH and PWML functionality. If PWMAPING5 or PWMAPING6 = 1, the dedicated PWM output pin functions, PWMH11 and PWMH12, respectively, will be disabled and rerouted to PWML5 and PWML6.
- 0 = PWMxL functionality remains on pins. Provides complimentary PWMH and PWML functionality.

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit(1)
- 1 = Input Capture modules use an alternative Timer pair as their timebase clock
- 0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit(1)
- 1 = Output Compare modules use an alternative Timer pair as their timebase clock
- 0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers are not allowed
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers are allowed

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers are not allowed
- 0 = Peripheral module is not locked. Writes to PMD registers are allowed

bit 11 **PGLOCK:** Permission Group Lock bit(1)
- 1 = Permission Group registers are locked. Writes to PG registers are not allowed
- 0 = Permission Group registers are not locked. Writes to PG registers are allowed

bit 10-9 **Reserved:** Write as '0'

bit 8 **Unimplemented:** Read as '0'

**Note 1:** To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

## Revision D (March 2017)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

In addition, minor updates to text and formatting were incorporated throughout the document.

**TABLE A-2: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps"** | page 1 - Updates in **"Power Management" "Motor Control PWM" "Motor Encoder Interface" "Audio/Graphics/Touch Interfaces" "Unique Features" "Advanced Analog Features" "Communication Interfaces" "Qualification and Class B Support"**<br>Removed VBAT column in Table 1.<br>Added Note 8 in Table 3.<br>Added Note 7 in Table 5. |
| **1.0 "Device Overview"** | Added Note 1 in Table 1-20. |
| **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** | Added Note 1 to Register 25-4. |
| **31.0 "Motor Control PWM Module"** | Updated first page bulleted list to "Nine Fault input pins are available for Faults and current limits."<br>Updated pin table in Figure 31-1.<br>Updated **31.1.2 "WRITE-PROTECTED REGISTERS"**<br>Updated label TMRx to PTMRx in Figure 31-2.<br>Updated "All Resets" value from 0000 to 0078 for IOCONx<31:16> registers in Table 31-1.<br>Updated bit 15-0 descriptions in Register 31-6.and Register 31-10<br>Updated note in Register 31-10.<br>Updated bit 11-10 description in Register 31-11.<br>Updated Notes 1 and 4 in Register 31-12.<br>Updated Note 1 and added note markers in DTCOMP<13:8> and DTCOMP<7:0> in Register 31-18. |
| **36.0 "Electrical Characteristics"** | Updated parameter DI20 Min. VDD value in Table 36-9.<br>Updated parameter OS13 Max. MHz value in Table 36-15.<br>Updated Note 2 equation value from PBCLK2 to PBCLKx in Table 36-16.<br>Updated Table 36-28 to include parameter OA14.<br>Updated Min. ADC Clock Period for parameter AD50 in Table 36-39.<br>Updated Max. Sample Throughput Rates for parameter AD51 in Table 36-39.<br>Updated Table 36-42 to include parameter CTMU0. |

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