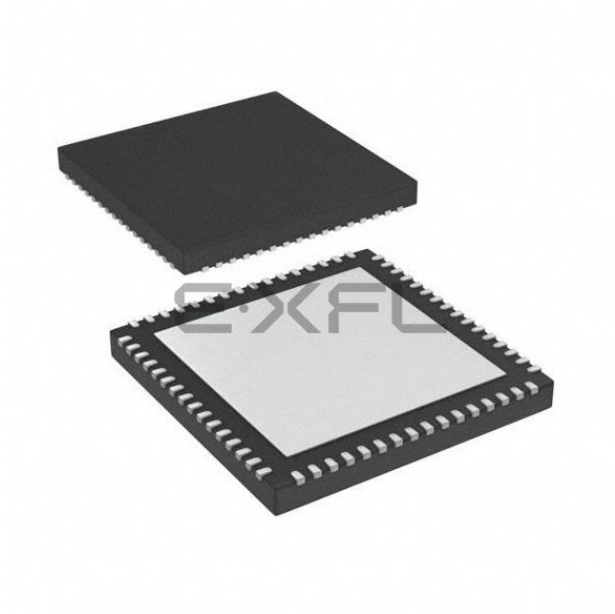
Microchip Technology - PIC32MK0512MCF064-E/MR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 27x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512mcf064-e-mr

TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 9-5: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-4)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)
1111 = Reserved
•
•
•
1001 = Reserved
1000 = REFCLKI
0111 = SPLL
0110 = UPLL
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = PBCLK1
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 12-3: UxOTGSTAT: USB OTG STATUS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
- 1 = No cable is attached or a Type-B cable has been plugged into the USB receptacle
- 0 = A Type-A cable has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
- 1 = USB line state (SE0 (UxCON<6>) and JSTATE (UxCON<7>)) has been stable for the previous 1 ms
- 0 = USB line state (SE0 and JSTATE) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A or B device
- 0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit
- 1 = VBUS voltage is below Session Valid on the B device
- 0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A device
- 0 = VBUS voltage is below Session Valid on the A device

REGISTER 12-8: UxEIR: USB ERROR INTERRUPT STATUS REGISTER ('x' = 1 AND 2)

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
- 1 = Token packet rejected due to CRC5 error
- 0 = Token packet accepted

EOFEF: EOF Error Flag bit(3,5)
- 1 = EOF error condition detected
- 0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit
- 1 = PID check failed
- 0 = PID check passed

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

TABLE 13-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA1	RPA1R	RPA1R<4:0>	00000 = Off 00001 = U3RTS 00010 = U4TX 00011 = SDO1 00100 = SDO2 00101 = OC2 00110 = OC8 00111 = C3OUT 01000 = OC9 01001 = OC12 01010 = OC16 01011 = U6RTS 01100 = C4TX 01101 = Reserved 01110 = SDO3 01111 = SDO4 10000 = SDO5 10001 = SCK6 10010 = REFCLKO3 10011 = Reserved 10100 = QEICMP2 10101 = QEICMP6 10110 = Reserved . . . 11111 = Reserved
RPB5	RPB5R	RPB5R<4:0>	
RPB1	RPB1R	RPB1R<4:0>	
RPB11	RPB11R	RPB11R<4:0>	
RPA8	RPA8R	RPA8R<4:0>	
RPC8	RPC8R	RPC8R<4:0>	
RPB12	RPB12R	RPB12R<4:0>	
RPA12	RPA12R	RPA12R<4:0>	
RPD6	RPD6R	RPD6R<4:0>	
RPG7	RPG7R	RPG7R<4:0>	
RPG0(1)	RPG0R(1)	RPG0R<4:0> (1)	
RPE1(1)	RPE1R(1)	RPE1R<4:0> (1)	
RPA14(1)	RPA14R(1)	RPA14R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-6: PORTC REGISTER MAP FOR 64-PIN AND 100-PIN DEVICES

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ANSC12	ANSC11	ANSC10	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	1007
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	TRISC11	TRISC10	TRIS92	TRISC8	TRISC7	TRISC6	—	—	—	TRISC2	TRISC1	TRISC0	FFC7
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	—	—	—	RC2	RC1	RC0	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	—	—	—	LATC2	LATC1	LATC0	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	—	—	—	ODCC2	ODCC1	ODCC0	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	—	—	—	CNPUC2	CNPUC1	CNPUC0	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	—	—	—	CNPDC2	CNPDC1	CNPDC0	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC7	—	—	—	CNIEC2	CNIEC1	CNIEC0	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATC15	CN STATC14	CN STATC13	CN STATC12	CN STATC11	CN STATC10	CN STATC9	CN STATC8	CN STATC7	CN STATC6	—	—	—	CN STATC2	CN STATC1	CN STATC0	0000
02A0	CNNEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	CNNEC11	CNNEC10	CNNEC9	CNNEC8	CNNEC7	CNNEC6	—	—	—	CNNEC2	CNNEC1	CNNEC0	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	CNFC11	CNFC10	CNFC9	CNFC8	CNFC7	CNFC6	—	—	—	CNFC2	CNFC1	CNFC0	0000
02C0	SRCON0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0C15	—	—	—	SR0C11	—	SR0C9	SR0C8	SR0C7	SR0C6	—	—	—	—	—	—	0000
02D0	SRCON1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1C15	—	—	—	SR1C11	—	SR1C9	SR1C8	SR1C7	SR1C6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

NOTES:

16.0 DEADMAN TIMER (DMT)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

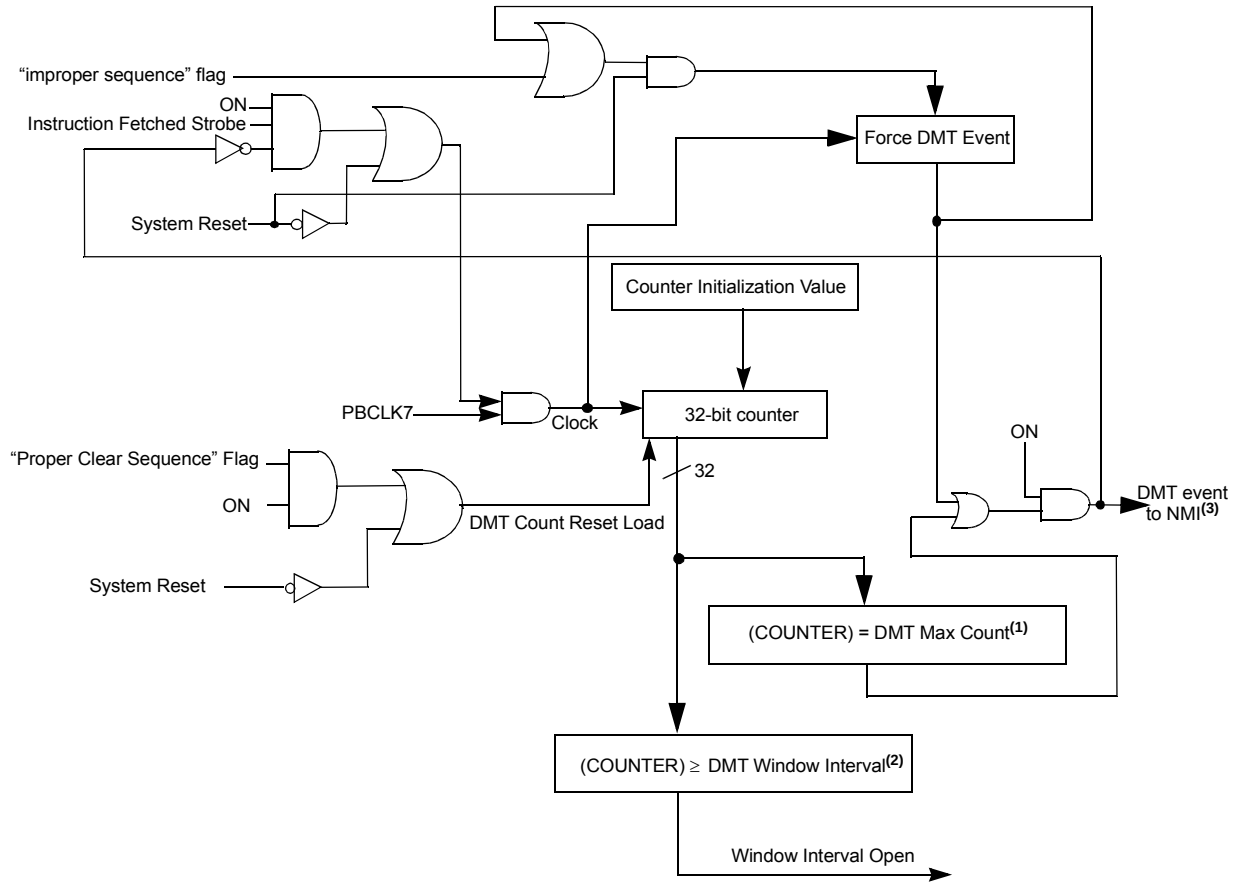
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

The DMT consists of a 32-bit counter with a time-out count match value as specified by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.

A Deadman Timer is typically used in mission critical and safety critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 16-1 shows a block diagram of the Deadman Timer module.

FIGURE 16-1: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.
2: DMT Window Interval is controlled by the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.
3: Refer to **7.0 "Resets"** for more information.

REGISTER 16-1: DMTCON: DEADMAN TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Deadman Timer Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is disabled

bit 13-0 **Unimplemented:** Read as '0'

Note 1: This bit only has control when the FDMTEN bit (DEVCFG1<3>) = 0.

REGISTER 16-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP1<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STEP1<7:0>:** Preclear Enable bits
01000000 = Enables the Deadman Timer Preclear (Step 1)
All other write patterns = Set BAD1 flag.
These bits are cleared when a DMT reset event occurs. STEP1<7:0> is also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 22-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits(2)
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
1 = Wake-up is enabled
0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: These bits can be changed only when the ON bit (UxMODE<15>) is set to '0'.
2: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
73E0	ADCEISTAT1	31:16	—	—	—	—	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23(1)	EIRDY22(1)	EIRDY21(1)	EIRDY20(1)	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
73F0	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	EIRDY53	EIRDY52	—	EIRDY50	EIRDY49	EIRDY48	0000
		15:0	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIRDY41(1)	EIRDY40(1)	EIRDY39(1)	EIRDY38(1)	EIRDY37(1)	EIRDY36(1)	EIRDY35(1)	EIRDY34(1)	EIRDY33(1)	—	0000
7400	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	WKIEN5	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	WKRDY5	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	ANEN5	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
7600	ADCDATA0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7610	ADCDATA1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7620	ADCDATA2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7630	ADCDATA3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7640	ADCDATA4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7650	ADCDATA5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7660	ADCDATA6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7670	ADCDATA7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7680	ADCDATA8	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7690	ADCDATA9	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76A0	ADCDATA10	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76B0	ADCDATA11	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76C0	ADCDATA12	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76D0	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., V_{BAT}, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-24: ADCTRG7: ADC TRIGGER SOURCE 7 REGISTER

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC26<4:0>:** Trigger Source for Conversion of Analog Input AN26 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC25<4:0>:** Trigger Source for Conversion of Analog Input AN25 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC24<4:0>:** Trigger Source for Conversion of Analog Input AN24 Select bits
See bits 28-24 for bit value definitions.

Note:	This register is not available on 64-pin devices.

REGISTER 25-25: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

bit 13-8 **AINID<5:0>:** Digital Comparator 1 Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by Digital Comparator 1.

In normal ADC mode, only analog inputs <31:0> can be processed by the Digital Comparator 1. The Digital Comparator 1 also supports the CVD mode, in which all Class 2 and Class 3 analog inputs may be stored in the AINID<5:0> bits.

111111 = Reserved
•
•
•
110110 = Reserved
110101 = Internal AN53 (CTMU temperature sensor)
110101 = Internal AN52 (V_{BAT}/2)
110101 = Reserved
110010 = Internal AN50 (IV_{REF} 1.2V)
110001 = AN49 is being monitored
•
•
•
101101 = AN45 is being monitored
101100 = Reserved
•
•
•
101010 = Reserved
101001 = AN41 is being monitored
•
•
•
100001 = AN33 is being monitored
111100 = Reserved
•
•
•
111000 = Reserved
111011 = AN27 is being monitored
•
•
•
000000 = AN0 is being monitored

Note: For 64-pin devices AN20-AN23 and AN33-AN47 inputs are not implemented.

bit 7 **ENDCMP:** Digital Comparator 1 Enable bit
1 = Digital Comparator 1 is enabled
0 = Digital Comparator 1 is not enabled, and the DCMPED status bit (ADCCMP0CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator 1 Global Interrupt Enable bit
1 = A Digital Comparator 1 interrupt is generated when the DCMPED status bit (ADCCMP0CON<5>) is set
0 = A Digital Comparator 1 interrupt is disabled

bit 5 **DCMPED:** Digital Comparator 1 "Output True" Event Status bit
The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI, and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator 1 output true event has occurred (output of Comparator is '1')
0 = Digital Comparator 1 output is false (output of comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator 1 Event bit
1 = Generate a digital comparator event when DCMPLO<15:0> ≤ DATA<31:0> < DCMPHI<15:0>
0 = Do not generate a digital comparator event

REGISTER 25-31: ADCDATAx: ADC OUTPUT DATA REGISTER 'x' ('x' = 0-27, 33-41, AND 45-53)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: The registers, ADCDATA23-20,ADCDATA41-33, and ADCDATA45-47, are not available on 64-pin devices.

2: The registers, ADCDATA32-28 and ADCDATA44-42, are not available on 64-pin and 100-pin devices.

3: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

4: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

REGISTER 30-4: POSxCNT: POSITION COUNTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **POSCNT<31:0>:** 32-bit Position Counter Register bits

The Operating mode of the position counter is controlled by the CCM bit in the QEIxCON register.

Quadrature Count mode: The QEA and QEB inputs are decoded to generate count pulses and direction information for controlling the position counter operation.

External Count with External Up/Down mode: The QEA/EXTCNT input is treated as an external count signal, and the QEB/DIR/GATE input provides the count direction information.

External Count with External Gate mode: The QEA/EXTCNT input is treated as an external count signal. If the GATEN bit in the QEIxCON register is equal to '1', the QEB/DIR/GATE input will gate the counter signal.

Internal Timer mode: The position counter uses PBCLK2 divided by the clock divider INTDIV as the count source.

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A780	LEBCON7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A790	LEBDLY7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A7A0	AUXCON7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A7B0	PTMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A7C0	PWMCON8	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A7D0	IOCON8	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A7E0	PDC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A7F0	SDC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A800	PHASE8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A810	DTR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
A820	ALTDTR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
A830	DTCOMP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A840	TRIG8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A850	TRGCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A860	STRIG8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A870	CAP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A880	LEBCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000

Legend: '—' = unimplemented; read as '0'.

35.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

35.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

TABLE 36-40: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

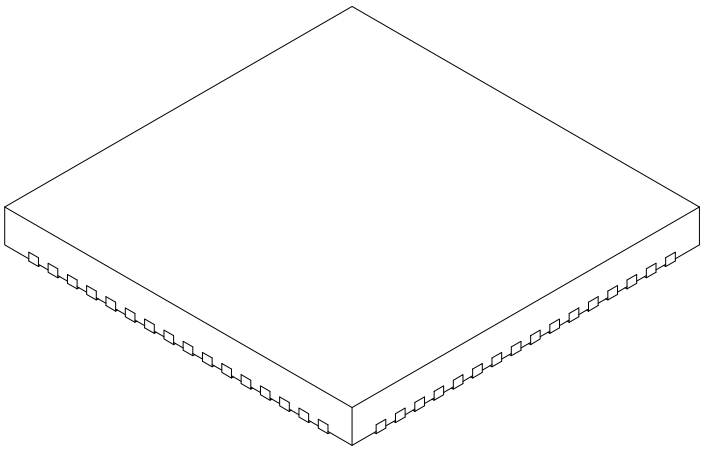
AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	16.667	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC5 (Class 1 Inputs)	— — — —	— — — —	3.75 4.284 4.992 6	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	3.53 4.00 4.615 5.45	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC5 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	See Table 36-41	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD µs	Lesser of 500 TAD or 20 µs

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2