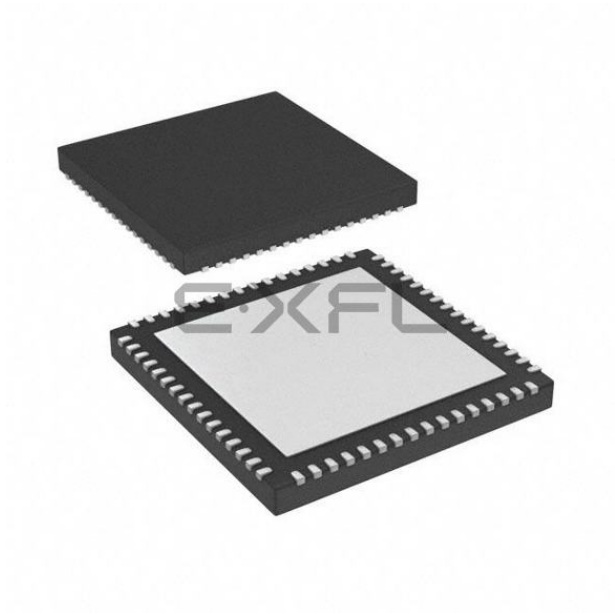
Microchip Technology - PIC32MK0512MCF064T-E/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 27x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512mcf064t-e-mr

TABLE 1-14: USB1 AND USB2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
VUSB3V3	55	35	P	—	USB internal transceiver supply. This pin should be connected to VDD.
VBUS1	54	34	I	Analog	USB1 Bus Power Monitor
VBUSON1	4	2	O	CMOS	USB1 VBUS Power Control Output
VBUSON2	10	—	O	CMOS	USB2 VBUS Power Control Output
D1+	57	37	I/O	Analog	USB1 D+
D1-	56	36	I/O	Analog	USB1 D-
USBID1	69	43	I	ST	USB1 OTG ID Detect
VBUS2	58	—	I	Analog	USB2 Bus Power Monitor
D2+	60	—	I/O	Analog	USB2 D+
D2-	59	—	I/O	Analog	USB2 D-
USBID2	77	—	I	ST	USB2 OTG ID detect

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-15: CTMU PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CTED1	25	16	I	ST	CTMU External Edge Input 1
CTED2	24	15	I	ST	CTMU External Edge Input 2
CTCMP	27	18	I	Analog	CTMU external capacitor input for pulse generation
CTPLS	PPS	PPS	O	CMOS	CTMU Pulse Generator Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-16: CDAC1 THROUGH CDAC3 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CDAC1	51	33	O	Analog	12-bit CDAC1 output
CDAC2	71	45	O	Analog	12-bit CDAC2 output
CDAC3	49	31	O	Analog	12-bit CDAC3 output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

The MIPS architecture defines that the result of a multiply or divide operation be placed in one of four pairs of HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

The MDU also implements various shift instructions operating on the HI/LO register and multiply instructions as defined in the DSP ASE. The MDU supports all of the data types required for this purpose and includes three extra HI/LO registers as defined by the ASE.

Table 3-2 lists the latencies and repeat rates for the DSP multiply and dot-product operations. The approximate latencies and repeat rates are listed in terms of pipeline clocks.

TABLE 3-2: DSP-RELATED LATENCIES AND REPEAT RATES

Op code	Latency	Repeat Rate
Multiply and dot-product without saturation after accumulation	5	1
Multiply and dot-product with saturation after accumulation	5	1
Multiply without accumulation	5	1

3.1.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as the presence of options like microMIPS is also available by accessing the CP0 registers, listed in Table 3-3.

TABLE 3-3: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MK GP Family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-privileged mode.
8	BadVAddr	Reports the address for the most recent address-related exception.
	BadInstr	Reports the instruction that caused the most recent exception.
	BadInstrP	Reports the branch instruction if a delay slot caused the most recent exception.
9	Count	Processor cycle count.
10	Reserved	Reserved in the PIC32MK GP Family core.
11	Compare	Core timer interrupt control.
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

bit 2-0 **K0<2:0>:** Kseg0 Coherency Algorithm bits
000 = Reserved
001 = Reserved
010 = Instruction Prefetch uncached (Default)
011 = Instruction Prefetch cached (Recommended)
100 = Reserved
•
•
•
111 = Reserved

REGISTER 3-11: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

bit 17 **E:** Unimplemented Operation bit

bit 16 **V:** Invalid Operation bit

bit 15 **Z:** Divide-by-Zero bit

bit 14 **O:** Overflow bit

bit 13 **U:** Underflow bit

bit 12 **I:** Inexact bit

bit 11-7 **ENABLES<4:0>:** FPU Exception Enable bits
These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.

bit 11 **V:** Invalid Operation bit

bit 10 **Z:** Divide-by-Zero bit

bit 9 **O:** Overflow bit

bit 8 **U:** Underflow bit

bit 7 **I:** Inexact bit

bit 6-2 **FLAGS<4:0>:** FPU Flags bits
These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.

bit 6 **V:** Invalid Operation bit

bit 5 **Z:** Divide-by-Zero bit

bit 4 **O:** Overflow bit

bit 3 **U:** Underflow bit

bit 2 **I:** Inexact bit

bit 1-0 **RM<1:0>:** Rounding Mode control bits
11 = Round towards Minus Infinity ($-\infty$)
10 = Round towards Plus Infinity ($+\infty$)
01 = Round toward Zero (0)
00 = Round to Nearest

REGISTER 7-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, HS	R/W-0, HS	U-0	U-0	U-0	U-0	U-0	U-0
	PORIO	PORCORE	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1, HS	R/W-1, HS
	—	—	—	—	—	—	VBPOR	VBAT
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
	—	—	—	—	—	DPSLP(1)	CMR	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR(2)	POR(2)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PORIO:** I/O Voltage POR Flag bit
1 = A Power-up Reset has occurred due to I/O Voltage
0 = A Power-up Reset has not occurred due to I/O Voltage

Note: Set by hardware at detection of an I/O POR event. User software must clear this bit to view the next detection; however, writing a '1' to this bit does not cause a PORIO.

bit 30 **PORCORE:** Core Voltage POR Flag bit
1 = A Power-up Reset has occurred due to Core Voltage
0 = A Power-up Reset has not occurred due to Core Voltage

Note: Set by hardware at detection of a Core POR event. User software must clear this bit to view the next detection; however, writing a '1' to this bit does not cause a PORCORE.

bit 29-18 **Unimplemented:** Read as '0'

bit 17 **VBPOR:** VBPOR Mode Flag bit
1 = A VBAT domain POR has occurred
0 = A VBAT domain POR has not occurred

bit 16 **VBAT:** VBAT Mode Flag bit
1 = A POR exit from VBAT has occurred (a true POR must be established with the valid VBAT voltage on the VBAT pin)
0 = A POR exit from VBAT has not occurred

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Deep Sleep Mode Flag bit(1)
1 = Deep Sleep mode has occurred
0 = Deep Sleep mode has not occurred

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

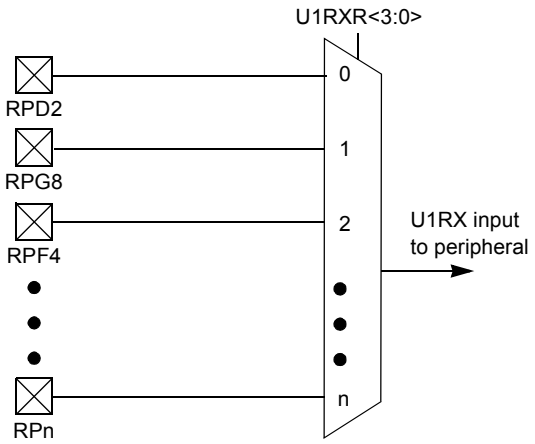
bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

Note 1: User software must clear this bit to view the next detection.

FIGURE 13-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

16.1 Deadman Timer Control Registers

TABLE 16-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0E00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0E10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0E20	DMCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0E30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0E40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0E60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	0000
0E70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

22.1 UART Control Registers

TABLE 22-1: UART1 AND UART2 REGISTER MAP

Virtual Address BF82_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8000	U1MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8010	U1STA(1)	31:16	ADDRMSK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8040	U1BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	U1BRG<19:16>				0000
		15:0	U1BRG<15:0>																0000
8200	U2MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8210	U2STA(1)	31:16	ADDRMSK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8240	U2BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BRG<19:16>				0000
		15:0	BRG<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 23-9: PMRADDR: PARALLEL PORT READ ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2a	CS1a	RADDR<21:16>					
	RADDR23	RADDR22						
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RCS2	RCS1	RADDR<13:8>					
	RADDR15	RADDR14						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CS2a:** Chip Select 2a bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2a is active
0 =Chip Select 2a is inactive

bit 23 **RADDR<23>:** Target Address bit 23
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 1.

bit 22 **CS1a:** Chip Select 1a bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1a is active
0 = Chip Select 1a is inactive

bit 22 **RADDR<22>:** Target Address bit 22
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 1.

bit 21-16 **RADDR<21:16>:** Address bits
This bit is only valid when the EXADR bit = 1 and the DUALBUF bit = 1.

bit 15 **RCS2:** Chip Select 2 bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive (RADDR15 function is selected)

bit 15 **RADDR<15>:** Target Address bit 15
This bit is only valid when the CSF<1:0> bits = 00.

bit 14 **RCS1:** Chip Select 1 bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive (RADDR14 function is selected)

bit 14 **RADDR<14>:** Target Address bit 14
This bit is only valid when the CSF<1:0> bits = 00 or 01.

bit 13-0 **RADDR<13:0>:** Address bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

25.2 ADC Control Registers

TABLE 25-2: ADC REGISTER MAP

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>		STRGSRC<4:0>					0600
		15:0	ON	—	SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	0000
7010	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>		SAMC<9:0>											0000
		15:0	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCDIV<6:0>							0000
7020	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>						DIGEN7	—	DIGEN5	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>						0000
7030	ADCTRGMODE	31:16	—	—	—	—	SH5ALT<1:0>		SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000
		15:0	—	—	STRGEN5	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	SSAMPEN5	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000
7040	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000
7050	ADCIMCON2	31:16	—	—	—	—	—	—	—	—	DIFF27	SIGN27	DIFF26	SIGN26	DIFF25	SIGN25	DIFF24	SIGN24	0000
		15:0	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000
7060	ADCIMCON3	31:16	DIFF47(1)	SIGN47(1)	DIFF46(1)	SIGN46(1)	DIFF45(1)	SIGN45(1)	—	—	—	—	—	—	DIFF41(1)	SIGN41(1)	DIFF40(1)	SIGN40(1)	0000
		15:0	DIFF39(1)	SIGN39(1)	DIFF38(1)	SIGN38(1)	DIFF37(1)	SIGN37(1)	DIFF36(1)	SIGN36(1)	DIFF35(1)	SIGN35(1)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	—	—	0000
7070	ADCIMCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	DIFF49	SIGN49	DIFF48	SIGN48	0000
7080	ADCGIRQEN1	31:16	—	—	—	—	AGIEN27	AGIEN26	AGIEN25	AGIEN24	AGIEN23(1)	AGIEN22(1)	AGIEN21(1)	AGIEN20(1)	AGIEN19	AGIEN18	AGIEN17	AGIEN16	0000
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000
7090	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	AGIEN53(3)	AGIEN52(3)	AGIEN51(3)	AGIEN50(3)	AGIEN49	AGIEN48	0000
		15:0	AGIEN47(1)	AGIEN46(1)	AGIEN45(1)	—	—	—	AGIEN41(1)	AGIEN40(1)	AGIEN39(1)	AGIEN38(1)	AGIEN37(1)	AGIEN36(1)	AGIEN35(1)	AGIEN34(1)	AGIEN33(1)	AGIEN32(1)	0000
70A0	ADCCSS1	31:16	—	—	—	—	CSS27	CSS26	CSS25	CSS24	CSS23(1)	CSS22(1)	CSS21(1)	CSS20(1)	CSS19	CSS18	CSS17	CSS16	0000
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
70B0	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	CSS53	CSS52	—	CSS50	CSS49	CSS48	0000
		15:0	CSS47(1)	CSS46(1)	CSS45(1)	—	—	—	CSS41(1)	CSS40(1)	CSS39(1)	CSS38(1)	CSS37(1)	CSS36(1)	CSS35(1)	CSS34(1)	CSS33(1)	—	0000
70C0	ADCDSTAT1	31:16	—	—	—	—	ARDY27	ARDY26	ARDY25	ARDY24	ARDY23(1)	ARDY22(1)	ARDY21(1)	ARDY20(1)	ARDY19	ARDY18	ARDY17	ARDY16	0000
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000
70D0	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	ARDY53	ARDY52	—	ARDY50	ARDY49	ARDY48	0000
		15:0	ARDY47(1)	ARDY46(1)	ARDY45(1)	—	—	—	ARDY41(1)	ARDY40(1)	ARDY39(1)	ARDY38(1)	ARDY37(1)	ARDY36(1)	ARDY35(1)	ARDY34(1)	ARDY33(1)	—	0000
70E0	ADCCMPEN1	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
70F0	ADCCMP1	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF15:** AN15 Mode bit
1 = Selects AN15 differential input pair as AN15+ and AN1-
0 = AN15 is using Single-ended mode

bit 30 **SIGN:15** AN15 Signed Data Mode bit
1 = AN15 is using Signed Data mode
0 = AN15 is using Unsigned Data mode

bit 29 **DIFF14:** AN14 Mode bit
1 = Selects AN14 differential input pair as AN14+ and AN1-
0 = AN14 is using Single-ended mode

bit 28 **SIGN14:** AN14 Signed Data Mode bit
1 = AN14 is using Signed Data mode
0 = AN14 is using Unsigned Data mode

bit 27 **DIFF13:** AN13 Mode bit
1 = Selects AN13 differential input pair as AN13+ and AN1-
0 = AN13 is using Single-ended mode

bit 26 **SIGN13:** AN13 Signed Data Mode bit
1 = AN13 is using Signed Data mode
0 = AN13 is using Unsigned Data mode

bit 25 **DIFF12:** AN12 Mode bit
1 = Selects AN12 differential input pair as AN12+ and AN1-
0 = AN12 is using Single-ended mode

bit 24 **SIGN12:** AN12 Signed Data Mode bit
1 = AN12 is using Signed Data mode
0 = AN12 is using Unsigned Data mode

bit 23 **DIFF11:** AN11 Mode bit
1 = Selects AN11 differential input pair as AN11+ and AN1-
0 = AN11 is using Single-ended mode

bit 22 **SIGN11:** AN11 Signed Data Mode bit
1 = AN11 is using Signed Data mode
0 = AN11 is using Unsigned Data mode

REGISTER 25-9: ADCGIRQEN1: ADC GLOBAL INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AGIEN27	AGIEN26	AGIEN25	AGIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN23(1)	AGIEN22(1)	AGIEN21(1)	AGIEN20(1)	AGIEN19	AGIEN18	AGIEN17	AGIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AGIEN27:AGIEN0:** ADC Global Interrupt Enable bits

1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT1 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

REGISTER 26-12: CxFLTCON2: CAN FILTER CONTROL REGISTER 2 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-13: CxFLTCON3: CAN FILTER CONTROL REGISTER 3 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = 11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = 11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-16: CxFIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('x' = 1-4;'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	FSIZE<4:0>(1)				
15:8	U-0	S/HC-0	S/HC-0	R/W-0	U-0	U-0	U-0	U-0
	—	FRESET	UINC	DONLY(1)	—	—	—	—
7:0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXEN	TXABAT(2)	TXLARB(3)	TXERR(3)	TXREQ	RTREN	TXPR<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **FSIZE<4:0>:** FIFO Size bits(1)

11111 = FIFO is 32 messages deep

•

•

•

00010 = FIFO is 3 messages deep

00001 = FIFO is 2 messages deep

00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRESET:** FIFO Reset bits

1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user should poll whether this bit is clear before taking any action.

0 = No effect

bit 13 **UINC:** Increment Head/Tail bit

TXEN = 1: (FIFO configured as a Transmit FIFO)
When this bit is set the FIFO head will increment by a single message

TXEN = 0: (FIFO configured as a Receive FIFO)
When this bit is set the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit(1)

TXEN = 1: (FIFO configured as a Transmit FIFO)
This bit is not used and has no effect.

TXEN = 0: (FIFO configured as a Receive FIFO)
1 = Only data bytes will be stored in the FIFO
0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as '0'

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CxCON<23:21>) = 100).

2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

3: This bit is reset on any read of this register or when the FIFO is reset.

REGISTER 27-2: CMxCON: OP AMP/COMPARATOR 'x' CONTROL REGISTER ('x' = 1-5) (CONTINUED)

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12 **Unimplemented:** Read as '0'

bit 11 **OAO:** Op amp Output Enable bit(1)
1 = Op amp output is present on the OAxOUT pin
0 = Op amp output is not present on the OAxOUT pin

bit 10 **AMPMOD:** Op amp Mode Enable bit(1)
1 = Amplifier/Comparator operating in Dual mode (both Op amps and Comparators are enabled)
0 = Amplifier/Comparator operating in Comparator-only mode

bit 9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{TH+}$
0 = $V_{IN+} < V_{TH-}$

When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{TH-}$
0 = $V_{IN+} > V_{TH+}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event Polarity Select bits
11 = Trigger/Event generated on any change of the comparator output
10 = Trigger/Event generated only on high-to-low transition of the polarity-selected comparator output
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output
01 = Trigger/Event generated only on low-to-high transition of the polarity-selected comparator output
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output
00 = Trigger/Event generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Op amp/Comparator Reference Select bit
1 = V_{IN+} input connects to internal CDAC3 output voltage
0 = V_{IN+} input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

Note 1: Before attempting to initialize or enable any of the Op amp bit, the user application must clear the corresponding OPA5MD, OPA3MD, OPA2MD, and OPA1MD bits in the PMD register.

Note: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition is occurred. The IFSx bits are persistent, so they must be cleared if they are set by user software after an IFSx user bit interrogation.

32.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MK GP/MC devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

32.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

32.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

33.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MK GP/MC devices is designed to operate at a nominal 1.2V. To simplify system designs, devices in the PIC32MK GP/MC family incorporate an on-chip regulator providing the required core logic voltage from VDD.

33.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

33.3.2 ON-CHIP REGULATOR AND BOR

PIC32MK GP/MC devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **36.1 "DC Characteristics"**.

33.4 On-chip Temperature Sensor

PIC32MK GP/MC devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **36.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

33.5 Programming and Diagnostics

PIC32MK GP/MC devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32MK devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 33-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS

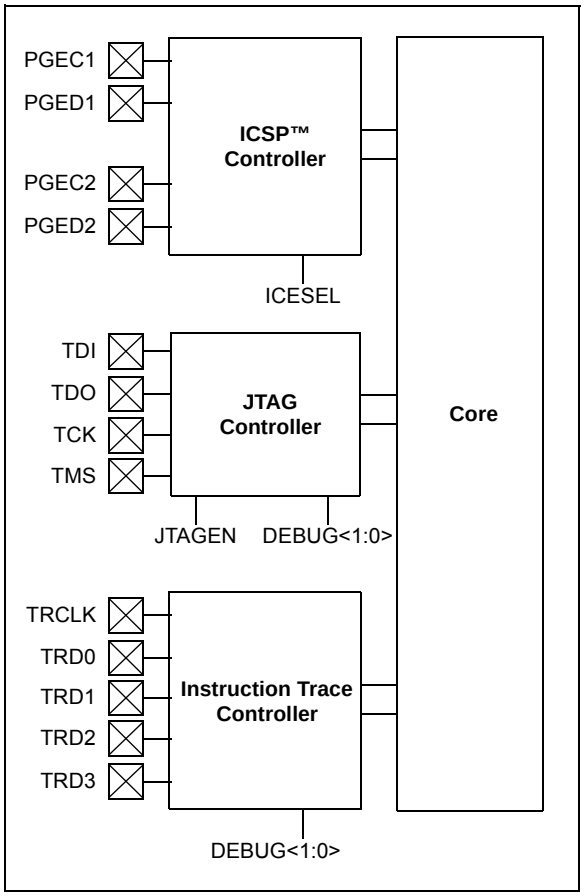


TABLE 36-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Param. No.	**Typical(2)**	**Maximum**	**Units**	**Conditions**	
Power-Down Current (IPD) (Note 1)					
DC40k	400	1200	µA	-40°C	Base Power-Down Sleep
DC40l	600	1200	µA	+25°C	
DC40m	1.8	6	mA	+85°C	
DC40o	4.5	10	mA	+125ºC	
DC41	6	40	µA	-40°C to 125ºC	Deep Sleep
DC42	6	40	µA	-40°C to 125ºC	VBAT
Module Differential Current					
DC41e	5	—	µA	3.6V	Watchdog Timer Current: ΔIWDT **(Note 3)**
DC42e	25	—	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)**
DC43d	3	—	mA	3.6V	ADC: ΔIADC **(Notes 3, 4)**

Note 1: The test conditions for IPD current measurements are as follows:

Sleep:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled, VUSB3V3 is connected to VDD
- PBCLKx divisor = 1:2 ('x' =/= 1,6,7), PBCLK6 = 1:4, PBCLK1 and PBCLK7 = 1:1
- CPU is in Sleep mode
- Prefetch module is disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is '0' (i.e., clocks enabled)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)
- IOANCPEN (CFGCON<7>) = 0, I/O Analog Charge Pump disabled
- AICPMPEN (ADCCON1><12>) = 0, ADC Input Charge Pump disabled

Deep Sleep Base plus Sleep:

- DSCON = POR state
- UPLLEN (DEVCFG2<31>) = 1 (PLL disabled)
- FSDEN (DEVCFG2<28>) = 1 (Deep Sleep enabled)
- DSWDTEN (DEVCFG2<27>) = 0 (Deep Sleep Watchdog disabled)
- DSBOREN (DEVCFG2<20>) = 0 (Deep Sleep BOR disabled)
- VBATBOREN (DEVCFG2<19>) = 0 (VBAT BOR disabled)

Deep Sleep with DSWDT:

- Deep Sleep Base plus DSWDTEN (DEVCFG2<27>) = 1 (Deep Sleep Watchdog enabled)

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

4: Voltage regulator is operational (VREGS = 1)

TABLE 36-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20a	VOH1	**Output High Voltage** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15 RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5, RF6, RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	1.5	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -12 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - 8x Source Driver Pins - RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6, RC7, RC8, RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	1.5	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -18 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.