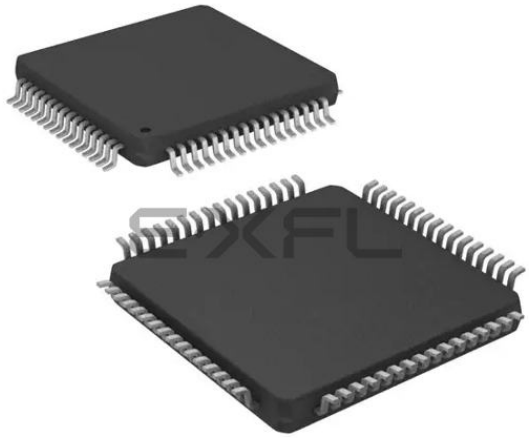
Microchip Technology - PIC32MK0512MCF064T-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 27x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512mcf064t-i-pt

3.6 MIPS32® microAptiv™ MCU Core Configuration

Register 3-1 through Register 3-5 show the default configuration of the MIPS32 microAptiv MCU core, which is included on the PIC32MK GP/MC family of devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	ISP
23:16	R-0	R-0	R-1	R-0	U-0	R-1	R-0	R-0
	DSP	UDI	SB	MDU	—	MM<1:0>		BM
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-1
	BE	AT<1:0>		AR<2:0>			U-0	U-0
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	—	—
	—	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the Config1 register.

bit 30-25 **Unimplemented:** Read as '0'

bit 24 **ISP:** Instruction Scratch Pad RAM bit
0 = Instruction Scratch Pad RAM is not implemented

bit 23 **DSP:** Data Scratch Pad RAM bit
0 = Data Scratch Pad RAM is not implemented

bit 22 **UDI:** User-defined bit
0 = CorExtend User-Defined Instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19 **Unimplemented:** Read as '0'

bit 18-17 **MM<1:0>:** Merge Mode bits
10 = Merging is allowed

bit 16 **BM:** Burst Mode bit
0 = Burst order is sequential

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-3 **Unimplemented:** Read as '0'

REGISTER 3-8: FCCR: FLOATING POINT CONDITION CODES REGISTER; CP1 REGISTER 25

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	FCC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FCC<7:0>:** Floating Point Condition Code bits

These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Number	Target Description	SBTxREGy Register					SBTxRDy Register		SBTxWRy Register	
		Name	Region	Physical Start Address	Region Size	Priority Level	Name	Read Permission (Group3, Group2, Group1, Group0)	Name	Write Permission (Group3, Group2, Group1, Group0)
0	System Bus	SBT0REG0	Region 0	1F8F0000		0	SBT0RD0	1,1,1,1	SBT0WR0	1,1,1,1
		SBT0REG1	Region 1	1F8F8000	32 KB	3	SBT0RD1	0,0,0,1	SBT0WR1	0,0,0,1
1	Flash Memory (CPU Instruction) Program Flash Boot Flash Prefetch	SBT1REG0	Region 0	1D000000		0	SBT1RD0	1,1,1,1	SBT1WR0	0,0,0,0
		SBT1REG2	Region 2	1FC04000	4 KB	2	SBT1RD2	0,0,0,1	SBT1WR2	0,0,0,0
		SBT1REG3	Region 3	1FC24000	4 KB	2	SBT1RD3	0,0,0,1	SBT1WR3	0,0,0,0
		SBT1REG4	Region 4	1FC44000	4 KB	2	SBT1RD4	0,0,0,1	SBT1WR4	0,0,0,0
		SBT1REG5	Region 5	1FC64000	4 KB	2	SBT1RD5	0,0,0,1	SBT1WR5	0,0,0,0
2	Flash Memory (CPU data) Program Flash	SBT2REG0	Region 0	1D000000		0	SBT2RD0	1,1,1,1	SBT2WR0	0,0,0,0
		SBT2REG2	Region 2	1FC04000	4 KB	2	SBT2RD2	0,0,0,1	SBT2WR2	0,0,0,0
		SBT2REG3	Region 3	1FC24000	4 KB	2	SBT2RD3	0,0,0,1	SBT2WR3	0,0,0,0
		SBT2REG4	Region 4	1FC44000	4 KB	2	SBT2RD4	0,0,0,1	SBT2WR4	0,0,0,0
		SBT2REG5	Region 5	1FC64000	4 KB	2	SBT2RD5	0,0,0,1	SBT2WR5	0,0,0,0
3	Flash Memory (peripheral) Program Flash	SBT3REG0	Region 0	1D000000		0	SBT3RD0	1,1,1,1	SBT3WR0	0,0,0,0
		SBT3REG2	Region 2	1FC04000	4 KB	2	SBT3RD2	0,0,0,1	SBT3WR2	0,0,0,0
		SBT3REG3	Region 3	1FC24000	4 KB	2	SBT3RD3	0,0,0,1	SBT3WR3	0,0,0,0
		SBT3REG4	Region 4	1FC44000	4 KB	2	SBT3RD4	0,0,0,1	SBT3WR4	0,0,0,0
		SBT3REG5	Region 5	1FC64000	4 KB	2	SBT3RD5	0,0,0,1	SBT3WR5	0,0,0,0

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0450	IPC49	31:16	—	—	—	OC10IP<2:0>			OC10IS<1:0>		—	—	—	IC10IP<2:0>			IC10IS<1:0>		0000
		15:0	—	—	—	IC10EIP<2:0>			IC10EIS<1:0>		—	—	—	—	—	—	—	—	0000
0460	IPC50	31:16	—	—	—	IC12EIP<2:0>			IC12EIS<1:0>		—	—	—	OC11IP<2:0>			OC11IS<1:0>		0000
		15:0	—	—	—	IC11IP<2:0>			IC11IS<1:0>		—	—	—	IC11EIP<2:0>			IC11EIS<1:0>		0000
0470	IPC51	31:16	—	—	—	IC13IP<2:0>			IC13IS<1:0>		—	—	—	IC13EIP<2:0>			IC13EIS<1:0>		0000
		15:0	—	—	—	OC12IP<2:0>			OC12IS<1:0>		—	—	—	IC12IP<2:0>			IC12IS<1:0>		0000
0480	IPC52	31:16	—	—	—	OC14IP<2:0>			OC14IS<1:0>		—	—	—	C14IP<2:0>			C14IS<1:0>		0000
		15:0	—	—	—	IC14EIP<2:0>			IC14EIS<1:0>		—	—	—	OC13IP<2:0>			OC13IS<1:0>		0000
0490	IPC53	31:16	—	—	—	IC16EIP<2:0>			IC16EIS<1:0>		—	—	—	OC15IP<2:0>			OC15IS<1:0>		0000
		15:0	—	—	—	IC15IP<2:0>			IC15IS<1:0>		—	—	—	IC15EIP<2:0>			IC15EIS<1:0>		0000
04A0	IPC54	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	OC16IP<2:0>			OC16IS<1:0>		—	—	—	IC16IP<2:0			IC16IS<1:0>		0000
04B0	IPC55	31:16	—	—	—	SPI4TXIP<2:0>			SPI4TXIS<1:0>		—	—	—	SPI4RXIP<2:0>			SPI4RXIS<1:0>		0000
		15:0	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
04C0	IPC56	31:16	—	—	—	SPI6EIP<2:0>			SPI6EIS<1:0>		—	—	—	SPI5TXIP<2:0>			SPI5TXIS<1:0>		0000
		15:0	—	—	—	SPI5RXIP<2:0>			SPI5RXIS<1:0>		—	—	—	SPI5EIP<2:0>			SPI5EIS<1:0>		0000
04D0	IPC57	31:16	—	—	—	—	—	—	—	—	—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	SPI6TXIP<2:0>			SPI6TXIS<1:0>		—	—	—	SPI6RXIP<2:0>			SPI6RXIS<1:0>		0000
0510	IPC61	31:16	—	—	—	—	—	—	—	—	—	—	—	AD1DC4IP<2:0>			AD1DC4IS<1:0>		0000
		15:0	—	—	—	AD1DC3IP<2:0>			AD1DC3IS<1:0>		—	—	—	USB2IP<2:0>(2)			USB2IS<1:0>(2)		0000
0530	IPC63	31:16	—	—	—	—	—	—	—	—	—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0540	OFF000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0544	OFF001	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0548	OFF002	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 9-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

bit 10-8 **PLLIDIV<2:0>:** System PLL Input Clock Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set to Divide-by-1.

bit 7 **PLLICLK:** System PLL Input Clock Source bit

1 = FRC is selected as the input to the System PLL
0 = POSC is selected as the input to the System PLL
The POR default is specified by the FPLLICLK Configuration bit in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **PLLRANGE<2:0>:** System PLL Frequency Range Selection bits

111 = Reserved
110 = 54-64 MHz
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

Use the highest filter range that covers the input freq to the VCO multiplier block that corresponds to the PLLIDIV output freq to minimize PLL system jitter (see Figure 9-1). For example, Crystal = 20 MHz, PLLIDIV<2:0> = 0b1; therefore, the filter input frequency is equal to 10 MHz and UPLLRANGE<2:0> = '0b010. The default setting is specified by the FPLLRNG<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

3: While the PLL is active, and if updating the PLL bits in the OSCCON register at run-time, the user application must remain within the following limits at all times for all nodes in the PLL clock tree. Therefore, the order in which the PLL values may be modified, (i.e., PLLODIV, PLLMULT, PLLODIV) becomes important. Failure to maintain PLL nodes within min/max ranges may result in unstable PLL and system behavior.

- Output and input to PLLIDIV block (i.e., FPLLI) 5 MHz to 64 MHz (min/max at all times)
- VCO output, (i.e., FVCO) 350 MHz to 700 MHz (min/max at all times)
- Output of PLLODIV, (i.e., FPLL) 10 MHz to 120 MHz (min/max at all times)

11.1 DMA Control Registers

TABLE 11-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
1010	DMASTAT	31:16	RDWR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	DMACH<2:0>			0000
1020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 11-2: DMA CRC REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
1040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
1050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT2	INT2R<3:0>	INT2R	0000 = RPB6
T4CK	T4CKR<3:0>	T4CKR	0001 = RPC15
T8CK	T8CKR<3:0>	T8CKR	0010 = RPA4
IC1	IC1R<3:0>	IC1R	0011 = RPB13
IC5	IC5R<3:0>	IC5R	0100 = RPB2
IC9	IC9R<3:0>	IC9R	0101 = RPC6
IC13	IC13R<3:0>	IC13R	0110 = RPC1
U1RX	U1RXR<3:0>	U1RXR	0111 = RPA7
$\overline{\text{U2CTS}}$	U2CTSR<3:0>	U2CTSR	1000 = RPE14
U5RX	U5RXR<3:0>	U5RXR	1001 = RPC13
$\overline{\text{SS1}}$	SS1R<3:0>	SS1R	1010 = RPG8
$\overline{\text{SS3}}$	SS3R<3:0>	SS3R	1011 = Reserved
$\overline{\text{SS4}}$	SS4R<3:0>	SS4R	1100 = RPF0
$\overline{\text{SS5}}$	SS5R<3:0>	SS5R	1101 = RPD4(1)
INDX1	INDX1R<3:0>	INDX1R	1110 = Reserved
QEB2	QEB2R<3:0>	QEB2R	1111 = Reserved
INDX3	INDX3R<3:0>	INDX3R	
QEB4	QEB4R<3:0>	QEB4R	
INDX5	INDX5R<3:0>	INDXR5	
QEB6	QEB6R<3:0>	QEB6R	
C1RX	C1RXR<3:0>	C1RXR	
OCFB	OCFBR<3:0>	OCFBR	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-8: PORTD REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TRISD8(2)	—	TRISD6	TRISD5	—	—	—	—	—	0160
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RD8(2)	—	RD6	RD5	—	—	—	—	—	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	LATD8(2)	—	LATD6	LATD5	—	—	—	—	—	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	ODCD8(2)	—	ODCD6	ODCD5	—	—	—	—	—	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNPUD8(2)	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNPDD8(2)	—	CNPDD6	CNPDD5	—	—	—	—	—	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNIED8(2)	—	CNIED6	CNIED5	—	—	—	—	—	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CN STATD8(2)	—	CN STATD6	CN STATD5	—	—	—	—	—	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNNED8(2)	—	CNNED6	CNNED5	—	—	—	—	—	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNFD8(2)	—	CNFD6	CNFD5	—	—	—	—	—	0000
03C0	SRCON0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR0D8(2)	—	SR0D6	SR0D5	—	—	—	—	—	0000
03D0	SRCON1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR1D8(2)	—	SR1D6	SR1D5	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on general purpose devices.

NOTES:

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7840	ADCDATA36(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7850	ADCDATA37(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7860	ADCDATA38(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7870	ADCDATA39(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7880	ADCDATA40(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7890	ADCDATA41(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78D0	ADCDATA45(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78E0	ADCDATA46(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78F0	ADCDATA47(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7900	ADCDATA48	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7910	ADCDATA49	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7920	ADCDATA50(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7940	ADCDATA52(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7950	ADCDATA53(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7E00	ADCSYSCFG0	31:16	—	—	—	—	AN27	AN26	AN25	AN24	AN23(1)	AN22(1)	AN21(1)	AN20(1)	AN19	AN18	AN17	AN16	0FxF
		15:0	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	FFFF
7E10	ADCSYSCFG1	31:16	—	—	—	—	—	—	—	—	—	—	AN53(1)	AN52(1)	—	AN50(1)	AN49	AN48	00xx
		15:0	AN47(1)	AN46(1)	AN45(1)	—	—	—	AN41(1)	AN40(1)	AN39(1)	AN38(1)	AN37(1)	AN36(1)	AN35(1)	AN34(1)	AN33(1)	—	xxxx
7D00	ADC0CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-37: ADCEISTAT2: ADC EARLY INTERRUPT STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	EIRDY53	EIRDY52	EIRDY51	EIRDY50	EIRDY49	EIRDY48
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIRDY41(1)	EIRDY40(1)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0
	EIRDY39(1)	EIRDY38(1)	EIRDY37(1)	EIRDY36(1)	EIRDY35(1)	EIRDY34(1)	EIRDY33(1)	—

Legend:	HS = Hardware Set	HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-13 **EIRDY53:EIRDY45:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9-1 **EIRDY41:EIRDY33:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

REGISTER 26-3: CxINT: CAN INTERRUPT REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF(1)	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 26-20 **Unimplemented:** Read as '0'

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CxCON<15>).

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 7-6 **OVRDAT<1:0>:** State(3) for PWMxH, PWMxL Pins if Override is Enabled bits
If OVRENH = 1, OVRDAT<1> provides data for PWMxH
If OVRENL = 1, OVRDAT<0> provides data for PWMxL

bit 5-4 **FLTDAT<1:0>:** State(3) for PWMxH and PWMxL Pins if FLTMOD is Enabled bits(2)
If FLTMOD<1:0> (IOCONx<17:16>) = 00 or 01, one of the following Fault modes is enabled:
If fault is active, FLTDAT<1> provides the state for PWMxH
If fault is active, FLTDAT<0> provides the state for PWMxL
If fault is inactive, FLTDAT<1:0> bits are ignored

bit 3-2 **CLDAT<1:0>:** State for PWMxH and PWMxL Pins if CLMOD is Enabled bits(3)
If CLMOD (IOCONx<24>) = 1, Current-Limit mode is enabled, as follows:
If current limit is active, CLTDAT<1> provides the state for PWMxH
If current limit is active, CLTDAT<0> provides the state for PWMxL
If current limit is inactive, CLTDAT<1:0> bits are ignored

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to PWMxL pin; PWMxL output signal is connected to PWMxH pin
0 = PWMxH and PWMxL output signals pins are mapped to their respective pins

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

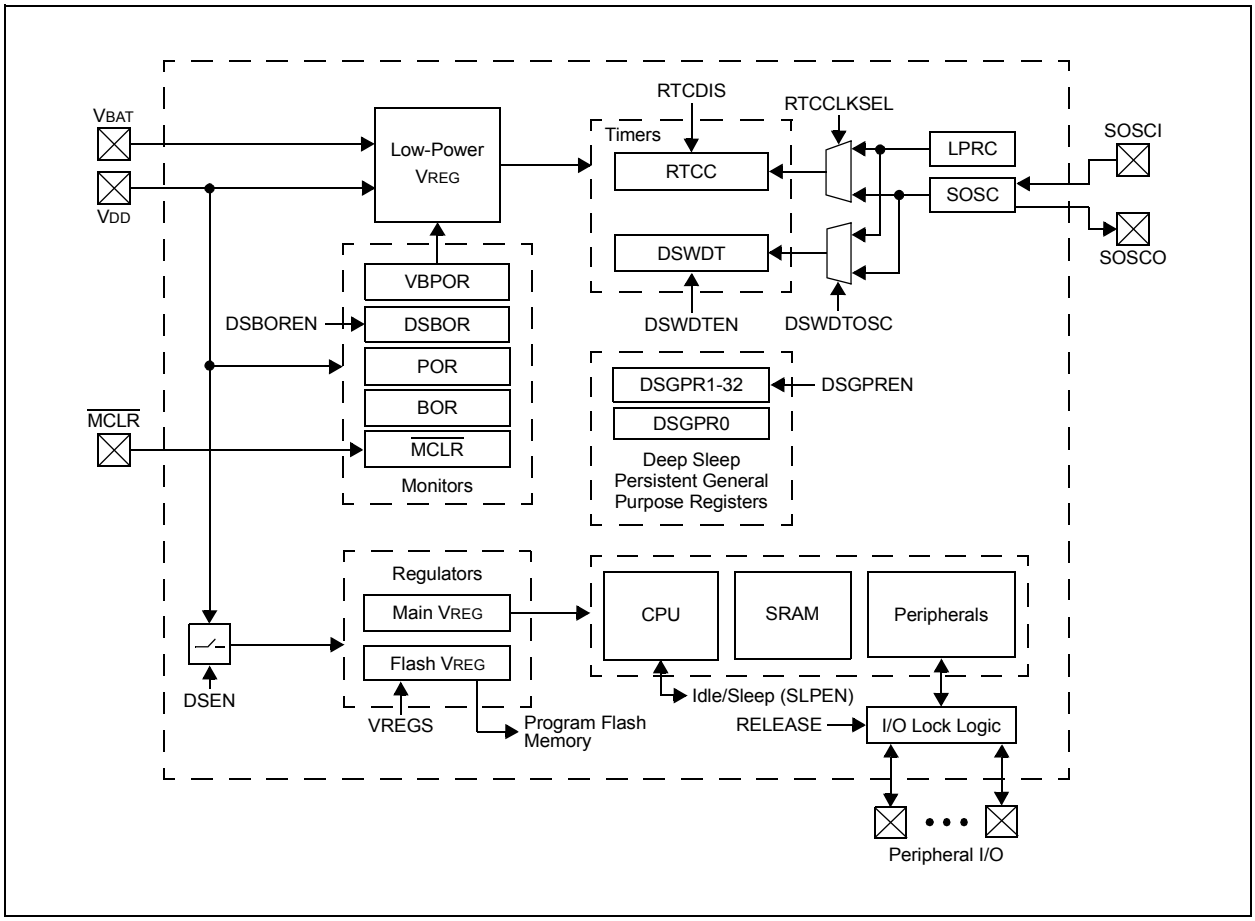
Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

FIGURE 32-1: LOW-POWER DEVICE BLOCK DIAGRAM



REGISTER 32-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER(3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
	—	—	—	—	—	—	—	DSINT0
7:0	R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0
	DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	—

Legend:		HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit
1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 **Unimplemented:** Read as '0'

Note 1: All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

2: To ensure a successful write, this register must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

3: After waking from deep sleep, writes to the DSWAKE register are ignored until the RELEASE bit (DSCON<0>) is cleared.

TABLE 32-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0040	PMD1(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	EEMD	CTMUMD	—	DAC3MD	DAC2MD	DAC1MD	—	—	—	ADCMD	0000
0050	PMD2(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	OPA5MD	—	OPA3MD	OPA2MD	OPA1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	CMP5MD	C4MPMD	C3MPMD	CMP2MD	CMP1MD	0000
0060	PMD3(2)	31:16	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
0070	PMD4(2)	31:16	—	—	—	—	PWM12MD	PWM11MD	PWM10MD	PWM9MD	PWM8MD	PWM7MD	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	0000
		15:0	—	—	—	—	—	—		T9MD	T8MD	T7MD	T6MD	T5MD	T4MD	T3MD	T2MD	T1MD	0000
0080	PMD5(1,2)	31:16	CAN4MD	CAN3MD	CAN2MD	CAN1MD	—	—	USB2MD	USB1MD	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SPI6MD	SPI5MD	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	U6MD	U5MD	U4MD	U3MD	U2MD	U1MD	0000
0090	PMD6(2)	31:16	—	—	—	—	QEI4MD	QEI3MD	QEI2MD	QEI1MD	—	—	—	—	QEI6MD	QEI5MD	—	PMPMD	0000
		15:0	—	—	—	—	REFO4MD	REFO3MD	REFO2MD	REFO1MD	—	—	—	—	—	—	—	—	0000
00A0	PMD7(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

2: For any associated PMDx bit, '0' = clocks enabled to the peripheral; '1' = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

REGISTER 33-3: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits
1xx = Allow CPU access to Permission Group 2 permission regions
x1x = Allow CPU access to Permission Group 1 permission regions
xx1 = Allow CPU access to Permission Group 0 permission regions
0xx = Deny CPU access to Permission Group 2 permission regions
x0x = Deny CPU access to Permission Group 1 permission regions
xx0 = Deny CPU access to Permission Group 0 permission regions

Note: When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

bit 10 **FSLEEP:** Flash Sleep Mode bit
1 = Flash is powered down when the device is in Sleep mode
0 = Flash power down is controlled by the VREGS bit (PWRCON<0>)

bit 9-7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
1 = Boot code and Exception code is MIPS32
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit(1)
1 = JTAG is enabled
0 = JTAG is disabled

Note: On Reset, this Configuration bit is copied into JTAGEN (CFGCON<3>). If JTAGEN (DEVCFG0<2>) = 0, the JTAGEN bit cannot be set to '1' by the user application at run-time, as JTAG is always disabled. However, if JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time as by simply writing JTAGEN (CFGCON<3> as required.

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
11 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Disabled
10 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Enabled
01 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Disabled
00 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Enabled

Note: When the FJTAGEN or JTAGEN bits are equal to '0', this prevents 4-wire JTAG debugging, but not PGECx/PGEDx debugging.

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

35.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

35.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9b	TSCK	SCKx Period	22	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 All other remappable SPI pins not contained in conditions for parameter SP9a.
			41	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 All other remappable SPI pins not contained in conditions for parameter SP9a.
			59	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 All other remappable SPI pins not contained in conditions for parameter SP9a.
			74	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 All other remappable SPI pins not contained in conditions for parameter SP9a.
SP70	TSCL	SCKx Input Low Time	TSCK/2	—	—	ns	—
SP71	TSCH	SCKx Input High Time	TSCK/2	—	—	ns	—
SP72	TSCF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TSCR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP35	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

NOTES: