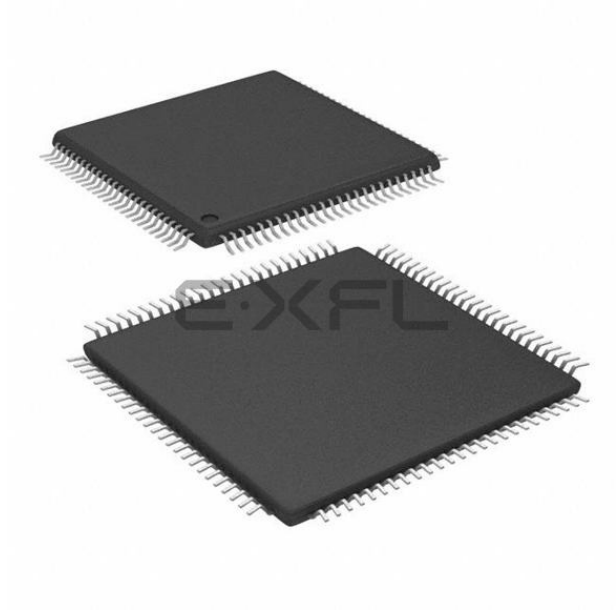
Microchip Technology - PIC32MK0512MCF100-E/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512mcf100-e-pt

REGISTER 5-6: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit
1 = Register is not locked and can be modified
0 = Register is locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits
Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 7-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

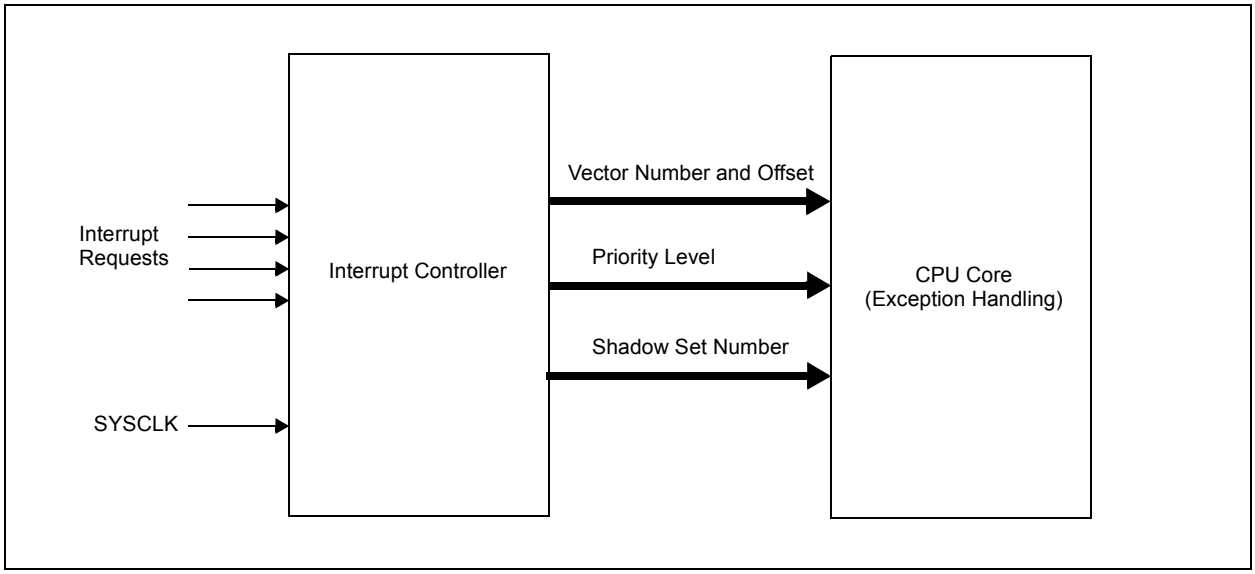
bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enable software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

Figure 8-1 shows the block diagram for the Interrupt Controller and CPU exceptions.

FIGURE 8-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



8.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 8-2 lists the exception types in order of priority.

REGISTER 11-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 12-9: UxEIE: USB ERROR INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

Note: For an interrupt to propagate USBIF, the UERRIE bit (UxIE<1>) must be set.

NOTES:

REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCSEL<1:0>		CONCLKDIV<5:0>					
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIGEN7	—	DIGEN5	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R-0, HS, HC
	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP(1,2,3,4)	RQCNVRT
7:0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GLSWTRG	GSWTRG	ADINSEL<5:0>					

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **ADCSEL<1:0>:** Analog-to-Digital Clock Source (TCLK) bits
11 = SYSCLK
10 = REFCLK3
01 = FRC
00 = PBCLK5

bit 29-24 **CONCLKDIV<5:0>:** Analog-to-Digital Control Clock (TQ) Divider bits
111111 = 126 * TCLK = TQ
•
•
•
000011 = 6 * TCLK = TQ
000010 = 4 * TCLK = TQ
000001 = 2 * TCLK = TQ
000000 = TCLK = TQ

bit 23 **DIGEN7:** Shared ADC (ADC7) Digital Enable bit
1 = ADC7 is digital enabled
0 = ADC7 is digital disabled

bit 22 **Unimplemented:** Read as '0'

bit 21 **DIGEN5:** ADC5 Digital Enable bit
1 = ADC5 is digital enabled (required for active operation)
0 = ADC5 is digital disabled (power-saving mode)

bit 20 **DIGEN4:** ADC4 Digital Enable bit
1 = ADC4 is digital enabled (required for active operation)
0 = ADC4 is digital disabled (power-saving mode)

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 25-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

bit 13 **STRGEN5:** ADC5 Presynchronized Triggers bit
1 = ADC5 uses presynchronized triggers
0 = ADC5 does not use presynchronized triggers

bit 12 **STRGEN4:** ADC4 Presynchronized Triggers bit
1 = ADC4 uses presynchronized triggers
0 = ADC4 does not use presynchronized triggers

bit 11 **STRGEN3:** ADC3 Presynchronized Triggers bit
1 = ADC3 uses presynchronized triggers
0 = ADC3 does not use presynchronized triggers

bit 10 **STRGEN2:** ADC2 Presynchronized Triggers bit
1 = ADC2 uses presynchronized triggers
0 = ADC2 does not use presynchronized triggers

bit 9 **STRGEN1:** ADC1 Presynchronized Triggers bit
1 = ADC1 uses presynchronized triggers
0 = ADC1 does not use presynchronized triggers

bit 8 **STRGEN0:** ADC0 Presynchronized Triggers bit
1 = ADC0 uses presynchronized triggers
0 = ADC0 does not use presynchronized triggers

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **SSAMPEN5:** ADC5 Synchronous Sampling bit
1 = ADC5 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC5 does not use synchronous sampling

bit 4 **SSAMPEN4:** ADC4 Synchronous Sampling bit
1 = ADC4 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC4 does not use synchronous sampling

bit 3 **SSAMPEN3:** ADC3 Synchronous Sampling bit
1 = ADC3 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC3 does not use synchronous sampling

bit 2 **SSAMPEN2:** ADC2Synchronous Sampling bit
1 = ADC2 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC2 does not use synchronous sampling

bit 1 **SSAMPEN1:** ADC1 Synchronous Sampling bit
1 = ADC1 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC1 does not use synchronous sampling

bit 0 **SSAMPEN0:** ADC0 Synchronous Sampling bit
1 = ADC0 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC0 does not use synchronous sampling

Note 1: Regardless of which alternate input is selected by SHxALT, for ADC0-ADC5 only, all control and results are handled by the native SHxALT = '0b00 input. For example, SH0ALT = '0b11 = AN24. However, from a software and silicon hardware control and results register perspective, the user must initialize the ADC0 module as if AN24 were actually AN0.

REGISTER 26-10: CxFLTCON0: CAN FILTER CONTROL REGISTER 0 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

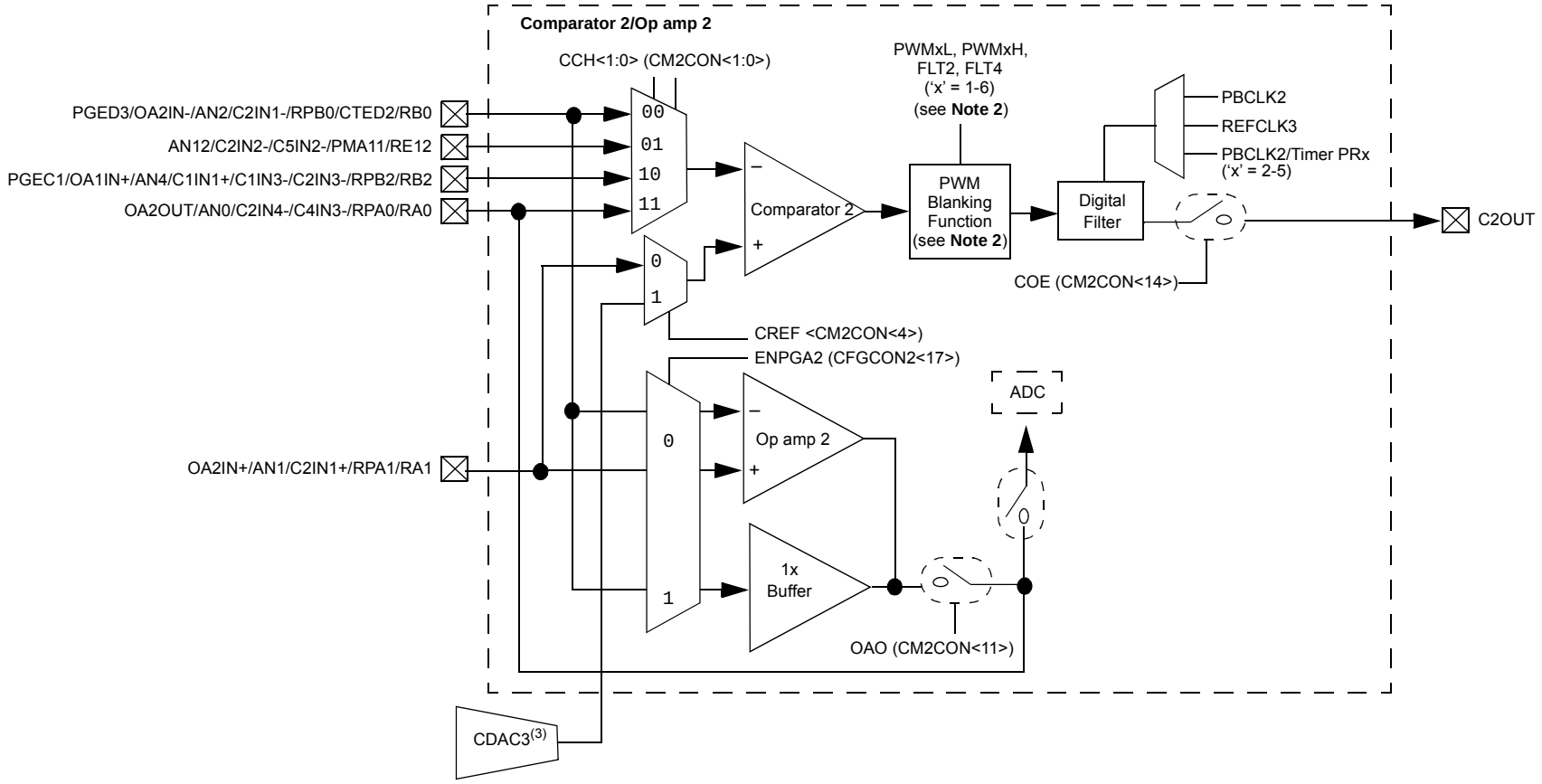
bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

NOTES:

FIGURE 27-2: OP AMP 2/COMPARATOR 2 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is available only on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

NOTES:

32.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MK GP/MC devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

32.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

32.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

REGISTER 33-6: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	r-1	r-1	r-1
	FVBUSIO1	FUSBIDIO1	IOL1WAY	PMDL1WAY	PGL1WAY	—	—	—
23:16	R/P	R/P	r-1	R/P	r-1	r-1	r-1	r-1
	FVBUSIO2	FUSBIDIO2	—	PWMLOCK	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FVBUSIO1:** USB1 VBUSON Selection bit
1 = VBUSON pin is controlled by the USB1 module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO1:** USB1 USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27 **PGL1WAY:** Permission Group Lock One Way Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 26-24 **Reserved:** Write as '1'

bit 23 **FVBUSIO2:** USB2 VBUSON Selection bit
1 = VBUSON pin is controlled by the USB2 module
0 = VBUSON pin is controlled by the port function

bit 22 **FUSBIDIO2:** USB2 USBID Selection bit
1 = USBID pin is controlled by the USB2 module
0 = USBID pin is controlled by the port function

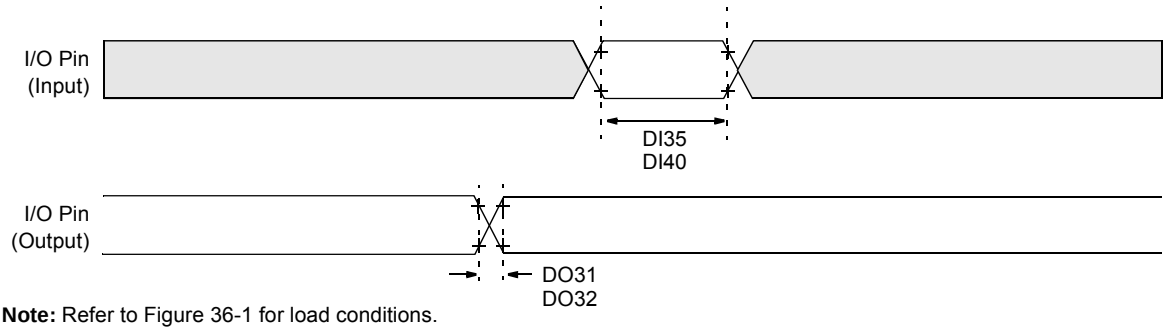
bit 21 **Reserved:** Write as '1'

bit 20 **PWMLOCK:** PWM Write Access Select bit
1 = Write accesses to the PWM IOCONx register are not locked or protected
0 = Write accesses to the PWM IOCONx register must use the PWMKEY unlock procedure

bit 19-16 **Reserved:** Write as '1'

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

FIGURE 36-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-22: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS		**Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	**Port Output Rise Time** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15, RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5-RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - Replace 8x Source Driver pins with: RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6-RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

TABLE 36-43: CTMU CURRENT SOURCE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU CURRENT SOURCE							
CTMU0	RES	Resolution	-2	—	+2	ºC	3.3V @ -40ºC to 125ºC
CTMUI1	IOUT1	Base Range(1)	—	0.55	—	µA	CTMUCON<1:0> = 01
CTMUI2	IOUT2	10x Range(1)	—	5.5	—	µA	CTMUCON<1:0> = 10
CTMUI3	IOUT3	100x Range(1)	—	55	—	µA	CTMUCON<1:0> = 11
CTMUI4	IOUT4	1000x Range(1)	—	550	—	µA	CTMUCON<1:0> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage(1,2)	—	0.598	—	V	TA = +25ºC, CTMUCON<1:0> = 01
			—	0.658	—	V	TA = +25ºC, CTMUCON<1:0> = 10
			—	0.721	—	V	TA = +25ºC, CTMUCON<1:0> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change(1,2)	—	-1.92	—	mV/ºC	CTMUCON<1:0> = 01
			—	-1.74	—	mV/ºC	CTMUCON<1:0> = 10
			—	-1.56	—	mV/ºC	CTMUCON<1:0> = 11

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

FIGURE 36-19: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

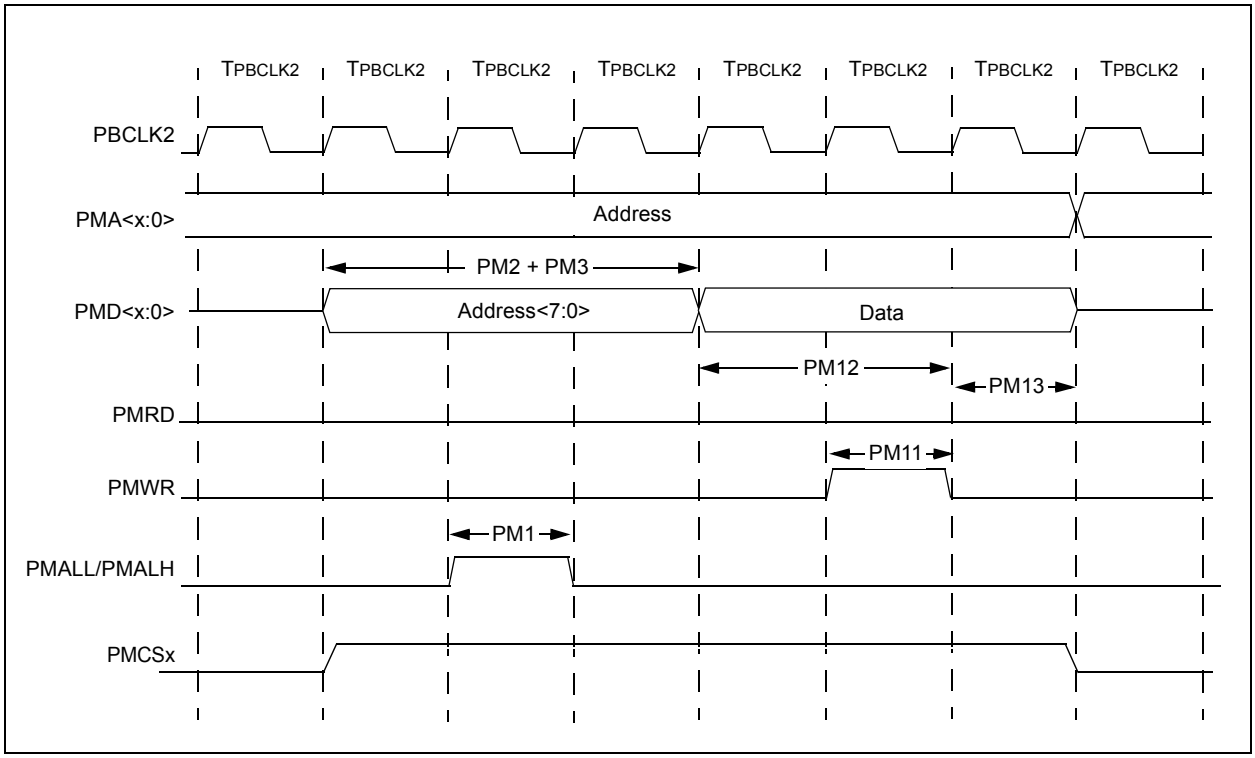


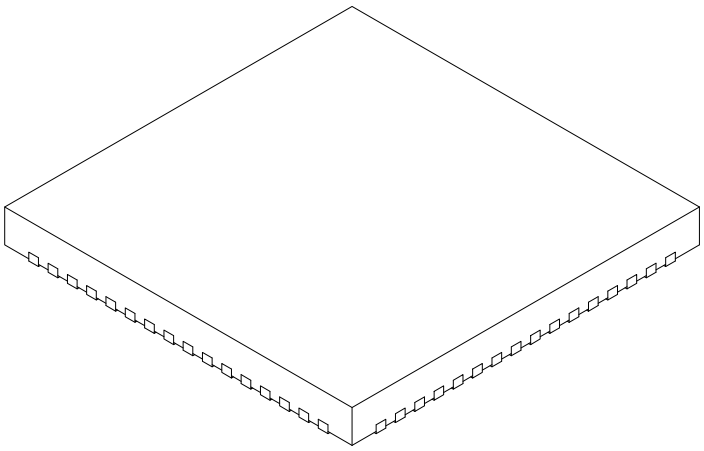
TABLE 36-46: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM11	TWR	PMWR Pulse Width	—	1 TPBCLK2	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPBCLK2	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPBCLK2	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

NOTES: