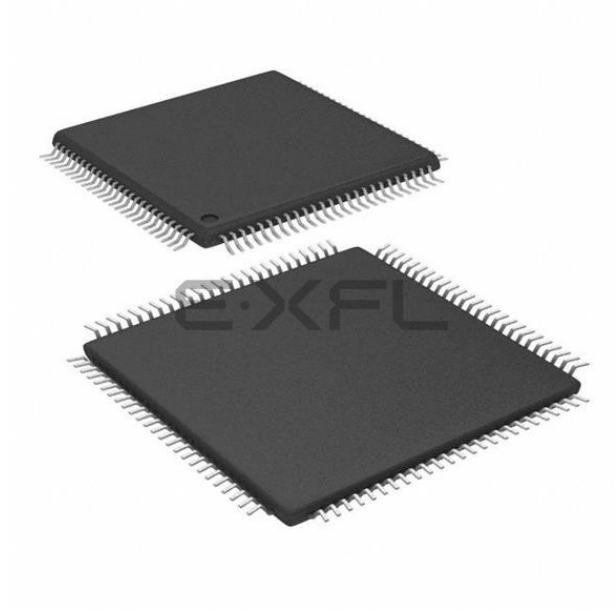
Microchip Technology - PIC32MK0512MCF100T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk0512mcf100t-i-pt

TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MK0512GPD100
PIC32MK0512GPE100
PIC32MK1024GPD100
PIC32MK1024GPE100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/PMA23/RG15	36	VSS
2	VDD	37	VDD
3	TCK/RPA7/PMD5/RA7	38	AN35/RG11
4	RPB14/VBUSON1/PMD6/RB14	39	AN36/RF13
5	RPB15/PMD7/RB15	40	AN37/RF12
6	RD1	41(6)	AN12/C2IN2-/C5IN2-/PMA11/RE12
7	RD2	42(5)	AN13/C3IN2-/PMA10/RE13
8	RPD3/RD3	43	AN14/RPE14/PMA1/RE14
9	RPD4/RD4	44	AN15/RPE15/PMA0/RE15
10	AN19/RPG6/VBUSON2/PMA5/RG6	45	VSS
11	AN18/RPG7/1/PMA4/RG7(5)	46	VDD
12	AN17/RPG8//PMA3/RG8(6)	47	AN38/RD14
13	$\overline{\text{MCLR}}$	48	AN39/RD15
14	AN16/RPG9/PMA2/RG9	49	TDI/CDAC3/AN26/RPA8/PMA9/RA8(6)
15	VSS	50	RPB4/PMA8/RB4(5)
16	VDD	51	OA5IN+/CDAC1/AN24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
17	AN22/RG10	52	AN40/RPE0/RE0
18	AN21/RE8	53	AN41/RPE1/RE1
19	AN20/RE9	54	VBUS1
20	AN10/RPA12/RA12	55	VUSB3V3
21	AN9/RPA11/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGED3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGEC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/RF5
27	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/PMA7/RF9	63	OSC1/CLKI/AN49/RPC12/RC12
29	VREF+/AN34/PMA6/RF10	64	OSC2/CLKO/RPC15/RC15
30	AVDD	65	VSS
31	AVSS	66	AN46/RPA14/RA14
32	OA3OUT/AN6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/RPA15/RA15
33	OA3IN-/AN7/C3IN1-/C4IN1-/RPC1/RC1	68	VBAT(7)
34	OA3IN+/AN8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	69	PGED2/RPB5/USBID1/RB5(6)
35	AN11/C1IN2-/PMA12/RC11	70	PGEC2/RPB6/SCK2/PMA15/RB6(5)

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).
7: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

TABLE 1-6: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTG					
RG0	90	—	I/O	ST	PORTG is a bidirectional I/O port
RG1	89	—	I/O	ST	
RG6	10	4	I/O	ST	
RG7	11	5	I/O	ST	
RG8	12	6	I/O	ST	
RG9	14	8	I/O	ST	
RG10	17	—	I/O	ST	
RG11	38	—	I/O	ST	
RG12	96	—	I/O	ST	
RG13	97	—	I/O	ST	
RG14	95	—	I/O	ST	
RG15	1	—	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

4.1.1 BOOT FLASH SEQUENCE AND CONFIGURATION SPACES

Sequence space is used to identify which boot Flash is aliased by aliased regions. If the value programmed into the TSEQ<15:0> bits of the BF1SEQ word is equal to or greater than the value programmed into the TSEQ<15:0> bits of the BF2SEQ word, Boot Flash 1 is aliased by the lower boot alias region, and Boot Flash 2 is aliased by the upper boot alias region. If the TSEQ<15:0> bits of the BF2SEQ word is greater than the TSEQ<15:0> bits of the BF1SEQ word, the opposite is true (see Table 4-2 and Table 4-3 for BFxSEQ word memory locations).

Once boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the Configuration words, DEVSIGN0, DEVCP0, and DEVCFGx. This means that the boot Flash region to be aliased by lower boot alias region memory must contain configuration values in the appropriate memory locations.

Note:	Use only Quad Word program operation (NVMOP<3:0> = `0010`) when programming data into the sequence and configuration spaces.

TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
84E0	SBT1REG5	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84F0	SBT1RD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84F8	SBT1WR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

7.1 Reset Control Registers

TABLE 7-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	PORIO	PORCORE	—	—	—	—	—	—	—	—	—	—	—	—	VBPOR	VBAT	0000
		15:0	—	—	—	—	—	DPSLP	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0000
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	GNMI	---	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	VREGRUN<1:0>		VREGSLP<1:0>		—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 9-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1350	PB6DIV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB7DIV(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1380	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
1390	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	UPLLRDY	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
2: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
3: The PB7DIV register is read-only.

The timer source for each Output Compare module depends on the setting of the OCACLK bit in the CFGCON register, the OC32 bit in the OCxCON register, and the OCTSEL bit in the OCxCON register. The available configurations are shown in Table 19-1.

TABLE 19-1: TIMER SOURCE CONFIGURATIONS

OCx	OCACLK CFGCON<16>	OC32 (OCxCON<5>	OCTSEL OCxCON<3>	Timerx	Timery	Output Compare Timer Source
OC1-OC3	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR4<15:0>	—	TMR4<15:0>
			1	—	TMR5<15:0>	TMR5<15:0>
	1	1	0	TMR4<31:0>	—	TMR4<31:0>
			1	—	TMR4<31:0>	TMR4<31:0>
OC4-OC6, OC13-OC16	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	1	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
OC7-OC9	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR6<15:0>	—	TMR6<15:0>
			1	—	TMR7<15:0>	TMR7<15:0>
	1	1	0	TMR6<31:0>	—	TMR6<31:0>
			1	—	TMR6<31:0>	TMR6<31:0>
OC10-OC12	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR8<15:0>	—	TMR8<15:0>
			1	—	TMR9<15:0>	TMR9<15:0>
	1	1	0	TMR8<31:0>	—	TMR8<31:0>
			1	—	TMR8<31:0>	TMR8<31:0>

REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MASK<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN(1)	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0, HS	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:	HS = Set by hardware	HC = cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **MASK<7:0>:** Address Match Mask bits

These bits are used to mask the ADDR<7:0> bits.

11111111 = Corresponding matching ADDR<7:0> bits are used to detect the address match

Note: This setting allows the user to assign individual address as well as a group broadcast address to a UART.

00000000 = Corresponding ADDRx bits are not used to detect the address match.

See **22.2 "UART Broadcast Mode Example"** for additional information.

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

1 = Corresponding MASKx bits are used to detect the address match.

Note: This setting allows the user to assign individual address as well as a group broadcast address to a UART.

0 = Corresponding MASKx bits are not used to detect the address match.

See **22.2 "UART Broadcast Mode Example"** for additional information.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits

11 = Reserved, do not use
10 = Interrupt is generated and asserted while the transmit buffer is empty
01 = Interrupt is generated and asserted when all characters have been transmitted
00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
1 = UxTX Idle state is '0'
0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
1 = IrDA encoded UxTX Idle state is '1'
0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit

1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON bit (UxMODE<15>) = 1)
0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module and released to the PORT

Note: The event of disabling an enabled receiver will release the RX pin to the PORT function; however, the receive buffers will not be reset. Disabling the receiver has no effect on the receive status flags.

Note 1: This bit should not be enabled until after the ON bit (UxMODE<15>) = 1. If TX interrupts are enabled, setting this bit will immediately cause a TX interrupt based on the value of the UTXISEL bit.

NOTES:

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7280	ADCCMPCON1	31:16	CVDDATA<15:0>																0000
		15:0	—	—	AINID<5:0>						ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
7290	ADCCMPCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
72A0	ADCCMPCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
72B0	ADCCMPCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
7300	ADCBASE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADCBASE<15:0>																0000
7310	ADCDSTAT	31:16	DMAEN	—	RBFIEN5	RBFIEN4	RBFIEN3	RBFIEN2	RBFIEN1	RBFIEN0	WOVERR	—	RBF5	RBF4	RBF3	RBF2	RBF1	RBF0	0000
		15:0	DMACEN	—	RAFIEN5	RAFIEN4	RAFIEN3	RAFIEN2	RAFIEN1	RAFIEN0	—	—	RAF5	RAF4	RAF3	RAF2	RAF1	RAF0	0000
7320	ADCCNTB	31:16	ADCCNTB<31:16>																0000
		15:0	ADCCNTB<15:0>																0000
7330	ADCDMAB	31:16	ADCDMAB<31:16>																0000
		15:0	ADCDMAB<15:0>																0000
7340	ADCTRGSNS	31:16	—	—	—	—	LVL27	LVL26	LVL25	LVL24	LVL23(1)	LVL22(1)	LVL21(1)	LVL20(1)	LVL19	LVL18	LVL17	LVL16	0000
		15:0	LVL15	LVL14	LVL13	LVL12	LVL11	LVL10	LVL9	LVL8	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	0000
7350	ADC0TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7360	ADC1TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7370	ADC2TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7380	ADC3TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7390	ADC4TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
73A0	ADC5TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
73C0	ADCEIEN1	31:16	—	—	—	—	EIEN27	EIEN26	EIEN25	EIEN24	EIEN23(1)	EIEN22(1)	EIEN21(1)	EIEN20(1)	EIEN19	EIEN18	EIEN17	EIEN16	0000
		15:0	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000
73D0	ADCEIEN2	31:16	—	—	—	—	—	—	—	—	—	—	EIRDY53	EIRDY52	—	EIRDY50	EIRDY49	EIRDY48	0000
		15:0	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIEN41(1)	EIEN40(1)	EIEN39(1)	EIEN38(1)	EIEN37(1)	EIEN36(1)	EIEN35(1)	EIEN34(1)	EIEN33(1)	—	0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3 (CONTINUED)

bit 15 **DIFF39:** AN39 Mode bit(1)
1 = Selects AN39 differential input pair as AN39+ and AN1-
0 = AN39 is using Single-ended mode

bit 14 **SIGN39:** AN39 Signed Data Mode bit(1)
1 = AN39 is using Signed Data mode
0 = AN39 is using Unsigned Data mode

bit 13 **DIFF38:** AN38 Mode bit(1)
1 = Selects AN38 differential input pair as AN38+ and AN1-
0 = AN38 is using Single-ended mode

bit 12 **SIGN38:** AN38 Signed Data Mode bit(1)
1 = AN38 is using Signed Data mode
0 = AN38 is using Unsigned Data mode

bit 11 **DIFF37:** AN37 Mode bit(1)
1 = Selects AN37 differential input pair as AN37+ and AN1-
0 = AN37 is using Single-ended mode

bit 10 **SIGN37:** AN37 Signed Data Mode bit(1)
1 = AN37 is using Signed Data mode
0 = AN37 is using Unsigned Data mode

bit 9 **DIFF36:** AN36 Mode bit(1)
1 = Selects AN36 differential input pair as AN36+ and AN1-
0 = AN36 is using Single-ended mode

bit 8 **SIGN36:** AN36 Signed Data Mode bit(1)
1 = AN36 is using Signed Data mode
0 = AN36 is using Unsigned Data mode

bit 7 **DIFF35:** AN35 Mode bit(1)
1 = Selects AN35 differential input pair as AN35+ and AN1-
0 = AN35 is using Single-ended mode

bit 6 **SIGN35:** AN35 Signed Data Mode bit(1)
1 = AN35 is using Signed Data mode
0 = AN35 is using Unsigned Data mode

bit 5 **DIFF34:** AN34 Mode bit(1)
1 = Selects AN34 differential input pair as AN34+ and AN1-
0 = AN34 is using Single-ended mode

bit 4 **SIGN34:** AN34 Signed Data Mode bit(1)
1 = AN34 is using Signed Data mode
0 = AN34 is using Unsigned Data mode

bit 3 **DIFF33:** AN33 Mode bit(1)
1 = Selects AN33 differential input pair as AN33+ and AN1-
0 = AN33 is using Single-ended mode

bit 2 **SIGN33:** AN33 Signed Data Mode bit(1)
1 = AN33 is using Signed Data mode
0 = AN33 is using Unsigned Data mode

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-17: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC
	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CHNLID<4:0>				
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<15:8>							
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<7:0>							

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AFEN:** Digital Filter 'x' Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled and the AFRDY status bit is cleared

bit 30 **DATA16EN:** Filter Significant Data Length bit
1 = All 16 bits of the filter output data are significant
0 = Only the first 12 bits are significant, followed by four zeros
Note: This bit is significant only if DFMODE = 1 (Averaging Mode) and FRACT (ADCCON1<23>) = 1 (Fractional Output Mode).

bit 29 **DFMODE:** ADC Filter Mode bit
1 = Filter 'x' works in Averaging mode
0 = Filter 'x' works in Oversampling Filter mode (default)

bit 28-26 **OVRSAM<2:0>:** Oversampling Filter Ratio bits
If DFMODE is '0':
111 = 128 samples (shift sum 3 bits to right, output data is in 15.1 format)
110 = 32 samples (shift sum 2 bits to right, output data is in 14.1 format)
101 = 8 samples (shift sum 1 bit to right, output data is in 13.1 format)
100 = 2 samples (shift sum 0 bits to right, output data is in 12.1 format)
011 = 256 samples (shift sum 4 bits to right, output data is 16 bits)
010 = 64 samples (shift sum 3 bits to right, output data is 15 bits)
001 = 16 samples (shift sum 2 bits to right, output data is 14 bits)
000 = 4 samples (shift sum 1 bit to right, output data is 13 bits)

If DFMODE is '1':
111 = 256 samples (256 samples to be averaged)
110 = 128 samples (128 samples to be averaged)
101 = 64 samples (64 samples to be averaged)
100 = 32 samples (32 samples to be averaged)
011 = 16 samples (16 samples to be averaged)
010 = 8 samples (8 samples to be averaged)
001 = 4 samples (4 samples to be averaged)
000 = 2 samples (2 samples to be averaged)

bit 25 **AFGIEN:** Digital Filter 'x' Interrupt Enable bit
1 = Digital filter interrupt is enabled and is generated by the AFRDY status bit
0 = Digital filter is disabled

Note 1: This selection is not available on 64-pin devices.

REGISTER 26-7: CxRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVF<15:0>:** FIFOx Receive Overflow Interrupt Pending bit
1 = FIFO has overflowed
0 = FIFO has not overflowed

REGISTER 26-8: CxTMR: CAN TIMER REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits
This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CxCON<20>) is set.

Note 1: CxTMR will be paused when CANCAP = 0.
2: The CxTMR prescaler count will be reset on any write to CxTMR (CANTSPRE will be unaffected).

27.0 OP AMP/COMPARATOR MODULE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 39. "Op amp/Comparator"** (DS60001178), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

Depending on the device, the Op amp/Comparator module consists of a Comparator and Op amp modules. When available, the Op amps can be independently enabled or disabled from the Comparator.

Key features of the Comparator include:

- Differential inputs
- Rail-to-rail operation
- Selectable output and trigger event polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal voltage reference via a 12-bit CDAC output or an external pin
- Output debounce or Digital noise filter with these selectable clocks:
  - Peripheral Bus Clock (PBCLK2)
  - System Clock (SYSCLK)
  - Reference Clock 3 (REFCLK3)
  - PBCLK2/Timer PRx ('x' = 2-5)
  - PWM Secondary Special Event
- Outputs can be internally configured as trigger sources

The following are key features of the Op amps:

- Inverting and non-inverting Inputs and output accessible on pins
- Rail-to-rail operation ($3V \leq AV_{DD} \leq 3.6V$)
- Internal connection to ADC Sample and Hold circuits/SAR cores
- Special voltage follower mode for buffering signals

Please refer to the PIC32MK GP Family Features in **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the actual number of available Op amp/ Comparator modules on your specific device.

Block diagrams of the Op amp/Comparator module are illustrated in Figure 27-1 through Figure 27-5.

Note: The Op amps are disabled by default (i.e., OPAxMD bit in the PMD2 register is equal to '1') on any Reset. Before use or access to any corresponding Op amp, ensure that the OPAxMD bit is equal to '0'.

NOTES:

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A120	ALTDTR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
A130	DTCOMP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A140	TRIG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A150	TRGCON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A160	STRIG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A170	CAP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A180	LEBCON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A190	LEBDLY1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A1A0	AUXCON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A1B0	PTMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A1C0	PWMCON2	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A1D0	IOCON2	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A1E0	PDC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A1F0	SDC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A200	PHASE2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A210	DTR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
A220	ALTDTR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A670	CAP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A680	LEBCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A690	LEBDLY6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A6A0	AUXCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A6B0	PTMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A6C0	PWMCON7	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A6D0	IOCON7	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A6E0	PDC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A6F0	SDC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A700	PHASE7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A710	DTR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
A720	ALTDTR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
A730	DTCOMP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A740	TRIG7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A750	TRGCON7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A760	STRIG7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A770	CAP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

REGISTER 31-23: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger/retrigger the Leading-Edge Blanking counter
0 = Rising edge of PWMxH will not trigger/retrigger the Leading-Edge Blanking counter

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger/retrigger the Leading-Edge Blanking counter
0 = Falling edge of PWMxH will not trigger/retrigger the Leading-Edge Blanking counter

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger/retrigger the Leading-Edge Blanking counter
0 = Rising edge of PWMxL will not trigger/retrigger the Leading-Edge Blanking counter

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger/retrigger the Leading-Edge Blanking counter
0 = Falling edge of PWMxL will not trigger/retrigger the Leading-Edge Blanking counter

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected fault input
0 = Leading-Edge Blanking is not applied to selected fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-0 **Unimplemented:** Read as '0'

REGISTER 32-3: DSGPRX: DEEP SLEEP PERSISTENT GENERAL PURPOSE REGISTER 'x' (x = 0 THROUGH 32)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Deep Sleep Persistent General Purpose bits**

Note: The contents of the DSGPR0 register are retained, even in Deep Sleep and VBAT modes. The DSPGR1 through DSPGR32 registers are disabled by default in Deep Sleep and VBAT modes, but can be enabled with the DSGPREN bit (DSCON<13>). All register bits are reset only in the case of a V_{DD} Power-on Reset (POR) event outside of Deep Sleep mode.

FIGURE 36-18: PARALLEL MASTER PORT READ TIMING DIAGRAM

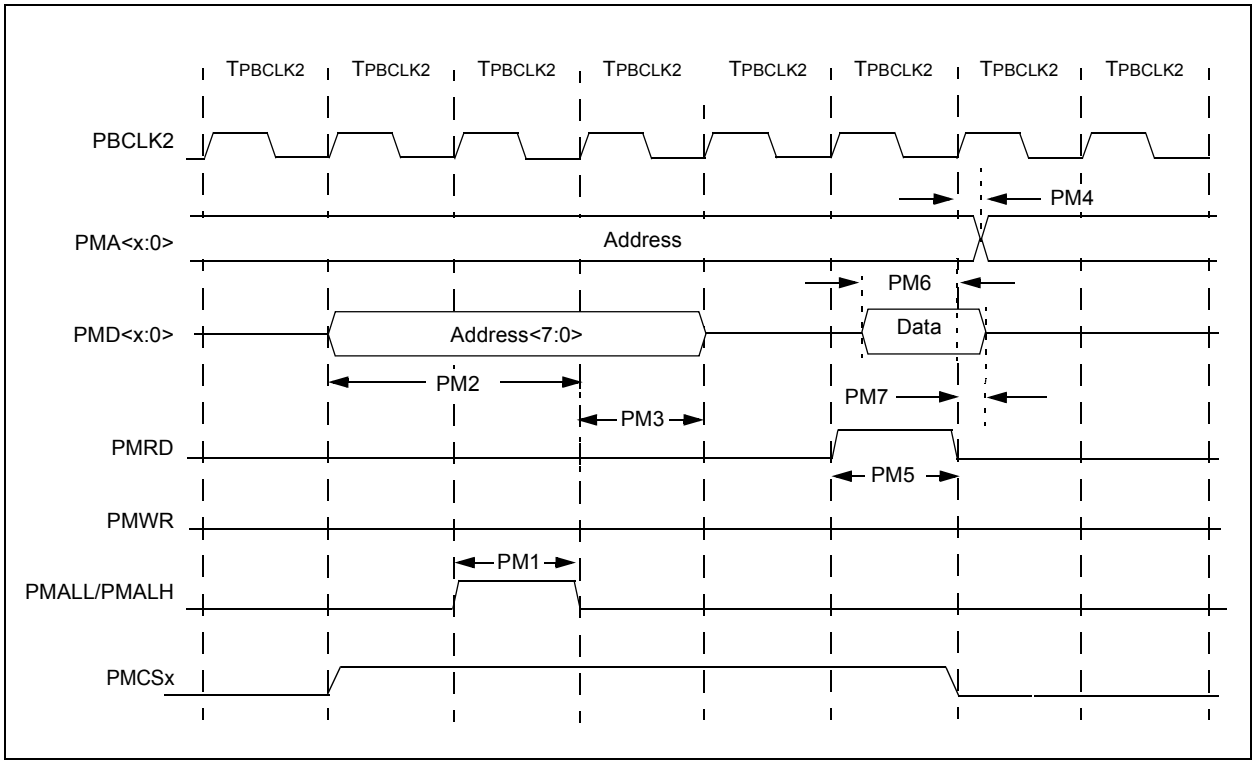

TABLE 36-45: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPBCLK2	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPBCLK2	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.