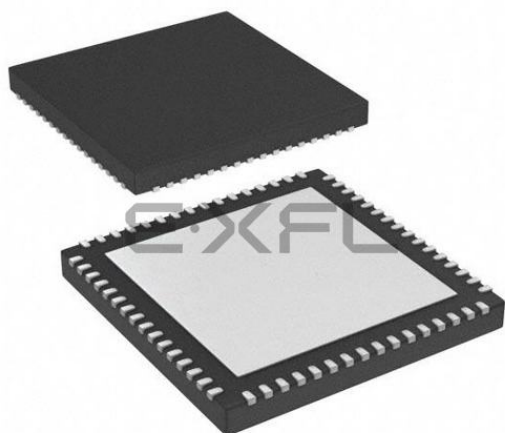




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, WDT
Number of I/O	48
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpd064-i-mr

PIC32MK GP/MC Family

TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

100-PIN TQFP (TOP VIEW)			
PIC32MK0512GPD100 PIC32MK0512GPE100 PIC32MK1024GPD100 PIC32MK1024GPE100		100 1	
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/PMA23/RG15	36	Vss
2	VDD	37	VDD
3	TCK/RPA7/PMD5/RA7	38	AN35/RG11
4	RPB14/VBUSON1/PMD6/RB14	39	AN36/RF13
5	RPB15/PMD7/RB15	40	AN37/RF12
6	RD1	41 ⁽⁶⁾	AN12/C2IN2-/C5IN2-/PMA11/RE12
7	RD2	42 ⁽⁵⁾	AN13/C3IN2-/PMA10/RE13
8	RPD3/RD3	43	AN14/RPE14/PMA1/RE14
9	RPD4/RD4	44	AN15/RPE15/PMA0/RE15
10	AN19/RPG6/VBUSON2/PMA5/RG6	45	Vss
11	AN18/RPG7/1/PMA4/RG7 ⁽⁵⁾	46	VDD
12	AN17/RPG8//PMA3/RG8 ⁽⁶⁾	47	AN38/RD14
13	MCLR	48	AN39/RD15
14	AN16/RPG9/PMA2/RG9	49	TDI/CDAC3/AN26/RPA8/PMA9/RA8 ⁽⁶⁾
15	Vss	50	RPB4/PMA8/RB4 ⁽⁵⁾
16	VDD	51	OA5IN+/CDAC1/AN24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
17	AN22/RG10	52	AN40/RPE0/RE0
18	AN21/RE8	53	AN41/RPE1/RE1
19	AN20/RE9	54	VBUS1
20	AN10/RPA12/RA12	55	VUSB3V3
21	AN9/RPA11/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGED3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGEC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/RF5
27	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/PMA7/RF9	63	OSC1/CLKI/AN49/RPC12/RC12
29	VREF+/AN34/PMA6/RF10	64	OSC2/CLKO/RPC15/RC15
30	AVDD	65	Vss
31	AVss	66	AN46/RPA14/RA14
32	OA3OUT/AN6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/RPA15/RA15
33	OA3IN-/AN7/C3IN1-/C4IN1-/RPC1/RC1	68	VBAT ⁽⁷⁾
34	OA3IN+/AN8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	69	PGED2/RPB5/USBID1/RB5 ⁽⁶⁾
35	AN11/C1IN2-/PMA12/RC11	70	PGEC2/RPB6/SCK2/PMA15/RB6 ⁽⁵⁾

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 “Peripheral Pin Select (PPS)”** for restrictions.
 - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
 - 5: The I²C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I²C master/slave clock. (i.e., SCL).
 - 6: The I²C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I²C data I/O. (i.e., SDA).
 - 7: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

PIC32MK GP/MC Family

TABLE 1-14: USB1 AND USB2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/TQFP			
VUSB3V3	55	35	P	—	USB internal transceiver supply. This pin should be connected to VDD.
VBUS1	54	34	I	Analog	USB1 Bus Power Monitor
VBUSON1	4	2	O	CMOS	USB1 Vbus Power Control Output
VBUSON2	10	—	O	CMOS	USB2 Vbus Power Control Output
D1+	57	37	I/O	Analog	USB1 D+
D1-	56	36	I/O	Analog	USB1 D-
USBID1	69	43	I	ST	USB1 OTG ID Detect
VBUS2	58	—	I	Analog	USB2 Bus Power Monitor
D2+	60	—	I/O	Analog	USB2 D+
D2-	59	—	I/O	Analog	USB2 D-
USBID2	77	—	I	ST	USB2 OTG ID detect

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

TABLE 1-15: CTMU PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/TQFP			
CTED1	25	16	I	ST	CTMU External Edge Input 1
CTED2	24	15	I	ST	CTMU External Edge Input 2
CTCMP	27	18	I	Analog	CTMU external capacitor input for pulse generation
CTPLS	PPS	PPS	O	CMOS	CTMU Pulse Generator Output

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

TABLE 1-16: CDAC1 THROUGH CDAC3 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/TQFP			
CDAC1	51	33	O	Analog	12-bit CDAC1 output
CDAC2	71	45	O	Analog	12-bit CDAC2 output
CDAC3	49	31	O	Analog	12-bit CDAC3 output

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MK GP/MC Family

TABLE 1-20: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/TQFP			
Power and Ground					
AVDD	30	19	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	31	20	P	P	Ground reference for analog modules. This pin must be connected at all times.
VDD	2, 16, 37, 46, 62, 86	10, 26, 38, 57	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VSS	15, 36, 45, 65, 75, 85	9, 25, 41, 56	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
VBAT ⁽¹⁾	68	42	P	P	Battery backup for selected peripherals; otherwise connect to VDD.
Voltage Reference					
VREF+	29	16	I	Analog	Analog Voltage Reference (High) Input
VREF-	28	15	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

Note 1: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

8.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Interrupt Controller”** (DS60001108) and **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **8.1 “CPU Exceptions”**.

The Interrupt Controller module includes the following features:

- Up to 216 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Two shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Table 8-1 provides Interrupt Service routine (ISR) latency information.

TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 40	_ADC_DATA40_VECTOR	146	OFF146<17:1>	IFS4<18>	IEC4<18>	IPC36<20:18>	IPC36<17:16>	Yes
ADC Data 41	_ADC_DATA41_VECTOR	147	OFF147<17:1>	IFS4<19>	IEC4<19>	IPC36<28:26>	IPC36<25:24>	Yes
Reserved	—	148	—	—	—	—	—	—
Reserved	—	149	—	—	—	—	—	—
Reserved	—	150	—	—	—	—	—	—
ADC Data 45	_ADC_DATA45_VECTOR	151	OFF151<17:1>	IFS4<23>	IEC4<23>	IPC37<28:26>	IPC37<25:24>	Yes
ADC Data 46	_ADC_DATA46_VECTOR	152	OFF152<17:1>	IFS4<24>	IEC4<24>	IPC38<4:2>	IPC38<1:0>	Yes
ADC Data 47	_ADC_DATA47_VECTOR	153	OFF153<17:1>	IFS4<25>	IEC4<25>	IPC38<12:10>	IPC38<9:8>	Yes
ADC Data 48	_ADC_DATA48_VECTOR	154	OFF154<17:1>	IFS4<26>	IEC4<26>	IPC38<20:18>	IPC38<17:16>	Yes
ADC Data 49	_ADC_DATA49_VECTOR	155	OFF155<17:1>	IFS4<27>	IEC4<27>	IPC38<28:26>	IPC38<25:24>	Yes
ADC Data 50	_ADC_DATA50_VECTOR	156	OFF156<17:1>	IFS4<28>	IEC4<28>	IPC39<4:2>	IPC39<1:0>	Yes
ADC Data 51	_ADC_DATA51_VECTOR	157	OFF157<17:1>	IFS4<29>	IEC4<29>	IPC39<12:10>	IPC39<9:8>	Yes
ADC Data 52	_ADC_DATA52_VECTOR	158	OFF158<17:1>	IFS4<30>	IEC4<30>	IPC39<20:18>	IPC39<17:16>	Yes
ADC Data 53	_ADC_DATA53_VECTOR	159	OFF159<17:1>	IFS4<31>	IEC4<31>	IPC39<28:26>	IPC39<25:24>	Yes
Comparator 3 Interrupt	_COMPARATOR_3_VECTOR	160	OFF160<17:1>	IFS5<0>	IEC5<0>	IPC40<4:2>	IPC40<1:0>	Yes
Comparator 4 Interrupt	_COMPARATOR_4_VECTOR	161	OFF161<17:1>	IFS5<1>	IEC5<1>	IPC40<12:10>	IPC40<9:8>	Yes
Comparator 5 Interrupt	_COMPARATOR_5_VECTOR	162	OFF162<17:1>	IFS5<2>	IEC5<2>	IPC40<20:18>	IPC40<17:16>	Yes
Reserved	—	163	—	—	—	—	—	—
UART6 Fault	_UART6_FAULT_VECTOR	164	OFF164<17:1>	IFS5<4>	IEC5<4>	IPC41<4:2>	IPC41<1:0>	Yes
UART6 Receive Done	_UART6_RX_VECTOR	165	OFF165<17:1>	IFS5<5>	IEC5<5>	IPC41<12:10>	IPC41<9:8>	Yes
UART6 Transfer Done	_UART6_TX_VECTOR	166	OFF166<17:1>	IFS5<6>	IEC5<6>	IPC41<20:18>	IPC41<17:16>	Yes
CAN1 Global Interrupt	_CAN1_VECTOR	167	OFF167<17:1>	IFS5<7>	IEC5<7>	IPC41<28:26>	IPC41<25:24>	Yes
CAN2 Global Interrupt	_CAN2_VECTOR	168	OFF168<17:1>	IFS5<8>	IEC5<8>	IPC42<4:2>	IPC42<1:0>	Yes
QEI1 Interrupt	_QE11_VECTOR	169	OFF169<17:1>	IFS5<9>	IEC5<9>	IPC42<12:10>	IPC42<9:8>	Yes
QEI2 Interrupt	_QE12_VECTOR	170	OFF170<17:1>	IFS5<10>	IEC5<10>	IPC42<20:18>	IPC42<17:16>	Yes
PWM Primary Event	_PWM_PRI_VECTOR	171	OFF171<17:1>	IFS5<11>	IEC5<11>	IPC42<28:26>	IPC42<25:24>	Yes
PWM Sec Event	_PWM_SEC_VECTOR	172	OFF172<17:1>	IFS5<12>	IEC5<12>	IPC43<4:2>	IPC43<1:0>	Yes
PWM1 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM1_VECTOR	173	OFF173<17:1>	IFS5<13>	IEC5<13>	IPC43<12:10>	IPC43<9:8>	Yes
PWM2 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM2_VECTOR	174	OFF174<17:1>	IFS5<14>	IEC5<14>	IPC43<20:18>	IPC43<17:16>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MK General Purpose (GP) Family Features”** for the list of available peripherals.

Note 2: This interrupt source is not available on 64-pin devices.

Note 3: This interrupt source is not available on 100-pin devices.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See 13.2 “CLR, SET, and INV Registers” for more information.
- 2: This bit is not available on 64-pin devices.
- 3: This bit is not available on devices without a CAN module.
- 4: This bit is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.
- 7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 11-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DMAADDR<31:0>**: DMA Module Address bits

These bits contain the address of the most recent DMA access when an error was detected.

Note: The DMAADDR register will be cleared when its contents are read. If more than one errors at the same time, the read transaction will be recorded. Additional transfers that occur later with an error will not update this register until it has been read or cleared.

TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1500	IC12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC12R<3:0>				0000
1504	IC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC13R<3:0>				0000
1508	IC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC14R<3:0>				0000
150C	IC15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC15R<3:0>				0000
1510	IC16R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC16R<3:0>				0000
1514	SCK5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK5R<3:0>				
1518	SDI5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
151C	SS5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
1520	SCK6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK6R<3:0>				
1524	SDI6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000
1528	SS6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
152C	C3RXR ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C3RXR<3:0>				0000
1530	C4RXR ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C4RXR<3:0>				0000
1534	QEA3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA3R<3:0>				0000
1538	QEB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: This register is not available on 64-pin devices.
 - 2: This register is not available on devices without a CAN module.
 - 3: This register is only available on PIC32MKXXXGPEXXX devices.

FIGURE 25-1: ADC BLOCK DIAGRAM

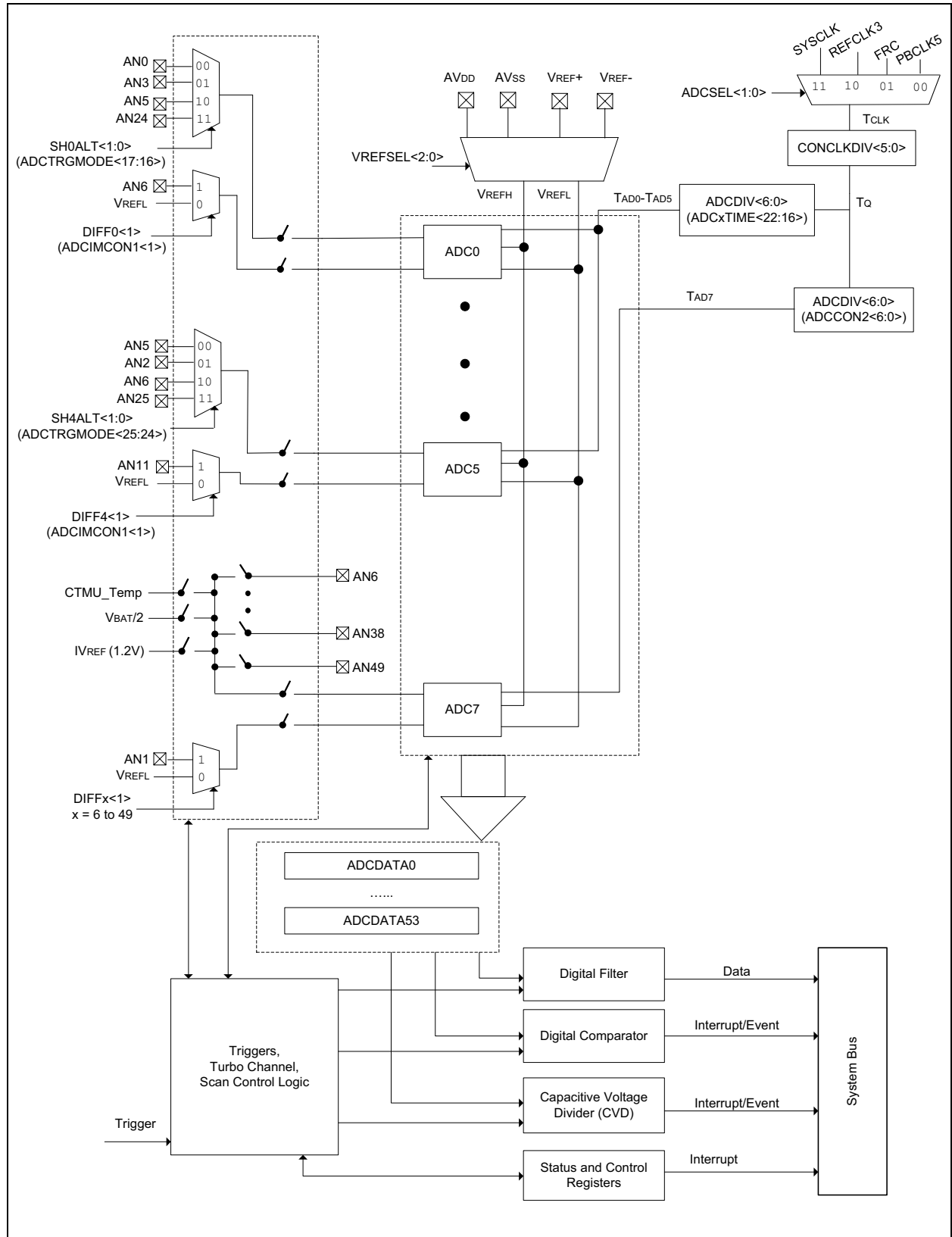


TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
73E0	ADCEISTAT1	31:16	—	—	—	—	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23 ⁽¹⁾	EIRDY22 ⁽¹⁾	EIRDY21 ⁽¹⁾	EIRDY20 ⁽¹⁾	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
73F0	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	EIRDY53	EIRDY52	—	EIRDY50	EIRDY49	EIRDY48	0000
		15:0	EIRDY47 ⁽¹⁾	EIRDY46 ⁽¹⁾	EIRDY45 ⁽¹⁾	—	—	—	EIRDY41 ⁽¹⁾	EIRDY40 ⁽¹⁾	EIRDY39 ⁽¹⁾	EIRDY38 ⁽¹⁾	EIRDY37 ⁽¹⁾	EIRDY36 ⁽¹⁾	EIRDY35 ⁽¹⁾	EIRDY34 ⁽¹⁾	EIRDY33 ⁽¹⁾	—	0000
7400	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	WKIEN5	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	WKRDY5	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	ANEN5	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
7600	ADCDATA0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7610	ADCDATA1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7620	ADCDATA2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7630	ADCDATA3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7640	ADCDATA4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7650	ADCDATA5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7660	ADCDATA6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7670	ADCDATA7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7680	ADCDATA8	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7690	ADCDATA9	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76A0	ADCDATA10	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76B0	ADCDATA11	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76C0	ADCDATA12	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76D0	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note

- 1: This bit or register is not available on 64-pin devices.
- 2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor).
- 3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBF45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCSEL<1:0>		CONCLKDIV<5:0>					
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIGEN7	—	DIGEN5	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R-0, HS, HC
	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP ^(1,2,3,4)	RQCNVRT
7:0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GLSWTRG	GSWTRG	ADINSEL<5:0>					

Legend:	HC = Hardware Set	HS = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-30 **ADCSEL<1:0>**: Analog-to-Digital Clock Source (TCLK) bits

11 = SYSCLK
10 = REFCLK3
01 = FRC
00 = PBCLK5

bit 29-24 **CONCLKDIV<5:0>**: Analog-to-Digital Control Clock (Tq) Divider bits

111111 = 126 * TCLK = Tq
.
.
.
000011 = 6 * TCLK = Tq
000010 = 4 * TCLK = Tq
000001 = 2 * TCLK = Tq
000000 = TCLK = Tq

bit 23 **DIGEN7**: Shared ADC (ADC7) Digital Enable bit

1 = ADC7 is digital enabled
0 = ADC7 is digital disabled

bit 22 **Unimplemented**: Read as '0'

bit 21 **DIGEN5**: ADC5 Digital Enable bit

1 = ADC5 is digital enabled (required for active operation)
0 = ADC5 is digital disabled (power-saving mode)

bit 20 **DIGEN4**: ADC4 Digital Enable bit

1 = ADC4 is digital enabled (required for active operation)
0 = ADC4 is digital disabled (power-saving mode)

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

- The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.
- The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.
- Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

26.1 Control Registers

TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
0000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480		
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000		
0010	C1CFG	31:16	—	—	—	—	—	—	—	—	WAKFIL		—	—	SEG2PH<2:0>				0000		
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>					0000			
0020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000		
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000		
0030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	FILHIT<4:0>				—	ICODE<6:0>							0040			
0040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000		
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000		
0050	C1FSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000		
0060	C1RXOVF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000		
0070	C1TMR	31:16	CANTS<15:0>																0000		
		15:0	CANTSPRE<15:0>																0000		
0080	C1RXM0	31:16	SID<10:0>													—	MIDE	—		EID<17:16>	xxxx
		15:0	EID<15:0>																		
0090	C1RXM1	31:16	SID<10:0>													—	MIDE	—		EID<17:16>	xxxx
		15:0	EID<15:0>																		
00A0	C1RXM2	31:16	SID<10:0>													—	MIDE	—		EID<17:16>	xxxx
		15:0	EID<15:0>																		
00B0	C1RXM3	31:16	SID<10:0>													—	MIDE	—		EID<17:16>	xxxx
		15:0	EID<15:0>																		
00C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>			FSEL3<4:0>				FLTEN2	MSEL2<1:0>			FSEL2<4:0>				0000		
		15:0	FLTEN1	MSEL1<1:0>			FSEL1<4:0>				FLTEN0	MSEL0<1:0>			FSEL0<4:0>				0000		
00D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>			FSEL7<4:0>				FLTEN6	MSEL6<1:0>			FSEL6<4:0>				0000		
		15:0	FLTEN5	MSEL5<1:0>			FSEL5<4:0>				FLTEN4	MSEL4<1:0>			FSEL4<4:0>				0000		
00E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>			FSEL11<4:0>				FLTEN10	MSEL10<1:0>			FSEL10<4:0>				0000		
		15:0	FLTEN9	MSEL9<1:0>			FSEL9<4:0>				FLTEN8	MSEL8<1:0>			FSEL8<4:0>				0000		
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>			FSEL15<4:0>				FLTEN14	MSEL14<1:0>			FSEL14<4:0>				0000		
		15:0	FLTEN13	MSEL13<1:0>			FSEL13<4:0>				FLTEN12	MSEL12<1:0>			FSEL12<4:0>				0000		
0140	C1RXFn (n = 0-15)	31:16	SID<10:0>													—	EXID	—		EID<17:16>	xxxx
		15:0	EID<15:0>																		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 “CLR, SET, and INV Registers”** for more information.

PIC32MK GP/MC Family

REGISTER 26-17: CxFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n'
(‘x’ = 1-4); n’ = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF ⁽¹⁾	TXHALFIF	TXEMPTYIF ⁽¹⁾
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF ⁽¹⁾	RXHALFIF ⁽¹⁾	RXNEMPTYIF ⁽¹⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit

1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit

1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit

1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as ‘0’

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit

1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit

1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit

1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit

1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit⁽¹⁾

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads ‘0’

Note 1: This bit is read-only and reflects the status of the FIFO.

27.8 Op amp/Comparator Control Registers

TABLE 27-2: OP AMP/COMPARATOR REGISTER MAP

Virtual Address (BF82)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT	0000
C010	CM1CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>		CFLTREN	CFDIV<2:0>			0000	
		15:0	ON	COE	CPOL	—	OA0	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	0000	
C020	CM1MSKCON ⁽²⁾	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C030	CM2CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>		CFLTREN	CFDIV<2:0>			0000	
		15:0	ON	COE	CPOL	—	OA0	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	0000	
C040	CM2MSKCON ⁽²⁾	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C050	CM3CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>		CFLTREN	CFDIV<2:0>			0000	
		15:0	ON	COE	CPOL	—	OA0	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	0000	
C060	CM3MSKCON ⁽²⁾	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C070	CM4CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>		CFLTREN	CFDIV<2:0>			0000	
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	0000	
C080	CM4MSKCON ⁽²⁾	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C090	CM5CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>		CFLTREN	CFDIV<2:0>			0000	
		15:0	ON	COE	CPOL	—	OA0	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	0000	
C0A0	CM5MSKCON ⁽²⁾	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See 13.2 “CLR, SET, and INV Registers” for more information.
- 2: This register is only available on PIC32MKXXMCXX devices.

PIC32MK GP/MC Family

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLSRC<3:0> ^(2,4)				CLPOL ^(2,4)	CLMOD ^(2,4)
23:16	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
	—	FLTSRC<3:0> ^(2,4)				FLTPOL ⁽²⁾	FLTMOD<1:0> ⁽⁴⁾	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PENH ⁽¹⁾	PENL ⁽¹⁾	POLH ⁽²⁾	POLL ⁽²⁾	PMOD<1:0> ⁽²⁾		OVRENH	OVRENL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	OVRDAT<1:0> ⁽³⁾		FLTDAT<1:0> ^(2,3)		CLDAT<1:0>		SWAP	OSYNC

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLT_x inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLT_x pin. In addition, DTCMP functions are fixed to specific FLT_x inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;           //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;              //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;        //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;             //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;       //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;           //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;              //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;        //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;             //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;       //Enable Fault for PWM1 on FLT3 pin
```

PIC32MK GP/MC Family

REGISTER 31-25: AUXCONx: PWM AUXILIARY CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CHOPSEL<3:0> ⁽¹⁾				CHOPHEN	CHOPLEN

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWM Chop Clock Source Select bits⁽¹⁾

The selected signal will enable and disable (CHOP) the selected PWM outputs.

1111 = Reserved. Do not use

1110 = Reserved. Do not use

1101 = Reserved. Do not use

1100 = PWM12H selected as CHOP clock source

.

.

.

0111 = PWM7H selected as CHOP clock source

.

.

.

0001 = PWM1H selected as CHOP clock source

0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled

0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled

0 = PWMxL chopping function is disabled

Note 1: This bit should be changed only when the PTEN bit (PTCON<15>) = 0.

33.2 Registers

TABLE 33-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3FC0	DEVCFG3	31:16	FVBUSIO1	FUSBIDIO1	IOL1WAY	PMDL1WAY	PGL1WAY	—	—	—	FVBUSIO2	FUSBIDIO2	—	PWMLOCK	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
3FC4	DEVCFG2	31:16	UPLLEN	—	BORSEL	FDSSEN	DSWDTEN	DSWDT OSC	DSWDTPS<4:0>					DSBOREN	VBAT BOREN	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>						FPLLICK	FPLLRNG<2:0>			—	FPLLDIV<2:0>			xxxx	
3FC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>				FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>						xxxx
		15:0	FCKSM<1:0>		—	—	—	—	OSCI OFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>		xxxx
3FCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	—	—	—	—	—	—	POSC BOOST	POSCGAIN<1:0>		SOSC BOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>				—	FSLEEP	—	—	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>	
3FDC	DEVCP	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
3FEC	DEVSIGN	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 33-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽²⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	ADCPRI	—	—	PWMAPIN6	PWMAPIN5	PWMAPIN4	PWMAPIN3	PWMAPIN2	PWMAPIN1	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	—	IOANCPEN	—	—	—	JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>						DEVID<27:16>										XXXX
		15:0	DEVID<15:0>																XXXX
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00E0	CFGPG	31:16	—	—	—	—	—	—	ADCPG<1:0>		FCPG<1:0>		—	—	CAN4PG<1:0>		CAN3PG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		USB2PG<1:0>		USB1PG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000
0110	CFGCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	ENPGA5	—	ENPGA3	ENPGA2	ENPGA1	0000
		15:0	—	—	—	—	—	—	—	—	EEWS<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See 13.2 "CLR, SET, and INV Registers" for more information.
 - 2: Reset values are dependent on the specific device.
 - 3: This register is not available on 64-pin devices.

35.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

35.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

35.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

35.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

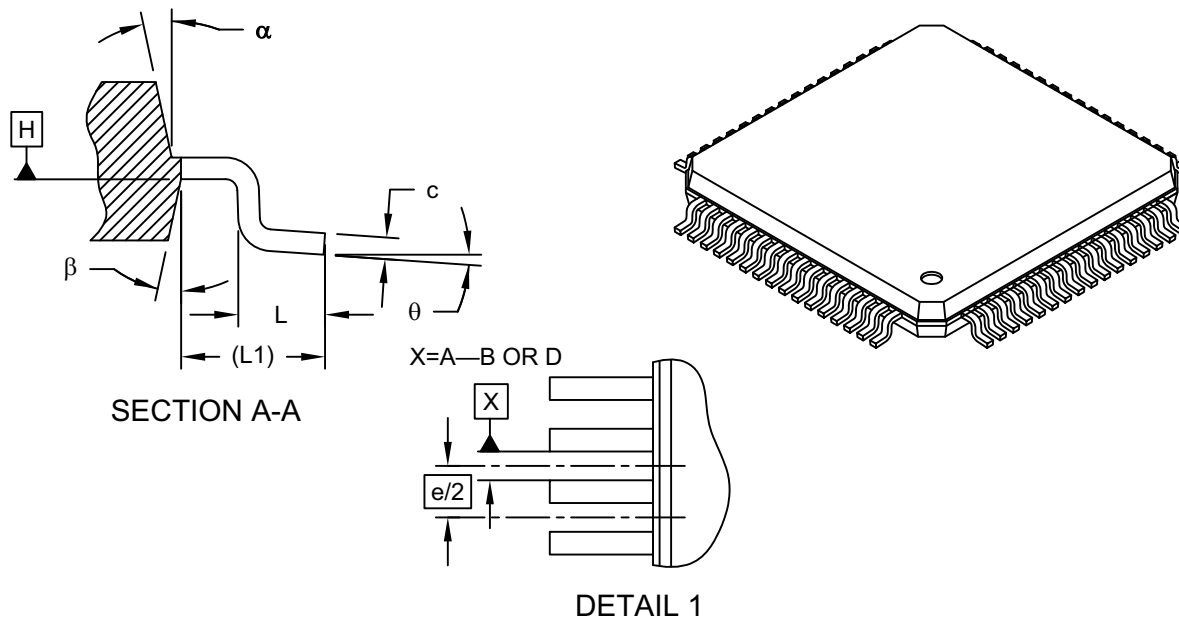
35.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

PIC32MK GP/MC Family

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

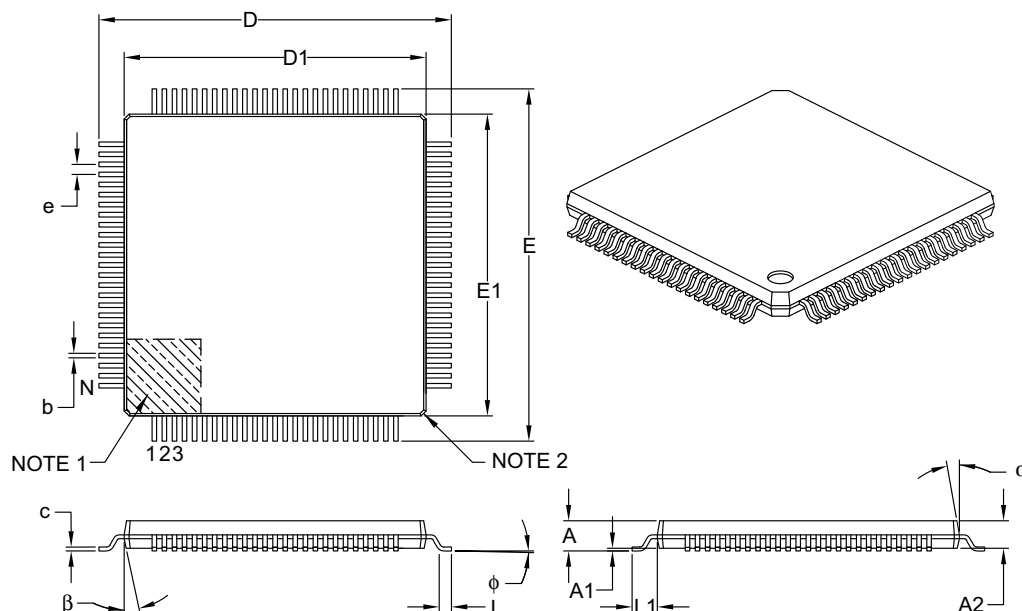
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

PIC32MK GP/MC Family

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packages>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.40 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D	14.00 BSC		
Molded Package Width	E1	12.00 BSC		
Molded Package Length	D1	12.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B