What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpd064-i-pt

TABLE 1-9: **TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Timer1 through Timer9					
T1CK	51	33	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar					
RTCC	27	18	O	—	Real-Time Clock Alarm/Seconds Output (not in VBAT power domain, requires V_{DD}

Legend: CMOS = CMOS-compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
TTL = Transistor-transistor Logic input buffer   PPS = Peripheral Pin Select

2.4 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS50001765
- *"MPLAB® ICD 3 Design Advisory"* DS50001764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) DS50001749

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.6 Trace

When present on select pin counts, the trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3:   **SUGGESTED OSCILLATOR CIRCUIT PLACEMENT**
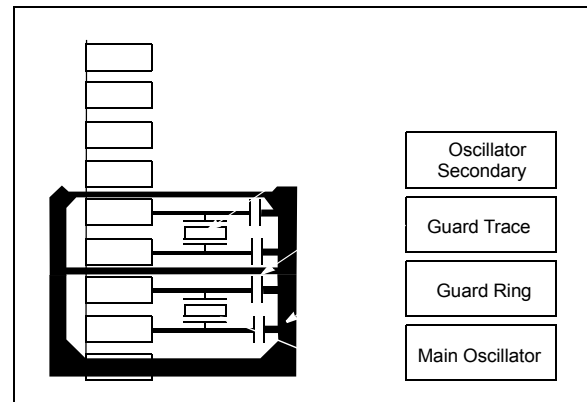
TABLE 3-3: **COPROCESSOR 0 REGISTERS (CONTINUED)**

Register Number	Register Name	Function
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	Reserved	Reserved in the PIC32MK GP Family core.
18	Reserved	Reserved in the PIC32MK GP Family core.
19	Reserved	Reserved in the PIC32MK GP Family core.
20-22	Reserved	Reserved in the PIC32MK GP Family core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	Reserved	Reserved in the PIC32MK GP Family core.
27	Reserved	Reserved in the PIC32MK GP Family core.
28	Reserved	Reserved in the PIC32MK GP Family core.
29	Reserved	Reserved in the PIC32MK GP Family core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

PIC32MK GP/MC Family

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
063C	OFF063	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0640	OFF064	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0644	OFF065	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0648	OFF066	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
064C	OFF067	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0650	OFF068	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0654	OFF069	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0658	OFF070	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
065C	OFF071	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0660	OFF072	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0664	OFF073	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0668	OFF074	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
066C	OFF075	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000
0670	OFF076	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0							VOFF<15:1>									—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
07A8	OFF154	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07AC	OFF155	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 9-7: **PBxDIV: PERIPHERAL BUS 'x' CLOCK DIVISOR CONTROL REGISTER ('x' = 1-7)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	R-1	U-0	U-0	U-0
	ON[1]	—	—	—	PBDIVRDY	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1[2]
	—	PBDIV<6:0>						

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Peripheral Bus 'x' Output Clock Enable bit[1]

1 = Output clock is enabled
0 = Output clock is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **PBDIVRDY:** Peripheral Bus 'x' Clock Divisor Ready bit

1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written
0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-7 **Unimplemented:** Read as '0'

bit 6-0 **PBDIV<6:0>:** Peripheral Bus 'x' Clock Divisor Control bits

1111111 = PBCLKx is SYSCLK divided by 128
1111110 = PBCLKx is SYSCLK divided by 127

•
•
•

0000011 = PBCLKx is SYSCLK divided by 4 (default value for x = 6)
0000010 = PBCLKx is SYSCLK divided by 3
0000001 = PBCLKx is SYSCLK divided by 2 (default value for x < 6)
0000000 = PBCLKx is SYSCLK divided by 1 (default value for x = 7)

Note 1: The clock for Peripheral Bus 1 and Peripheral Bus 7 cannot be turned off. Therefore, the ON bit in the PB1DIV register and the PB7DIV register cannot be written as a '0'.

2: The default value for CPU clock PB7DIV Lsb = 0, where PB7CLK = SYSCLK (PB7DIV is read-only).

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 12-8: **UxEIR: USB ERROR INTERRUPT STATUS REGISTER ('x' = 1 AND 2)**

bit 1   **CRC5EF:** CRC5 Host Error Flag bit[4]

1 = Token packet rejected due to CRC5 error
0 = Token packet accepted

EOFEF: EOF Error Flag bit[3,5]

1 = EOF error condition detected
0 = No EOF error condition

bit 0   **PIDEF:** PID Check Failure Flag bit

1 = PID check failed
0 = PID check passed

Note 1:   This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2:   This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3:   This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4:   Device mode.

5:   Host mode.

TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
16D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD4R<4:0>					0000
16D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD5R<4:0>					0000
16D8	RPD6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD6R<4:0>					0000
1700	RPE0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE0R<4:0>					0000
1704	RPE1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE1R<4:0>					0000
1738	RPE14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF14R<4:0>					0000
173C	RPE15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE15R<4:0>					0000
1740	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF0R<4:0>					0000
1744	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF1R<4:0>					0000
1780	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG0R<4:0>					0000
1784	RPG1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG1R<4:0>					0000
1798	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG6R<4:0>					0000
179C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG7R<4:0>					0000
17A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG8R<4:0>					0000
17A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG9R<4:0>					0000
17B0	RPG12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG12R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 13-1: **[*pin name*]R: PERIPHERAL PIN SELECT INPUT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[*pin name*]R<3:0>			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-4   **Unimplemented:** Read as '0'

bit 3-0   **[*pin name*]R<3:0>:** Peripheral Pin Select Input bits
Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table 13-1 for input pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

REGISTER 13-2: **RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RPnR<4:0>				

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-5   **Unimplemented:** Read as '0'

bit 4-0   **RPnR<4:0>:** Peripheral Pin Select Output bits
See Table 13-2 for output pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

15.2 Timer2-Timer9 Control Registers

TABLE 15-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF82_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	TMR2<31:16>																0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	PR2<31:16>																FFFF
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0410	TMR3	31:16	TMR3<31:16>																0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	PR3<31:16>																FFFF
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	TMR4<31:16>																0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	PR4<31:16>																FFFF
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0810	TMR5	31:16	TMR5<31:16>																0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	PR5<31:16>																FFFF
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	TMR6<31:16>																0000
		15:0	TMR6<15:0>																0000
0A20	PR6	31:16	PR6<31:16>																FFFF
		15:0	PR6<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7100	ADCCMPEN2	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23[1]	CMPE22[1]	CMPE21[1]	CMPE20[1]	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
7110	ADCCMP2	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
7120	ADCCMPEN3	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23[1]	CMPE22[1]	CMPE21[1]	CMPE20[1]	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
7130	ADCCMP3	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
7140	ADCCMPEN4	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23[1]	CMPE22[1]	CMPE21[1]	CMPE20[1]	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
7150	ADCCMP4	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
71A0	ADCFLTR1	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
71B0	ADCFLTR2	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
71C0	ADCFLTR3	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
71D0	ADCFLTR4	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
7200	ADCTRG1	31:16	—	—	—	TRGSRC3<4:0>					—	—	—	TRGSRC2<4:0>					0000
		15:0	—	—	—	TRGSRC1<4:0>					—	—	—	TRGSRC0<4:0>					0000
7210	ADCTRG2	31:16	—	—	—	TRGSRC7<4:0>					—	—	—	TRGSRC6<4:0>					0000
		15:0	—	—	—	TRGSRC5<4:0>					—	—	—	TRGSRC4<4:0>					0000
7220	ADCTRG3	31:16	—	—	—	TRGSRC11<4:0>					—	—	—	TRGSRC10<4:0>					0000
		15:0	—	—	—	TRGSRC9<4:0>					—	—	—	TRGSRC8<4:0>					0000
7230	ADCTRG4	31:16	—	—	—	TRGSRC15<4:0>					—	—	—	TRGSRC14<4:0>					0000
		15:0	—	—	—	TRGSRC13<4:0>					—	—	—	TRGSRC12<4:0>					0000
7240	ADCTRG5	31:16	—	—	—	TRGSRC19<4:0>[1]					—	—	—	TRGSRC18<4:0>					0000
		15:0	—	—	—	TRGSRC17<4:0>					—	—	—	TRGSRC16<4:0>					0000
7250	ADCTRG6[1]	31:16	—	—	—	TRGSRC23<4:0>					—	—	—	TRGSRC22<4:0>					0000
		15:0	—	—	—	TRGSRC21<4:0>					—	—	—	TRGSRC20<4:0>					0000
7260	ADCTRG7	31:16	—	—	—	TRGSRC27<4:0>					—	—	—	TRGSRC26<4:0>					0000
		15:0	—	—	—	TRGSRC25<4:0>					—	—	—	TRGSRC24<4:0>					0000

Note 1: This bit or register is not available on 64-pin devices.

2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor).

3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-8:   ADCIMCON4: ADC INPUT MODE CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DIFF49	SIGN49	DIFF48	SIGN48

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-4   **Unimplemented:** Read as '0'

bit 3   **DIFF49:** AN49 Mode bit

1 = Selects AN49 differential input pair as AN49+ and AN1-

0 = AN49 is using Single-ended mode

bit 2   **SIGN49:** AN41 Signed Data Mode bit

1 = AN49 is using Signed Data mode

0 = AN49 is using Unsigned Data mode

bit 1   **DIFF48:** AN48 Mode bit

1 = Selects AN40 differential input pair as AN48+ and AN1-

0 = AN48 is using Single-ended mode

bit 0   **SIGN48:** AN48 Signed Data Mode bit

1 = AN48 is using Signed Data mode

0 = AN48 is using Unsigned Data mode

NOTES:

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 29-26   **CLSRC<3:0>:** Current-Limit Control Signal Source select bit for PWM Generator 'x'[2,4]

These bits specify the current-limit control signal source.

1111 = FLT15
1110 = Reserved
1101 = Reserved
1100 = Comparator 5
1011 = Comparator 4
1010 = Comparator 3
1001 = Comparator 2
1000 = Comparator 1
0111 = FLT8
0110 = FLT7
0101 = FLT6
0100 = FLT5
0011 = FLT4
0010 = FLT3
0001 = FLT2
0000 = FLT1

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)
```
PWMCON1bits.DTC = 0b11;        //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;          //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;     //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;         //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;    //Enable Fault for PWM1 on FLT8 pin
```
Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)
```
PWMCON1bits.DTC = 0b11;        //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;          //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;     //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;         //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;    //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 32-3: **DSGPRX: DEEP SLEEP PERSISTENT GENERAL PURPOSE REGISTER 'x'
(x = 0 THROUGH 32)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-0   **Deep Sleep Persistent General Purpose bits**

Note: The contents of the DSGPR0 register are retained, even in Deep Sleep and VBAT modes. The DSPGR1 through DSPGR32 registers are disabled by default in Deep Sleep and VBAT modes, but can be enabled with the DSGPREN bit (DSCON<13>). All register bits are reset only in the case of a V$_{DD}$ Power-on Reset (POR) event outside of Deep Sleep mode.

REGISTER 33-8: **CFGPG: PERMISSION GROUP CONFIGURATION REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ADCPG<1:0>	
23:16	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCPG<1:0>		—	—	CAN4PG<1:0>		CAN3PG<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAN2PG<1:0>		CAN1PG<1:0>		USB2PG<1:0>		USB1PG<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	DMAPG<1:0>		—	—	CPUPG<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **ADCPG<1:0>:** ADC Permission bits
The Bus Initiator has access to access controlled memory regions as defined by the bus structure's permission group SFRs for RDPER and WRPER.
11 = Read access if RDPER<3> = 1; write access if WRPER<3> = 1
10 = Read access if RDPER<2> = 1; write access if WRPER<2> = 1
01 = Read access if RDPER<1> = 1; write access if WRPER<1> = 1
00 = Read access if RDPER<0> = 1; write access if WRPER<0> = 1

bit 23-22 **FCPG<1:0>:** Flash Control Permission Group bits
Same definition as bits 25-24.

bit 21-20 **Unimplemented:** Read as '0'

bit 19-18 **CAN4G<1:0>:** CAN4 Module Permission Group bits
Same definition as bits 25-24.

bit 17-16 **CAN3PG<1:0>:** CAN3 Module Permission Group bits
Same definition as bits 25-24.

bit 15-14 **CAN2PG<1:0>:** CAN2 Module Permission Group bits
Same definition as bits 25-24.

bit 13-12 **CAN1PG<1:0>:** CAN1 Module Permission Group bits
Same definition as bits 25-24.

bit 11-10 **USB2PG<1:0>:** USB2 Module Permission Group bits
Same definition as bits 25-24.

bit 9-8 **USB1PG<1:0>:** USB1 Module Permission Group bits
Same definition as bits 25-24.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DMAPG<1:0>:** DMA Module Permission Group bits
Same definition as bits 25-24.

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CPUPG<1:0>:** CPU Permission Group bits
Same definition as bits 25-24.

33.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MK GP/MC devices is designed to operate at a nominal 1.2V. To simplify system designs, devices in the PIC32MK GP/MC family incorporate an on-chip regulator providing the required core logic voltage from V_{DD}.

33.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as T_{PU}, code execution is disabled. T_{PU} is applied every time the device resumes operation after any power-down, including Sleep mode.

33.3.2 ON-CHIP REGULATOR AND BOR

PIC32MK GP/MC devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **36.1 "DC Characteristics"**.

33.4 On-chip Temperature Sensor

PIC32MK GP/MC devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **36.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

33.5 Programming and Diagnostics

PIC32MK GP/MC devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32MK devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 33-1: **BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS**
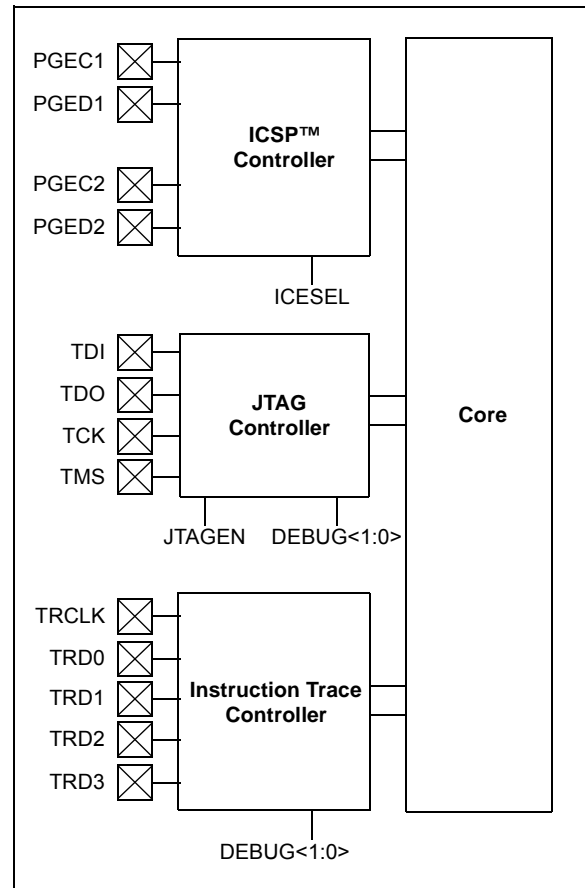
PIC32MK GP/MC Family

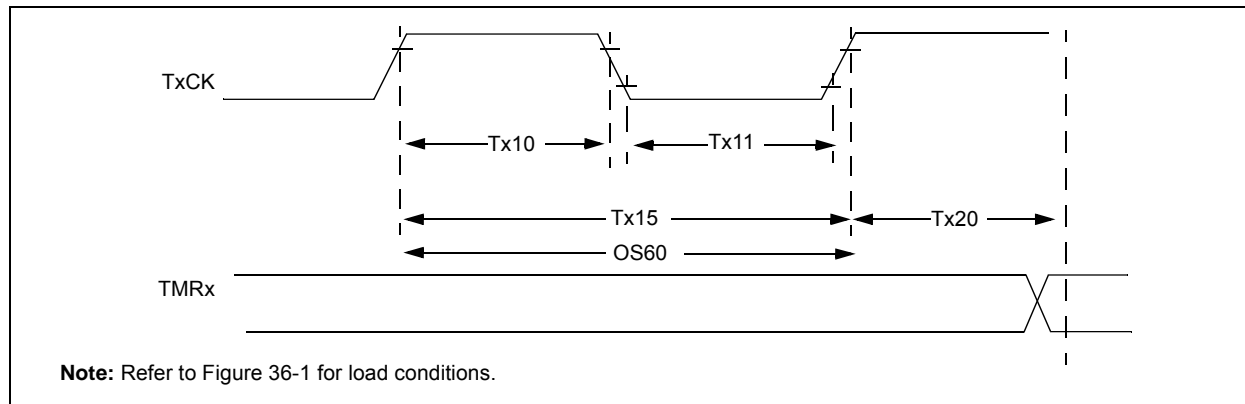**FIGURE 36-6:** TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS

Note: Refer to Figure 36-1 for load conditions.

TABLE 36-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS[1]				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics[2]		Min.	Typ.	Max.	Units	Conditions
TA10	TTxH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TTxL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TTxP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	—	ns	VDD > 2.7V (**Note 3**)
				[(Greater of 20 ns or 2 TPBCLK3)/N] + 50 ns	—	—	ns	VDD < 2.7V (**Note 3**)
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V
				50	—	—	ns	VDD < 2.7V
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPBCLK3	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

PIC32MK GP/MC Family

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

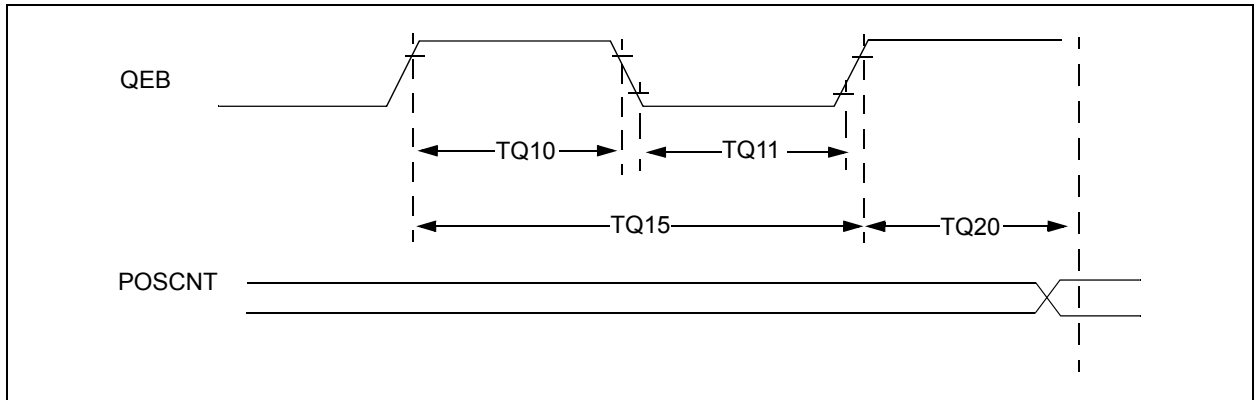**FIGURE 36-14:** **QEI MODULE EXTERNAL CLOCK TIMING CHARACTERISTICS**

TABLE 36-36: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +125°C$ for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	$[(12.5$ or $0.5 \ T_{CY}) / N]$ $+ 25$	—	—	ns	Must also meet parameter TQ15. N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	$[(12.5$ or $0.5 \ T_{CY}) / N]$ $+ 25$	—	—	ns	Must also meet parameter TQ15. N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	$[(25$ or $T_{CY})$ $/ N] + 50$	—	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ20	T$_{CKEXTMRL}$	Delay from External TxCK Clock Edge to Timer Increment		—	1	T$_{CY}$	—	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: N = Index Channel Digital Filter Clock Divide Select bits.