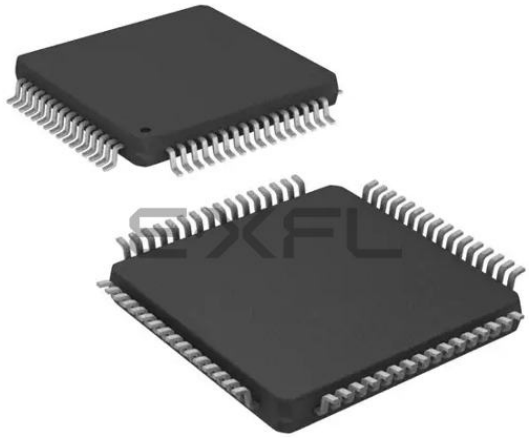
Microchip Technology - PIC32MK1024GPD064T-I/PT Datasheet



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Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpd064t-i-pt

REGISTER 4-6: SBTxECLRS: SYSTEM BUS TARGET 'x' SINGLE ERROR CLEAR REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Single Error on Read bit
A single error as reported through SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-7: SBTxECLRM: SYSTEM BUS TARGET 'x' MULTIPLE ERROR CLEAR REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Multiple Errors on Read bit
Multiple errors as reported through SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 7-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI reset counter.
11111111-00000001 = Number of SYSCLK cycles before a device Reset occurs(1)
00000000 = No delay between NMI assertion and device Reset event

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered the NMICNT will start decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit is written. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
054C	OFF003	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0550	OFF004	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0554	OFF005	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0558	OFF006	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
055C	OFF007	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0560	OFF008	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0564	OFF009	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0568	OFF010	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
056C	OFF011	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0570	OFF012	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0574	OFF013	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0578	OFF014	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
057C	OFF015	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0580	OFF016	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14C4	C1RXR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C1RXR<3:0>				0000
14C8	C2RXR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C2RXR<3:0>				0000
14CC	REFIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFIR<3:0>				0000
14D0	QEA1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA1R<3:0>				0000
14D4	QEB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB1R<3:0>				0000
14D8	INDX1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX1R<3:0>				0000
14DC	HOME1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME1R<3:0>				0000
14E0	QEA2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA2R<3:0>				0000
14E4	QEB2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB2R<3:0>				0000
14E8	INDX2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX2R<3:0>				0000
14EC	HOME2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME2R<3:0>				0000
14F0	FLT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	FLT1R<3:0>				0000
14F4	FLT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	FLT2R<3:0>				0000
14F8	IC10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC10R<3:0>				0000
14FC	IC11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC11R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

3: This register is only available on PIC32MKXXXGPEXXX devices.

TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
16D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD4R<4:0>					0000
16D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD5R<4:0>					0000
16D8	RPD6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD6R<4:0>					0000
1700	RPE0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE0R<4:0>					0000
1704	RPE1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE1R<4:0>					0000
1738	RPE14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF14R<4:0>					0000
173C	RPE15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE15R<4:0>					0000
1740	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF0R<4:0>					0000
1744	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF1R<4:0>					0000
1780	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG0R<4:0>					0000
1784	RPG1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG1R<4:0>					0000
1798	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG6R<4:0>					0000
179C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG7R<4:0>					0000
17A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG8R<4:0>					0000
17A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG9R<4:0>					0000
17B0	RPG12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG12R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 20-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI/I2S Module On bit
1 = SPI/I2S module is enabled
0 = SPI/I2S module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit(4)
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin used for Slave mode
0 = $\overline{SSx}$ pin not used for Slave mode, pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

Note 1: This bit can only be written when the ON bit = 0. Refer to **36.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 25-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 TAD
•
•
•
0000000001 = 3 TAD
0000000000 = 2 TAD

Where TAD = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

Note: Unlike the High-Speed Class 1 ADC modules, the trigger event for the shared Class 3 ADC7 module initiates the SAMC *sampling* sequence, rather than the *convert* sequence.

Shared ADC7 Throughput rate:

= ((1/((Sample time + Conversion Time)(TAD))) / Number of ADC inputs used in scan list)

= ((1 / ((SAMC + Number of Bit Resolution + 1)(TAD))) / Number of ADC inputs used in scan list)

Example:

Scan mode enabled with two ANx inputs in the scan list (i.e., ADCCSSx<CSSy>),
SAMC = 4 TAD, 12-bit mode, TAD = 16.667 ns = 60 MHz:

Throughput rate = ((1 / ((4+12 + 1)(16.667 ns))) / 2)

= ((1 / (17 * 16.667 ns)) / 2)

= 1.764706 msps

bit 15 **BGVRIEN:** Band Gap/VREF Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

bit 14 **REFFLTIEN:** Band Gap/VREF Voltage Fault Interrupt Enable bit

1 = Interrupt will be generated when the REFFLT bit is set
0 = No interrupt is generated when the REFFLT bit is set

bit 13 **EOSIEN:** End of Scan Interrupt Enable bit

1 = Interrupt will be generated when EOSRDY bit is set
0 = No interrupt is generated when the EOSRDY bit is set

bit 12 **ADCEIOVR:** Early Interrupt Request Override bit

1 = Early interrupt generation is overridden and interrupt generation is controlled by the ADCGIRQEN1 and ADCGIRQEN2 registers
0 = Early interrupt generation is not overridden and interrupt generation is controlled by the ADCEIEN1 and ADCEIEN2 registers

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCEIS<2:0>:** Shared ADC (ADC7) Early Interrupt Select bits

These bits select the number of clocks (TAD7) prior to the arrival of valid data that the associated interrupt is generated.

111 = The data ready interrupt is generated 8 ADC clocks prior to end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to end of conversion
•
•
•
001 = The data ready interrupt is generated 2 ADC module clocks prior to end of conversion
000 = The data ready interrupt is generated 1 ADC module clock prior to end of conversion

Note: All options are available when the selected resolution, set by the SELRES<1:0> bits (ADCCON1<22:21>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 7 **Unimplemented:** Read as '0'

REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 19 **DIGEN3:** ADC3 Digital Enable bit
1 = ADC3 is digital enabled (required for active operation)
0 = ADC3 is digital disabled (power-saving mode)

bit 18 **DIGEN2:** ADC2 Digital Enable bit
1 = ADC2 is digital enabled (required for active operation)
0 = ADC2 is digital disabled (power-saving mode)

bit 17 **DIGEN1:** ADC1 Digital Enable bit
1 = ADC1 is digital enabled (required for active operation)
0 = ADC1 is digital disabled (power-saving mode)

bit 16 **DIGEN0:** ADC0 Digital Enable bit
1 = ADC0 is digital enabled (required for active operation)
0 = ADC0 is digital disabled (power-saving mode)

bit 15-13 **VREFSEL<2:0>:** Voltage Reference (VREF) Input Selection bits

VREFSEL<2:0>	ADC VREFH	ADC VREFL
1xx	Reserved	Reserved
011	VREF+	VREF-
010	AVDD	VREF-
001	VREF+	AVSS
000	AVDD	AVSS

bit 12 **TRGSUSP:** Trigger Suspend bit
1 = Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0 = Triggers are not blocked

bit 11 **UPDIEN:** Update Ready Interrupt Enable bit
1 = Interrupt will be generated when the UPDRDY bit is set by hardware
0 = No interrupt is generated

bit 10 **UPDRDY:** ADC Update Ready Status bit
1 = ADC SFRs can be updated
0 = ADC SFRs cannot be updated

Note: This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

bit 9 **SAMP:** Shared ADC7 Analog Input Sampling Enable bit**(1,2,3,4)**
1 = The ADC S&H amplifier is sampling
0 = The ADC S&H amplifier is holding

bit 8 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input through software.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = Do not trigger the conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 25-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 14 **SIGN23:** AN23 Signed Data Mode bit(1)
1 = AN23 is using Signed Data mode
0 = AN23 is using Unsigned Data mode

bit 13 **DIFF22:** AN22 Mode bit(1)
1 = Selects AN22 differential pair input as AN22+ and AN1-
0 = AN22 is using Single-ended mode

bit 12 **SIGN22:** AN22 Signed Data Mode bit(1)
1 = AN22 is using Signed Data mode
0 = AN22 is using Unsigned Data mode

bit 11 **DIFF21:** AN21 Mode bit(1)
1 = Selects AN21 differential pair input as AN21+ and AN1-
0 = AN21 is using Single-ended mode

bit 10 **SIGN21:** AN21 Signed Data Mode bit(1)
1 = AN21 is using Signed Data mode
0 = AN21 is using Unsigned Data mode

bit 9 **DIFF20:** AN20 Mode bit(1)
1 = Selects AN20 differential pair input as AN20+ and AN1-
0 = AN20 is using Single-ended mode

bit 8 **SIGN20:** AN20 Signed Data Mode bit(1)
1 = AN20 is using Signed Data mode
0 = AN20 is using Unsigned Data mode

bit 7 **DIFF19:** AN19 Mode bit
1 = Selects AN19 differential pair input as AN19+ and AN1-
0 = AN19 is using Single-ended mode

bit 6 **SIGN19:** AN19 Signed Data Mode bit
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = Selects AN18 differential pair input as AN18+ and AN1-
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = Selects AN17 differential pair input as AN17+ and AN1-
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = Selects AN16 differential pair input as AN16+ and AN1-
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-15: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER ('x' = 1 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **CMPE27:CMPE0:** ADC Digital Comparator 'x' Enable bits

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

Note 1: CMPE*x* = AN*x*, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

2: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

REGISTER 25-27: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the AIRDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

REGISTER 26-14: CxRXFn: CAN ACCEPTANCE FILTER 'n' REGISTER 7 ('x' = 1-4; 'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SID<10:3>							
23:16	R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
	SID<2:0>			—	EXID	—	EID<17:16>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 20 **Unimplemented:** Read as '0'

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

Note: This register can only be modified when the filter is disabled (FLTENn = 0).

REGISTER 27-3: CMxMSKCON: COMPARATOR 'x' MASK CONTROL REGISTER ('x' = 1-5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SELSRCC<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SELSRCB<3:0>				SELSRCA<3:0>			
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-24 **SELSRCC<3:0>:** Mask C Input Select bits
See the definitions for the SELSRCA<3:0> bits.

bit 23-20 **SELSRCB<3:0>:** Mask B Input Select bits
See the definitions for the SELSRCA<3:0> bits.

bit 19-16 **SELSRCA<3:0>:** Mask A Input Select bits
1111 = FLT4 pin
1110 = FLT2 pin
1101 = Reserved
1100 = Reserved
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 15 **HLMS:** High or Low Level Masking Select bit
1 = The comparator deasserted state is 1, and the masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The comparator deasserted state is 0, and the masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate "C" Input Enable bit
1 = "C" input enabled as input to OR gate
0 = "C" input disabled as input to OR gate

Note: This register is only available on PIC32MKXXMCXXX devices.

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 7-6 **OVRDAT<1:0>:** State(3) for PWMxH, PWMxL Pins if Override is Enabled bits
If OVRENH = 1, OVRDAT<1> provides data for PWMxH
If OVRENL = 1, OVRDAT<0> provides data for PWMxL

bit 5-4 **FLTDAT<1:0>:** State(3) for PWMxH and PWMxL Pins if FLTMOD is Enabled bits(2)
If FLTMOD<1:0> (IOCONx<17:16>) = 00 or 01, one of the following Fault modes is enabled:
If fault is active, FLTDAT<1> provides the state for PWMxH
If fault is active, FLTDAT<0> provides the state for PWMxL
If fault is inactive, FLTDAT<1:0> bits are ignored

bit 3-2 **CLDAT<1:0>:** State for PWMxH and PWMxL Pins if CLMOD is Enabled bits(3)
If CLMOD (IOCONx<24>) = 1, Current-Limit mode is enabled, as follows:
If current limit is active, CLTDAT<1> provides the state for PWMxH
If current limit is active, CLTDAT<0> provides the state for PWMxL
If current limit is inactive, CLTDAT<1:0> bits are ignored

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to PWMxL pin; PWMxL output signal is connected to PWMxH pin
0 = PWMxH and PWMxL output signals pins are mapped to their respective pins

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

TABLE 32-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name(3)	Register Name and Bit Location
ADC1-ADC7	ADC1MD	PMD1<0>
CDAC1	DAC1MD	PMD1<4>
CDAC2	DAC2MD	PMD1<5>
CDAC3	DAC3MD	PMD1<6>
CTMU	CTMU1MD	PMD1<8>
Data EEPROM	EEMD	PMD1<9>
Comparator 1	C1MD	PMD2<0>
Comparator 2	C2MD	PMD2<1>
Comparator 3	C3MD	PMD2<2>
Comparator 4	C4MD	PMD2<3>
Comparator 5	C5MD	PMD2<4>
Op amp 1	OPA1MD	PMD2<16>
Op amp 2	OPA2MD	PMD2<17>
Op amp 3	OPA3MD	PMD2<18>
Op amp 5	OPA5MD	PMD2<20>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Input Capture 10	IC10MD	PMD3<9>
Input Capture 11	IC11MD	PMD3<10>
Input Capture 12	IC12MD	PMD3<11>
Input Capture 13	IC13MD	PMD3<12>
Input Capture 14	IC14MD	PMD3<13>
Input Capture 15	IC15MD	PMD3<14>
Input Capture 16	IC16MD	PMD3<15>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

3: For any associated PMDx bit, `0` = clocks enabled to the peripheral; `1` = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

35.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

35.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

35.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

35.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 36-21: COMPARATOR SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (Note 2): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM30	VIOFF	Input Offset Voltage	-10	—	10	mV	—
CM31	VICM	Input Common Mode Voltage	AVSS +0.9	—	2.5V	V	—
CM33	TRESP	Large Signal Response Time	—	50	—	ns	VCM = VDD/2; 200 mV step
CM36	VHYST	Input Hysteresis Voltage	48	120	192	mV	—
CM37	VGAIN	Open Loop Voltage Gain	—	90	—	dB	—
CM38	TSRESP	Small Signal Response Time	—	100	—	ns	VCM = VDD/2; 100 mV step
CM39	TRISE	Output Rise Time	—	20	—	ns	Refer to parameter DO56.
CM40	TFALL	Output Fall Time	—	20	—	ns	Refer to parameter DO56.
CM41	V I/P	Input Voltage Range	AVSS	—	AVDD	V	—
CM42	ILKG	Input Leakage Control	—	See IIL in Table 36-9	—	nA	—
CM43	TON	Comparator Enabled to Output Valid	—	10	—	µs	Comparator module is configured before setting the Comparator ON bit
CM44	TOFF	Disable to outputs disabled	—	100	—	ns	—

Note 1: These parameters are characterized but not tested.

TABLE 36-39: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.3	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	VREFL + 1.8	—	AVDD	V	**(Note 1)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.8	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.8	—	AVDD	V	**(Note 2)**
AD08	IREF	Current Drain	—	102	—	µA	ADC is operating or is in Stand-by.
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS	—	VREFL	V	—
AD14	VINH	Absolute VINH Input Voltage	AVSS	—	VREFH	V	—
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	—	±2	—	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed **(Note 2)**
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	67	—	dB	Single-ended **(Notes 2,3)**
AD34b	ENOB	Effective Number of bits	—	10.8	—	bits	**(Notes 2,3)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

FIGURE 36-20: MOTOR CONTROL PWM MODULE FAULT TIMING CHARACTERISTICS

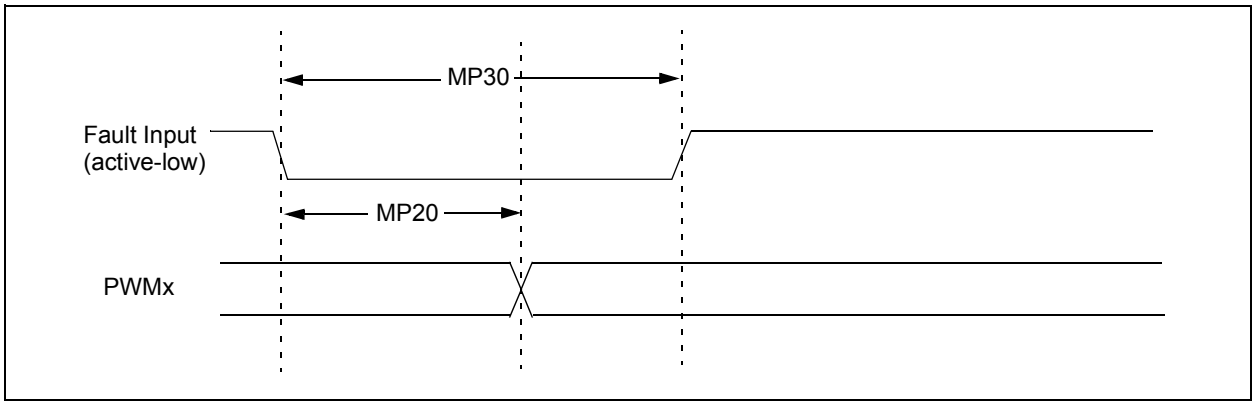


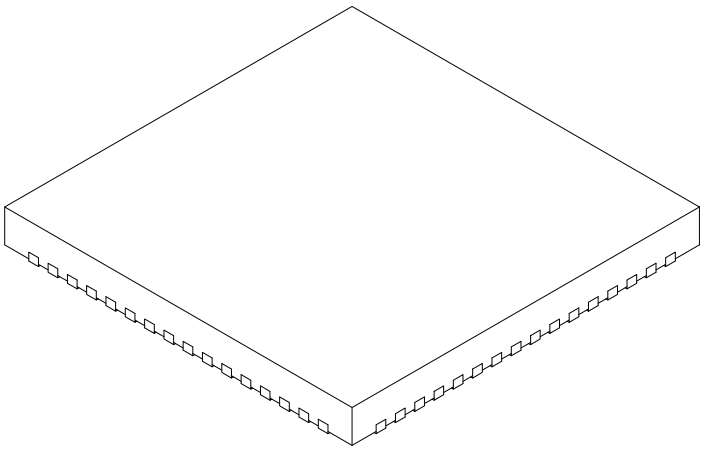
TABLE 36-49: MOTOR CONTROL PWM MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	TFPWM	PWM Output Fall Time	—	—	—	ns	See parameter DO32
MP11	TRPWM	PWM Output Rise Time	—	—	—	ns	See parameter DO31
MP20	TFD	Fault Input ↓ to PWM I/O Change	—	—	50	ns	—
MP30	TFH	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2