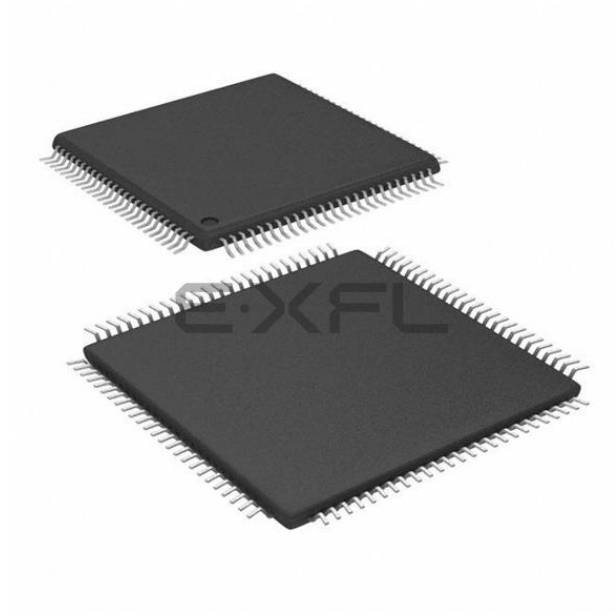
Microchip Technology - PIC32MK1024GPD100T-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	77
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpd100t-i-pt

TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MK0512MCF100
PIC32MK1024MCF100

100

1

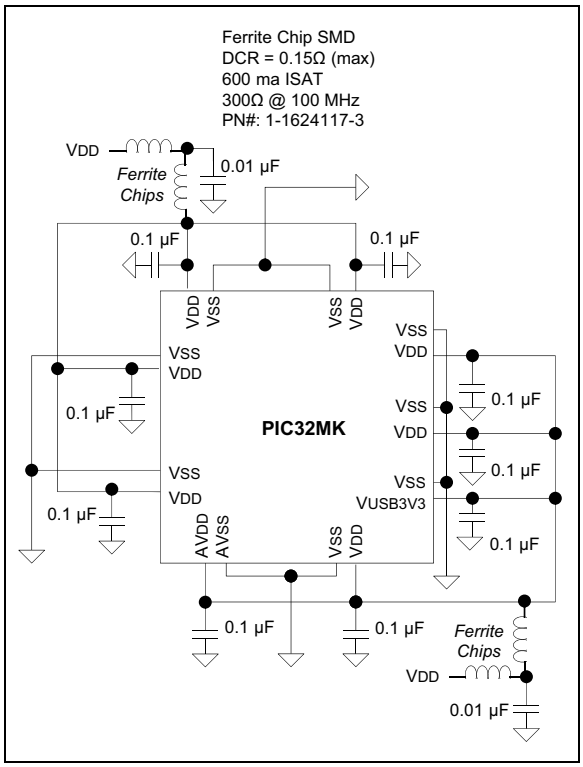
Pin #	Full Pin Name	Pin #	Full Pin Name
71	DAC2/AN48/CVD48/RPC10/PMPA14/PSPCS/RC10	86	VDD
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7	87	RPF0/PWM11H/PMPD11/RF0
73	SOSCI/RPC13(4)/RC13(4)	88	RPF1/PWM11L/PMPD10/RF1
74	SOSCO/RPB8(4)/RB8(4)	89	RPG1/PMPD9/RG1
75	VSS	90	RPG0/PMPD8/RG0
76	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9	91	TRCLK/PMPA18/RF6
77	RPC6/USBID2/PMPA16/RC6	92	TRD3/PMPA19/RF7
78	RPC7/PMPA17/RC7	93	RPB10/PWM3H/PMPD0/RB10
79	PMPD12/RD12	94	RPB11/PWM9H/PWM3L/PMPD1/RB11
80	PMPD13/RD13	95	TRD2/PMPA20/RG14
81	RPC8/PMPWR/PSPWR/RC8	96	TRD1/RPG12/PMPA21/RG12
82	RPD5/PWM12H/PMPRD/PSPRD/RD5	97	TRD0/PMPA22/RG13
83	RPD6/PWM12L/PMPD14/RD6	98	RPB12/PWM2H/PMPD2/RB12
84	RPC9/PMPD15/RC9	99	RPB13/PWM8H/PWM2L/CTPLS/PMPD3/RB13
85	VSS	100	TDO/PWM4H/PMPD4/RA10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

2.10.1.3 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/Boost regulators as the local power source for PIC32MK GP devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-9. In addition to a more stable power source, use of this type of T-Filter can greatly reduce susceptibility to EMI sources and events.

FIGURE 2-9: EMI/EMC/EFT SUPPRESSION CIRCUIT



REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, C	U-0	U-0	U-0	R/W-0, C	R/W-0, C	R/W-0, C	R/W-0, C
	MULTI	—	—	—	CODE<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	INITID<7:0>							
7:0	R-0	R-0	R-0	R-0	U-0	R-0	R-0	R-0
	REGION<3:0>				—	CMD<2:0>		

Legend:	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31 **MULTI:** Multiple Permission Violations Status bit
This bit is cleared by writing a '1'.
1 = Multiple errors have been detected
0 = No multiple errors have been detected

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CODE<3:0>:** Error Code bits
Indicates the type of error that was detected. These bits are cleared by writing a '1'.
1111 = Reserved
1101 = Reserved
•
•
•
0011 = Permission violation
0010 = Reserved
0001 = Reserved
0000 = No error

bit 23-16 **Unimplemented:** Read as '0'

bit 15-8 **INITID<7:0>:** Initiator ID of Requester bits
11111111 = Reserved
•
•
•
00001111 = Reserved
00001110 = Reserved
00001101 = CAN4
00001100 = CAN3
00001011 = CAN2
00001010 = CAN1
00001001 = USB2
00001000 = USB1
00000111 = ADC0-ADC5, ADC7
00000110 = Reserved
00000101 = Flash Controller
00000100 = DMA Read
00000011 = DMA Read
00000010 = CPU (CPUPRI (CFGCON<24>) = 1)
00000001 = CPU (CPUPRI (CFGCON<25>) = 0)
00000000 = Reserved

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 9-5: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 9-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Output Enable bit(1)
1 = Reference Oscillator Module enabled
0 = Reference Oscillator Module disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on REFCLKOx pin
0 = Reference clock is not driven out on REFCLKOx pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference Oscillator Module output continues to run in Sleep
0 = Reference Oscillator Module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 11-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
Either the source or the destination address is invalid.
0 = No interrupt is pending

REGISTER 11-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

12.1 Control Registers

TABLE 12-1: USB1 AND USB2 REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9040	U1OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
9050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
9060	U1OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
9070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
9080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
9200	U1IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
9210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
9220	U1EIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
9230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
9240	U1STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
9250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
9260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
9270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<15:9>							—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

TABLE 12-1: USB1 AND USB2 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A040	U2OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
A050	U2OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
A060	U2OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
A070	U2OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
A080	U2PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
A200	U2IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
A210	U2IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

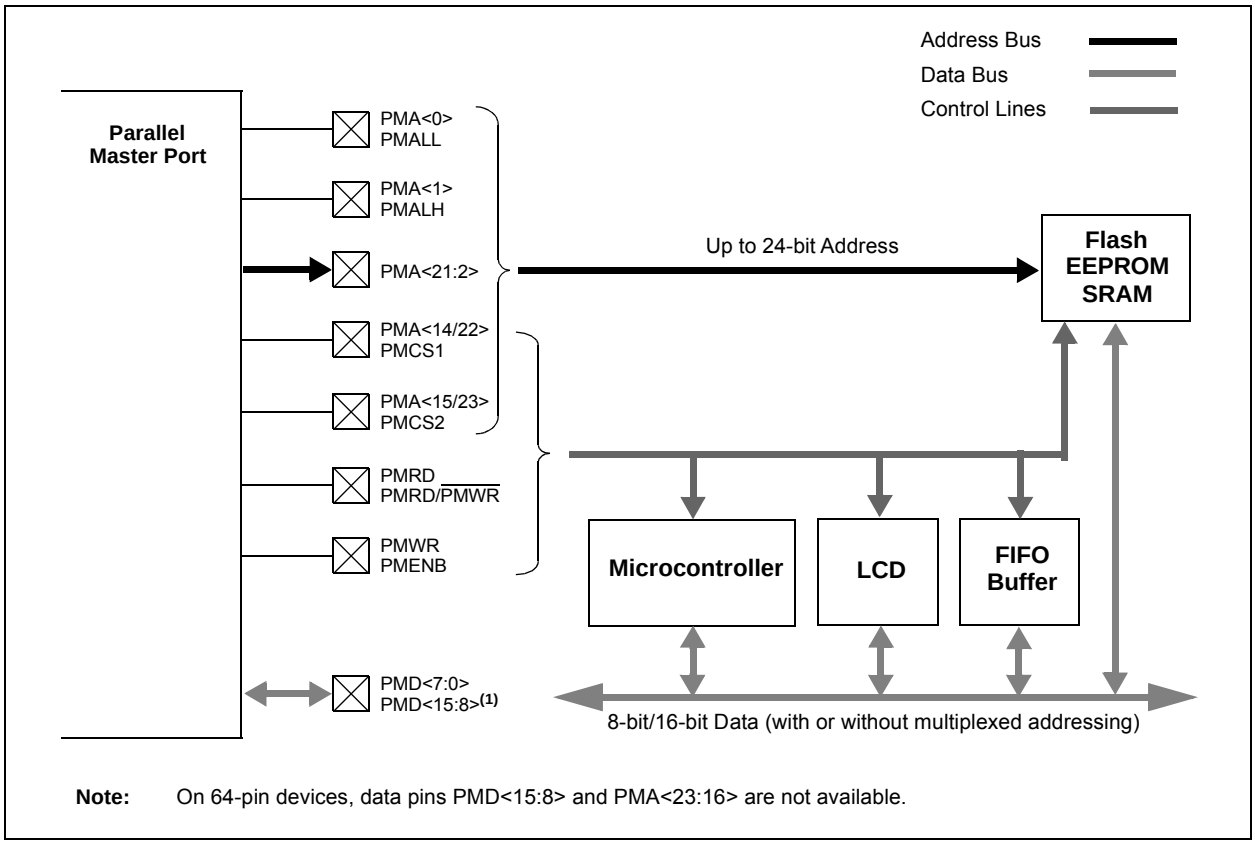
TABLE 13-4: PORTA REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ANSA12	ANSA11	—	—	ANSA8	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0623
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TRISA12	TRISA11	TRISA10	—	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	06FF
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	RA12	RA11	RA10	—	RA8	RA7	—	—	RA4	—	—	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LATA12	LATA11	LATA10	—	LATA8	LATA7	—	—	LATA4	—	—	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ODCA12	ODCA11	ODCA10	—	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNPUA12	CNPUA11	CNPUA10	—	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNPDA12	CNPDA11	CNPDA10	—	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNIEA12	CNIEA11	CNIEA10	—	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CN STATA12	CN STATA11	CN STATA10	—	CN STATA8	CN STATA7	—	—	CN STATA4	—	—	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNNEA12	CNNEA11	CNNEA10	—	CNNEA8	CNNEA7	—	—	CNNEA4	—	—	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNFA12	CNFA11	CNFA10	—	CNFA8	CNFA7	—	—	CNFA4	—	—	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR0A10	—	SR0A8	SR0A7	—	—	—	—	—	—	—	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR1A10	—	SR1A8	SR1A7	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

FIGURE 23-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Note: On 64-pin devices, data pins PMD<15:8> and PMA<23:16> are not available.

REGISTER 24-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6

REGISTER 25-16: ADCCMPx: ADC DIGITAL COMPARATOR 'x' LIMIT VALUE REGISTER ('x' = 1 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<15:8>(1,2,3)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<7:0>(1,2,3)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<15:8>(1,2,3)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<7:0>(1,2,3)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DCMPHI<15:0>:** Digital Comparator 'x' High Limit Value bits(1,2,3)

These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

bit 15-0 **DCMPLO<15:0>:** Digital Comparator 'x' Low Limit Value bits(1,2,3)

These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

Note 1: Changing theses bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

2: The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.

3: For Digital Comparator 0 used in CVD mode, the DCMPHI<15:0> and DCMPLO<15:0> bits must always be specified in signed format, as the CVD output data is differential and is always signed.

REGISTER 26-17: CxFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('x' = 1-4); n' = 0 THROUGH 15) (CONTINUED)

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'

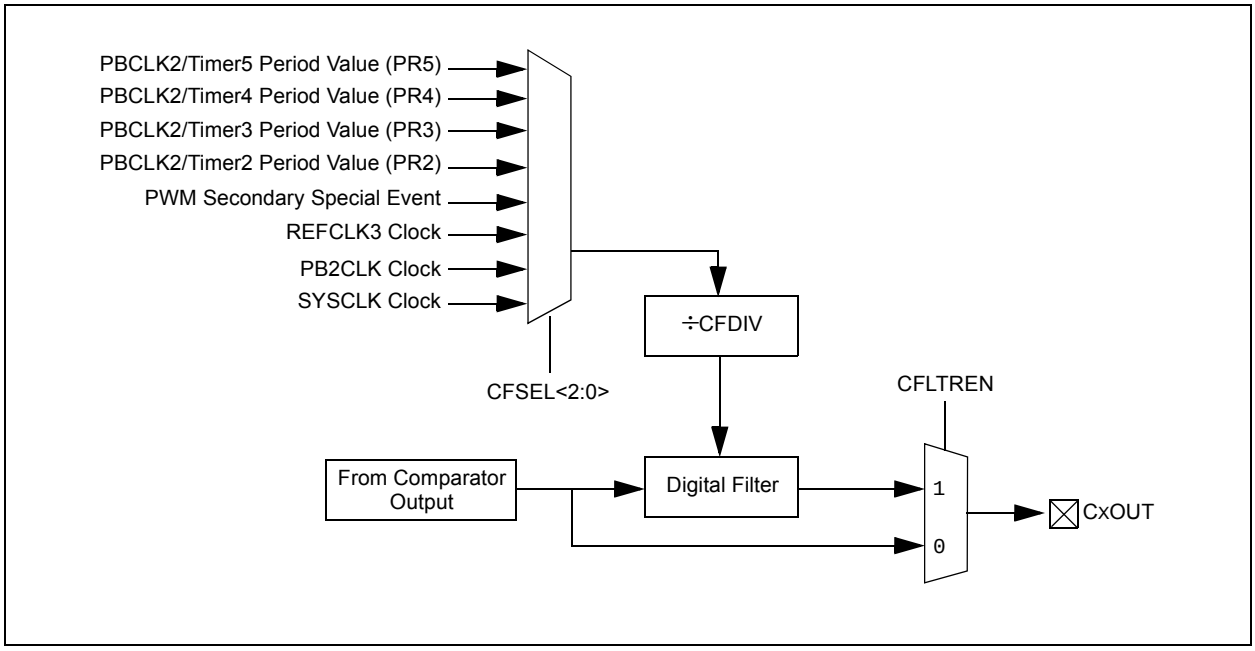
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

27.4 Comparator Output Filtering

The outputs can also be digitally filtered for glitches or noise. The digital filter has the capability to sample at different frequencies using different clock sources specified by the CFSEL<2:0> bits in the CxCON register. The digital filter looks for three consecutive samples of the same logic state before updating the comparator output. Since the digital filter affects the response times of the output, care should be taken while choosing the filter clock divisor to best suit the application at hand.

FIGURE 27-7: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 25 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control edge source
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 24 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control edge source
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 23 **EDG2MOD:** Edge 2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 programmed for a positive edge response
0 = Edge 2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = C5OUT Capture Event is selected
1110 = C4OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC6 Capture Event is selected
1011 = IC5 Capture Event is selected
1010 = IC4 Capture Event is selected
1001 = IC3 pin is selected
1000 = IC2 pin is selected
0111 = IC1 pin is selected
0110 = OC4 pin is selected
0101 = OC3 pin is selected
0100 = OC2 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1101' to select C1OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 36-43) in **Section 36.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

5: For CTMU temperature measurements on this range, ADC sampling time ≥ 1.6 µs.

6: For CTMU temperature measurements on this range, ADC sampling time ≥ 300 ns.

REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 must occur before Edge 2 can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current (i.e., 55 µA Typical(6))
10 = 10 times base current (i.e., 5.5 µA Typical(5))
01 = Base current level (i.e., 0.55 µA Typical(4))
00 = 1000 times base current (i.e., 550 µA Typical(4))

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1101' to select C1OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 36-43) in **Section 36.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

5: For CTMU temperature measurements on this range, ADC sampling time ≥ 1.6 µs.

6: For CTMU temperature measurements on this range, ADC sampling time ≥ 300 ns.

31.2 Motor Control PWM Control Registers

TABLE 31-1: MCPWM REGISTER MAP

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	PTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN	—	PTSIDL	SESTAT	SEIEN	PWMRDY	—	—	—	PCLKDIV<2:0>			SEVTPS<3:0>				0000
A010	PTPER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTPER<15:0>																0020
A020	SEVTCMP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SEVTCMP<15:0>																0000
A030	PMTMR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMTMR<15:0>																0000
A040	STCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	SSESTAT	SSEIEN	—	—	—	—	SCLKDIV<2:0>			SEVTPS<3:0>				0000
A050	STPER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STPER<15:0>																0020
A060	SSEVTCMP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SSEVTCMP<15:0>																0000
A070	SMTMR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SMTMR<15:0>																0000
A080	CHOP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:0>										0000
A090	PWMKEY	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PWMKEY<15:0>																0000
A0C0	PWMCON1	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A0D0	IOCON1	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A0E0	PDC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A0F0	SDC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A100	PHASE1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A110	DTR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

FIGURE 36-2: EXTERNAL CLOCK TIMING

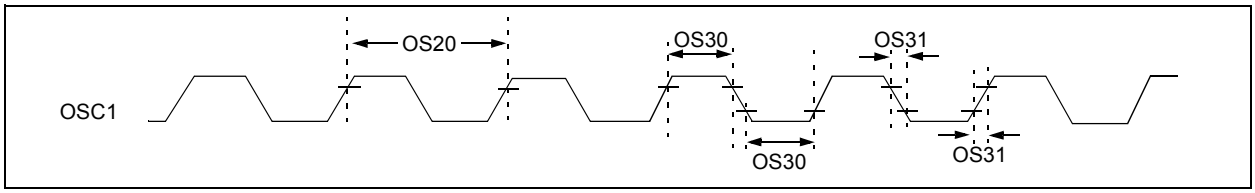


TABLE 36-15: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical(1)**	**Maximum**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC **(Note 2,3)**
OS13		Oscillator Crystal Frequency	4	—	24	MHz	HS **(Note 2,3)**
OS15			32	32.768	100	kHz	SOSC **(Note 2)**
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.375 x TOSC	—	0.675 x TOSC	ns	EC **(Note 2)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC **(Note 2)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 2)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 2)**
OS42	GM	External Oscillator Transconductance	—	16	—	mA/V	VDD = 3.3V, TA = +25°C, HS **(Note 2)**

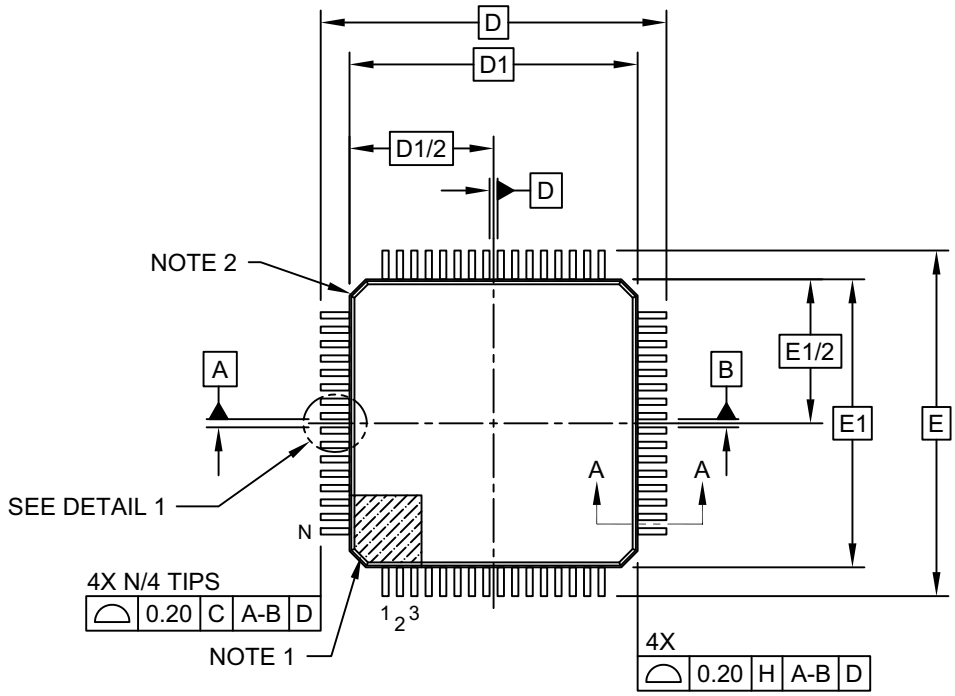
Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

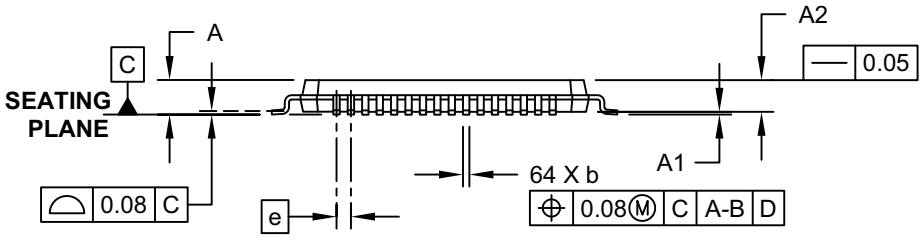
3: See parameter OS50 for PLL input frequency limitations.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

Revision D (March 2017)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
"32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps"	page 1 - Updates in **"Power Management" "Motor Control PWM" "Motor Encoder Interface" "Audio/Graphics/Touch Interfaces" "Unique Features" "Advanced Analog Features" "Communication Interfaces" "Qualification and Class B Support"** Removed VBAT column in Table 1. Added Note 8 in Table 3. Added Note 7 in Table 5.
1.0 "Device Overview"	Added Note 1 in Table 1-20.
25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	Added Note 1 to Register 25-4.
31.0 "Motor Control PWM Module"	Updated first page bulleted list to "Nine Fault input pins are available for Faults and current limits." Updated pin table in Figure 31-1. Updated **31.1.2 "WRITE-PROTECTED REGISTERS"** Updated label TMRx to PTMRx in Figure 31-2. Updated "All Resets" value from 0000 to 0078 for IOCONx<31:16> registers in Table 31-1. Updated bit 15-0 descriptions in Register 31-6.and Register 31-10 Updated note in Register 31-10. Updated bit 11-10 description in Register 31-11. Updated Notes 1 and 4 in Register 31-12. Updated Note 1 and added note markers in DTCOMP<13:8> and DTCOMP<7:0> in Register 31-18.
36.0 "Electrical Characteristics"	Updated parameter DI20 Min. VDD value in Table 36-9. Updated parameter OS13 Max. MHz value in Table 36-15. Updated Note 2 equation value from PBCLK2 to PBCLKx in Table 36-16. Updated Table 36-28 to include parameter OA14. Updated Min. ADC Clock Period for parameter AD50 in Table 36-39. Updated Max. Sample Throughput Rates for parameter AD51 in Table 36-39. Updated Table 36-42 to include parameter CTMU0.