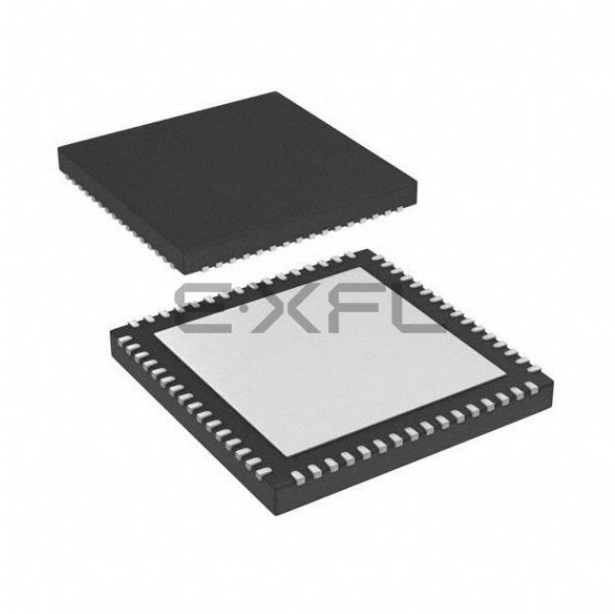
Microchip Technology - PIC32MK1024GPE064-E/MR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpe064-e-mr

TABLE 1-14: USB1 AND USB2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
VUSB3V3	55	35	P	—	USB internal transceiver supply. This pin should be connected to VDD.
VBUS1	54	34	I	Analog	USB1 Bus Power Monitor
VBUSON1	4	2	O	CMOS	USB1 VBUS Power Control Output
VBUSON2	10	—	O	CMOS	USB2 VBUS Power Control Output
D1+	57	37	I/O	Analog	USB1 D+
D1-	56	36	I/O	Analog	USB1 D-
USBID1	69	43	I	ST	USB1 OTG ID Detect
VBUS2	58	—	I	Analog	USB2 Bus Power Monitor
D2+	60	—	I/O	Analog	USB2 D+
D2-	59	—	I/O	Analog	USB2 D-
USBID2	77	—	I	ST	USB2 OTG ID detect

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-15: CTMU PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CTED1	25	16	I	ST	CTMU External Edge Input 1
CTED2	24	15	I	ST	CTMU External Edge Input 2
CTCMP	27	18	I	Analog	CTMU external capacitor input for pulse generation
CTPLS	PPS	PPS	O	CMOS	CTMU Pulse Generator Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-16: CDAC1 THROUGH CDAC3 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CDAC1	51	33	O	Analog	12-bit CDAC1 output
CDAC2	71	45	O	Analog	12-bit CDAC2 output
CDAC3	49	31	O	Analog	12-bit CDAC3 output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

8.3 Interrupt Control Registers

TABLE 8-4: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	INTCON	31:16	SWNMIKEY<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0(7)	31:16	FCEIF	RTCCIF	—	—	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1(7)	31:16	U3RXIF	U3EIF	—	—	—	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	CNGIF	CNFIF	CNEIF	0000
		15:0	CNDIF	CNCIF	CNBIF	CNAIF	—	—	—	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USB1IF	CMP2IF	CMP1IF	0000
0060	IFS2(7)	31:16	AD1DC2IF	AD1DC1IF	-	AD1IF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
		15:0	OC6IF	IC6IF	IC6EIF	T6IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	U5TXIF	U5RXIF	U5EIF	U4TXIF	U4RXIF	U4EIF	U3TXIF	0000
0070	IFS3(7)	31:16	AD1D21IF	AD1D20IF	AD1D19IF	AD1D18IF	AD1D17IF	AD1D16IF	AD1D15IF	AD1D14IF	AD1D13IF	AD1D12IF	AD1D11IF	AD1D10IF	AD1D9IF	AD1D8IF	AD1D7IF	AD1D6IF	0000
		15:0	AD1D5IF	AD1D4IF	AD1D3IF	AD1D2IF	AD1D1IF	AD1D0IF	AD1G1IF	AD1FCBTIF	AD1RSIF	AD1ARIF	AD1EOSIF	AD1F1IF	AD1DF4IF	AD1DF3IF	AD1DF2IF	AD1DF1IF	0000
0080	IFS4(7)	31:16	AD1D53IF	AD1D52IF	AD1D51IF	AD1D50IF	AD1D49IF	AD1D48IF	AD1D47IF	AD1D46IF	AD1D45IF	—	—	—	AD1D41IF	AD1D40IF	AD1D39IF	AD1D38IF	0000
		15:0	AD1D37IF	AD1D36IF	AD1D35IF	AD1D34IF	AD1D33IF	—	—	—	—	—	AD1D27IF	AD1D26IF	AD1D25IF	AD1D24IF	AD1D23IF	AD1D22IF	0000
0090	IFS5(7)	31:16	QEI5IF	QEI4IF	QEI3IF	CAN4IF(3)	CAN3IF(3)	DATAEEIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	—	—	—	PWM6IF	PWM5IF	PWM4IF	0000
		15:0	PWM3IF	PWM2IF	PWM1IF	PWM SEVTIF	PWM PEVTIF	QEI2IF	QEI1IF	CAN2IF(3)	CAN1IF(3)	U6TXIF	U6RXIF	U6EIF	—	CMP5IF	CMP4IF	CMP3IF	0000
00A0	IFS6(7)	31:16	SPI4TXIF	SPI4RXIF	SPI4EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	OC16IF	IC16IF	IC16EIF	OC15IF	IC15IF	IC15EIF	OC14IF	C14IF	IC14EIF	OC13IF	0000
		15:0	IC13IF	IC13EIF	OC12IF	IC12IF	IC12EIF	OC11IF	IC11IF	IC11EIF	OC10IF	IC10IF	IC10EIF	—	—	—	—	QEI6IF	0000
00B0	IFS7(7)	31:16	—	CPCIF	—	—	—	—	—	—	—	AD1DC4IF	AD1DC3IF	USB2IF(2)	PWM12IF	PWM11IF	PWM10IF	PWM9IF	0000
		15:0	PWM8IF	PWM7IF	—	—	—	—	—	—	—	SBIF	SPI6TXIF	SPI6RXIF	SPI6EIF	SPI5TXIF	SPI5RXIF	SPI5EIF	0000
00C0	IEC0	31:16	FCEIE	RTCCIE	-	-	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 8-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER 'x' ('x' = 0-63)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 8-3 for the exact bit definitions.

REGISTER 9-6: REFOxTRIM: REFERENCE OSCILLATOR TRIM REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value
111111110 = 510/512 divisor added to RODIV value
•
•
•
100000000 = 256/512 divisor added to RODIV value
•
•
•
000000010 = 2/512 divisor added to RODIV value
000000001 = 1/512 divisor added to RODIV value
000000000 = 0 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '0'

Note 1: While the ON bit (REFOxCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

2: Do not write to this register when the ON bit (REFOxCON<15>) is not equal to the ACTIVE bit (REFOxCON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFOxCON<30:16>) = 0.

4: REFCLKOx Frequency = ((Selected Source Clock / 2) * (N + (M / 512)))
where, Selected source clock = ROSEL, N = RODIV<14:0>, and M = ROTRIM<8:0>.
If the value of REFCLKOx Frequency is not a whole integer value, the output clock will have jitter as it will cause the REFCLKOx circuit to clock cycle steal to produce an average frequency equivalent to the user application's desired frequency. The amount of jitter, (i.e., clock cycle steals), become less as the fractional remainder value becomes closer to a whole number and is greatest at any value plus 0.5.

REGISTER 10-3: CHEMIS: CACHE MISS STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEMIS<31:0>:** Instruction Cache Miss Count bits

When the CHEPERFEN bit (CHECON<12>) = 1, the CHEMIS<31:0> bits increment each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

The CHEMIS<31:0> bits are reset on a '0' to '1' transition of the CHEPERFEN bit.

TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14A0	DCH5DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
14B0	DCH5CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
14C0	DCH5CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
14D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
14E0	DCH6CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
14F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1510	DCH6SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1520	DCH6DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
15A0	DCH7CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-10: PORTE REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0440	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATE15	CN STATE14	CN STATE13	CN STATE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEE15	CNNEE14	CNNEE13	CNNEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFE15	CNFE14	CNFE13	CNFE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0E15	SR0E14	SR0E13	SR0E12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1E15	SR1E14	SR1E13	SR1E12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1600	RPA0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA0R<4:0>					0000
1604	RPA1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA1R<4:0>					0000
1608	RPA2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA2R<4:0>					0000
160C	RPA3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA3R<4:0>					0000
1610	RPA4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA4R<4:0>					0000
161C	RPA7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA7R<4:0>					0000
1620	RPA8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA8R<4:0>					0000
162C	RPA11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA11R<4:0>					0000
1630	RPA12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA12R<4:0>					0000
1638	RPA14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA14R<4:0>					0000
163C	RPA15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA15R<4:0>					0000
1640	RPB0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB0R<4:0>					0000
1644	RPB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB1R<4:0>					0000
1648	RPB2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB2R<4:0>					0000
164C	RPB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB3R<4:0>					0000
1650	RPB4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB4R<4:0>					0000
1654	RPB5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB5R<4:0>					0000
1658	RPB6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB6R<4:0>					0000
165C	RPB7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB7R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 14-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit
1 = Timer is enabled
0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when device enters Idle mode
0 = Continue operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit
In Asynchronous Timer mode:
1 = Asynchronous write to TMR1 register in progress
0 = Asynchronous write to TMR1 register complete
In Synchronous Timer mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK pin
00 = External clock comes from the SOSC

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

NOTES:

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DUALBUF	EXADR
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	CS2P(2)	CS1P(2)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read Cycle on PMP Bus bit
- 1 = Start a ready cycle on the PMP bus
- 0 = No effect

Note: This bit is cleared by hardware at the end of the read cycle when the BUSY bit (PMMODE<15>) is equal to '0'.

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit

This bit is only valid in Master mode.
- 1 = PMP uses separate registers for reads and writes
  Reads: PMRADDR and PMRDIN
  Writes: PMRWADDR and PMDOUT
- 0 = PMP uses legacy registers for reads and writes
  Reads/Writes: PMADDR and PMRDIN

bit 16 **EXADR:** Parallel Master Port Extended 24-bit Addressing bit (Master mode only)
- 1 = PMP 24-bit addressing is enabled
- 0 = PMP 24-bit addressing is disabled

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP is enabled
- 0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 25-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 20-16 **STRGSRC<4:0>:** Scan Trigger Source Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 period end
10010 = Output Compare 3 period end
10001 = Output Compare 2 period end
10000 = Output Compare 1 period end
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary PWM time base (Motor Control only)
01000 = Primary PWM time base (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: These triggers only apply to implemented analog inputs AN32-AN53. For AN0-AN27 refer to ADCTRG1-ADCTRG7.

bit 15 **ON:** ADC Module Enable bit
1 = ADC module is enabled
0 = ADC module is disabled

Note: The ON bit should be set only after the ADC module has been configured.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

REGISTER 25-22: ADCTRG5: ADC TRIGGER SOURCE 5 REGISTER

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC18<4:0>:** Trigger Source for Conversion of Analog Input AN18 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC17<4:0>:** Trigger Source for Conversion of Analog Input AN17 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC16<4:0>:** Trigger Source for Conversion of Analog Input AN16 Select bits
See bits 28-24 for bit value definitions.

Note 1: These bits are not available on 64-pin devices.

REGISTER 26-3: CxINT: CAN INTERRUPT REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF(1)	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 26-20 **Unimplemented:** Read as '0'

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CxCON<15>).

REGISTER 30-3: QEIxSTAT: QEIx STATUS REGISTER (CONTINUED)

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No Home event has occurred

bit 2 **HOMIEN:** Home Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **IDXIRQ:** Status Flag for Index Event Status bit
1 = Index event has occurred
0 = No Index event has occurred

bit 0 **IDXIEN:** Index Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This status bit in only applies to PIMOD<2:0> modes '011' and '100'.

REGISTER 31-24: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LEB<11:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LEB<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB<11:0>:** Leading-Edge Blanking Delay bits for Current-Limit and Fault Inputs bits

These bits specify the time period for which the selected current limit and fault signals are blanked or delayed following the selected edge transition of the PWM signals. This retriggerable counter has the PWM module clock source (SYSCLK) as the time base.

REGISTER 33-3: DEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-x	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	EJTAGBEN	—	—	—	—	—	—
23:16	r-1	r-1	R/P	R/P	R/P	R/P	R/P	R/P
	—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>	
15:8	R/P	R/P	R/P	R/P	r-y	R/P	r-1	r-1
	SMCLR	DBGPER<2:0>			—	FSLEEP	—	—
7:0	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN(1)	DEBUG<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** The reset value of this bit is the same as DEVSIGN0<31>.

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit
1 = Normal EJTAG functionality
0 = Reduced EJTAG functionality

bit 29-22 **Reserved:** Write as '1'

bit 21 **POSCBOOST:** Primary Oscillator Boost Kick Start Enable bit
1 = Boost the kick start of the oscillator
0 = Normal start of the oscillator

Note: For Revision A1 silicon, the POSBOOST bit should be set and do not use an external gain resistor (i.e., RSHUNT).

bit 20-19 **POSCGAIN<1:0>:** Primary Oscillator Gain Control bits
11 = Gain Level 3 (highest)
10 = Gain Level 2
01 = Gain Level 1
00 = Gain Level 0 (lowest)

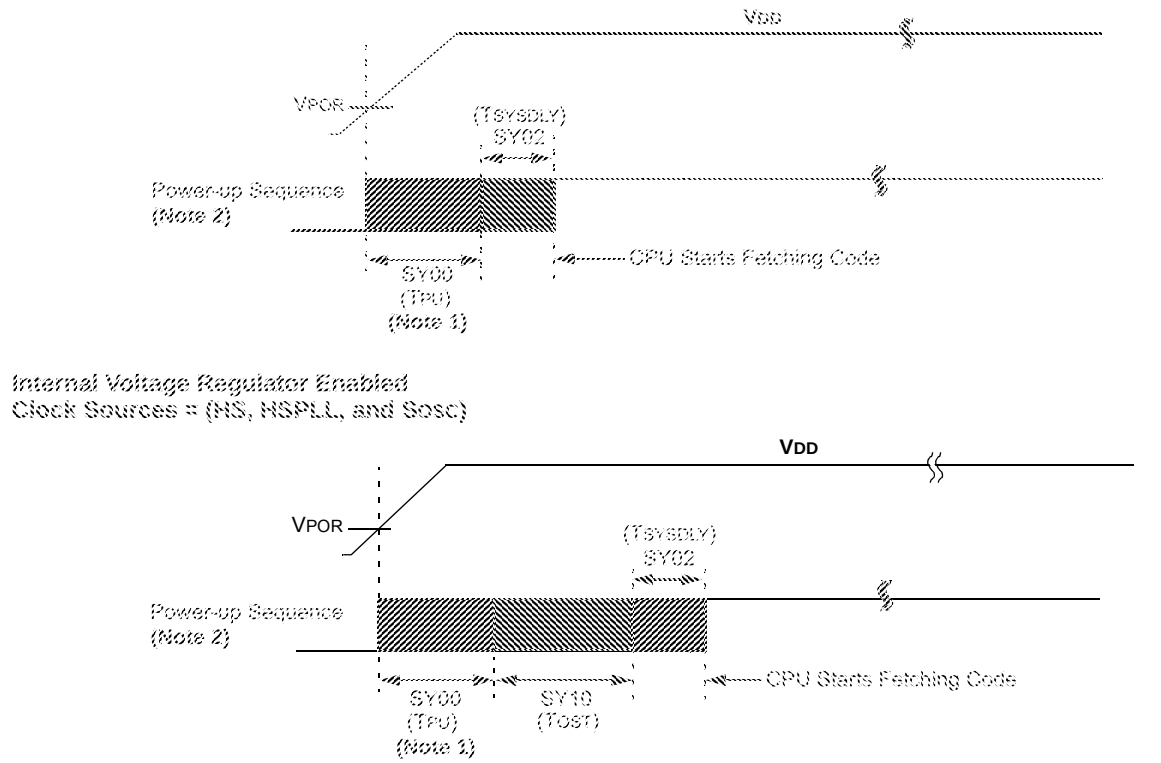
bit 18 **SOSCBOOST:** Secondary Oscillator Boost Kick Start Enable bit
1 = Boost the kick start of the oscillator
0 = Normal start of the oscillator

bit 17-16 **SOSCGAIN<1:0>:** Secondary Oscillator Gain Control bits
11 = Gain Level 3 (highest)
10 = Gain Level 2
01 = Gain Level 1
00 = Gain Level 0 (lowest)

bit 15 **SMCLR:** Soft Master Clear Enable bit
1 = $\overline{\text{MCLR}}$ pin generates a normal system Reset
0 = $\overline{\text{MCLR}}$ pin generates a POR Reset

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

FIGURE 36-4: POWER-ON RESET TIMING CHARACTERISTICS



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{DDMIN}$).

2: Includes interval voltage regulator stabilization delay.

FIGURE 36-16: CANx MODULE I/O TIMING CHARACTERISTICS

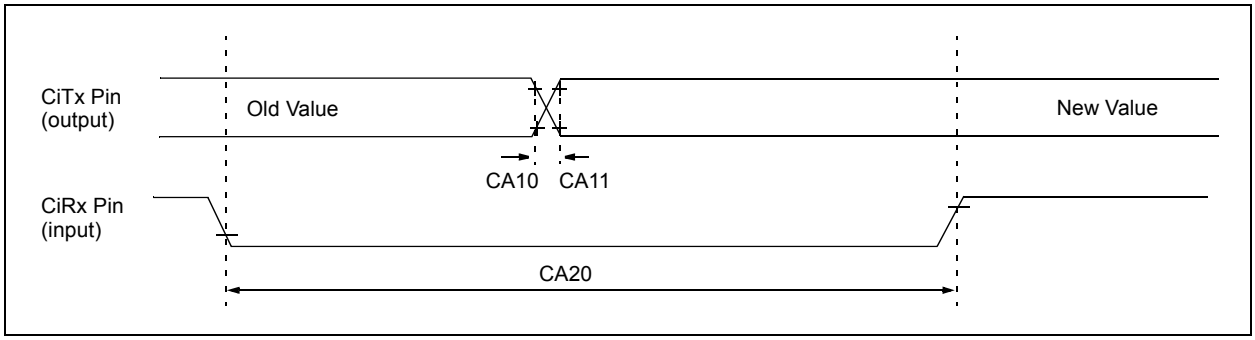


TABLE 36-38: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.