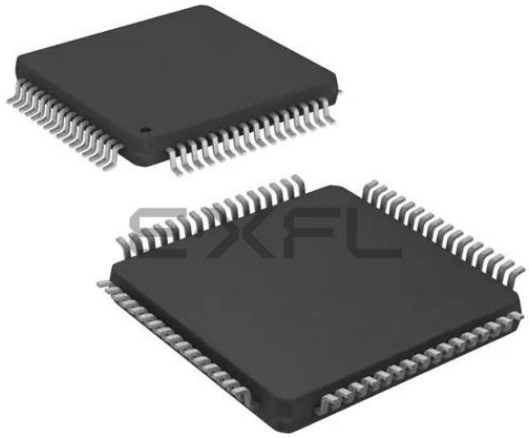

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	48
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 26x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpe064-e-pt

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 web site: http://www.microchip.com/pic32.

- **Section 1. "Introduction"** (DS60001127)
- **Section 4. "Prefetch Cache Module"** (DS60001119)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)
- **Section 39. "Op amp/Comparator"** (DS60001178)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 43. "Quadrature Encoder Interface (QEI)"** (DS60001346)
- **Section 44. "Motor Control PWM (MCPWM)** (DS60001393)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)
- **Section 58. "Data EEPROM"** (DS60001341)

3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: The microAptiv™ CPU core resources are available at: www.imgtec.com.

The MIPS32® microAptiv™ MCU Core is the heart of the PIC32MK GP/MC family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

Key features include:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 5):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
  - Virtual memory support
- microMIPS™ compatible instruction set:
  - Improves code size density over MIPS32, while maintaining MIPS32 performance.
  - Supports all MIPS32 instructions (except branch-likely instructions)
  - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
  - Stack pointer implicit in instruction
  - MIPS32 assembly and ABI compatible
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x32 multiply per clock
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - Hardware breakpoint supports both address match and address range triggering.
  - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
  - Real-time instruction program counter
  - Special events trace capability
  - Two performance counters with 34 user-selectable countable events
  - Disabled if the processor enters Debug mode
  - Program Counter sampling
- DSP ASE Extension:
  - Native fractional format data type operations
  - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
  - GPR-based shift
  - Bit manipulation
  - Compare-Pick
  - DSP Control Access
  - Indexed-Load
  - Branch
  - Multiplication of complex operands
  - Variable bit insertion and extraction
  - Virtual circular buffers
  - Arithmetic saturation and overflow handling
  - Zero-cycle overhead saturation and rounding operations
- Floating Point Unit (FPU):
  - 1985 IEEE-754 compliant Floating Point Unit
  - Supports single and double precision datatypes
  - 2008 IEEE-754 compatibility control of NaN handling and Abs/Neg instructions
  - Runs at 1:1 core/FPU clock ratio

REGISTER 5-8: NVMCON2: FLASH PROGRAMMING CONTROL REGISTER 2 (CONTINUED)

bit 13 **CREAD1:** Compare Read of Logic 1 bit(1)

1 = Compare Read is enabled (only if VERIFYREAD1 = 1)
0 = Compare Read is disabled

Compare Read 1 causes all bits in a Flash Word to be evaluated during the read. If all bits are '1', the lowest Word in the Flash Word evaluates to 0x00000001, all other words are 0x00010000. If any bit is '0', the read evaluates to 0x00000000 for all Words in the Flash Word.

bit 12 **VREAD1:** Verify Read of Logic 1 Control bit(1)

1 = Selects Erase Retry Procedure with Verify Read
0 = Selects Single Erase w/o Verify Read

When VREAD1 = 1, Flash wait state control is from the LPRDWS<4:0> bits for the panel containing NVMADDR.

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ERETRY<1:0>:** Erase Retry Control bits

11 = Erase strength for last retry cycle
10 = Erase strength for third retry cycle
01 = Erase strength for second retry cycle
00 = Erase strength for first retry cycle

The user application should start with '00' (first retry cycle) and move on to higher strength if the programming does not complete.

This bit is used only when VREAD1 = 1 and when VREAD1 = 1.

bit 7-6 **SWAPLOCK<1:0>:** Flash Memory Swap Lock Control bits

11 = PFSWAP and BFSWAP are not writable and SWAPLOCK is not writable
10 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable
01 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable
00 = PFSWAP and BFSWAP are writable and SWAPLOCK is writable

bit 5-0 **Unimplemented:** Read as '0'

Note 1: This bit can only be modified when the WREN bit = 0, and the NVMKEY unlock sequence is satisfied.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0450	IPC49	31:16	—	—	—	OC10IP<2:0>			OC10IS<1:0>		—	—	—	IC10IP<2:0>			IC10IS<1:0>		0000
		15:0	—	—	—	IC10EIP<2:0>			IC10EIS<1:0>		—	—	—	—	—	—	—	—	0000
0460	IPC50	31:16	—	—	—	IC12EIP<2:0>			IC12EIS<1:0>		—	—	—	OC11IP<2:0>			OC11IS<1:0>		0000
		15:0	—	—	—	IC11IP<2:0>			IC11IS<1:0>		—	—	—	IC11EIP<2:0>			IC11EIS<1:0>		0000
0470	IPC51	31:16	—	—	—	IC13IP<2:0>			IC13IS<1:0>		—	—	—	IC13EIP<2:0>			IC13EIS<1:0>		0000
		15:0	—	—	—	OC12IP<2:0>			OC12IS<1:0>		—	—	—	IC12IP<2:0>			IC12IS<1:0>		0000
0480	IPC52	31:16	—	—	—	OC14IP<2:0>			OC14IS<1:0>		—	—	—	C14IP<2:0>			C14IS<1:0>		0000
		15:0	—	—	—	IC14EIP<2:0>			IC14EIS<1:0>		—	—	—	OC13IP<2:0>			OC13IS<1:0>		0000
0490	IPC53	31:16	—	—	—	IC16EIP<2:0>			IC16EIS<1:0>		—	—	—	OC15IP<2:0>			OC15IS<1:0>		0000
		15:0	—	—	—	IC15IP<2:0>			IC15IS<1:0>		—	—	—	IC15EIP<2:0>			IC15EIS<1:0>		0000
04A0	IPC54	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	OC16IP<2:0>			OC16IS<1:0>		—	—	—	IC16IP<2:0			IC16IS<1:0>		0000
04B0	IPC55	31:16	—	—	—	SPI4TXIP<2:0>			SPI4TXIS<1:0>		—	—	—	SPI4RXIP<2:0>			SPI4RXIS<1:0>		0000
		15:0	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
04C0	IPC56	31:16	—	—	—	SPI6EIP<2:0>			SPI6EIS<1:0>		—	—	—	SPI5TXIP<2:0>			SPI5TXIS<1:0>		0000
		15:0	—	—	—	SPI5RXIP<2:0>			SPI5RXIS<1:0>		—	—	—	SPI5EIP<2:0>			SPI5EIS<1:0>		0000
04D0	IPC57	31:16	—	—	—	—	—	—	—	—	—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	SPI6TXIP<2:0>			SPI6TXIS<1:0>		—	—	—	SPI6RXIP<2:0>			SPI6RXIS<1:0>		0000
0510	IPC61	31:16	—	—	—	—	—	—	—	—	—	—	—	AD1DC4IP<2:0>			AD1DC4IS<1:0>		0000
		15:0	—	—	—	AD1DC3IP<2:0>			AD1DC3IS<1:0>		—	—	—	USB2IP<2:0>(2)			USB2IS<1:0>(2)		0000
0530	IPC63	31:16	—	—	—	—	—	—	—	—	—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0540	OFF000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0544	OFF001	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0548	OFF002	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 8-8: OFFx: INTERRUPT VECTOR ADDRESS OFFSET REGISTER (x = 0-190)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	VOFF<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VOFF<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	VOFF<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 17-1 **VOFF<17:1>:** Interrupt Vector 'x' Address Offset bits

bit 0 **Unimplemented:** Read as '0'

TABLE 13-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT3	INT3R<3:0>	INT3R	0000 = RPA1
T3CK	T3CKR<3:0>	T3CKR	0001 = RPB5
T7CK	T7CKR<3:0>	T7CKR	0010 = RPB1
IC3	IC3R<3:0>	IC3R	0011 = RPB11
IC8	IC8R<3:0>	IC8R	0100 = RPB8
IC11	IC11R<3:0>	IC11R	0101 = RPA8
IC16	IC16R<3:0>	IC16R	0110 = RPC8
$\overline{\text{U1CTS}}$	U1CTSR<3:0>	U1CTSR	0111 = RPB12
U2RX	U2RXR<3:0>	U2RXR	1000 = RPA12
$\overline{\text{U5CTS}}$	U5CTSR<3:0>	U5CTSR	1001 = RPD6
SDI2	SDI2R<3:0>	SDI2R	1010 = RPG7
SDI4	SDI4R<3:0>	SDI4R	1011 = RPG0(1)
SCK6	SCK6R<3:0>	SCK6R	1100 = RPE1(1)
QEB1	QEB1R<3:0>	QEB1R	1101 = RPA14(1)
INDX2	INDX2R<3:0>	INDX2R	1110 = Reserved
QEB3	QEB3R<3:0>	QEB3R	1111 = Reserved
INDX4	INDX4R<3:0>	INDX4R	
QEB5	QEB5R<3:0>	QEB5R	
INDX6	INDX6R<3:0>	INDX6R	
C2RX	C2RXR<3:0>	C2RXR	
FLT2	FLT2R<3:0>	FLT2R	

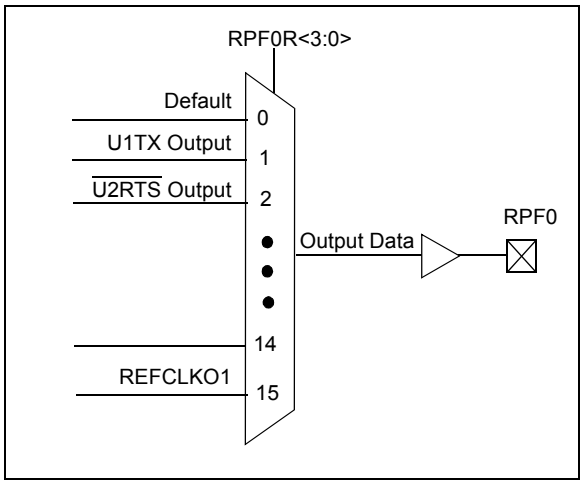
Note 1: This selection is not available on 64-pin devices.

13.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 13-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 13-2 and Figure 13-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 13-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



13.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The PIC32MK GP/MC devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

13.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting the IOLOCK bit prevents writes to the control registers and clearing the IOLOCK bit allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

13.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If the IOLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

TABLE 13-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA0	RPA0R	RPA0R<4:0>	00000 = Off 00001 = U1TX 00010 = U2RTS 00011 = SDO1 00100 = SDO2 00101 = OCI 00110 = OC7 00111 = C2OUT 01000 = C4OUT 01001 = OC13 01010 = Reserved 01011 = U5RTS 01100 = C1TX 01101 = Reserved 01110 = SDO3 01111 = SCK4 10000 = SDO5 10001 = SS6 10010 = REFCLKO4 10011 = Reserved 10100 = QEICMP1 10101 = QEICMP5 10110 = Reserved . . . 11111 = Reserved
RPB3	RPB3R	RPB3R<4:0>	
RPB4	RPB4R	RPB4R<4:0>	
RPB15	RPB15R	RPB15R<4:0>	
RPB7	RPB7R	RPB7R<4:0>	
RPC7	RPC7R	RPC7R<4:0>	
RPC0	RPC0R	RPC0R<4:0>	
RPA11	RPA11R	RPA11R<4:0>	
RPD5	RPD5R	RPD5R<4:0>	
RPG6	RPG6R	RPG6R<4:0>	
RPF1	RPF1R	RPF1R<4:0>	
RPE0(1)	RPE0R(1)	RPE0R<4:0> (1)	
RPA15(1)	RPA15R(1)	RPA15R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-7: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	—	—	—	TRISD8(2)	—	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	—	F1FE
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	—	—	—	RD8(2)	—	RD6	RD5	RD4	RD3	RD2	RD1	—	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	—	—	—	LATD8(2)	—	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	—	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	—	—	—	ODCD8(2)	—	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	—	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	—	—	—	CNPUD8(2)	—	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	—	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	—	—	—	CNPDD8(2)	—	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	—	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	—	—	—	CNIED8(2)	—	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	—	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	—	—	—	CN STATD8(2)	—	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	—	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	—	—	—	CNNED8(2)	—	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	—	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	—	—	—	CNFD8(2)	—	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	—	0000
03C0	SRCON0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR0D8(2)	—	SR0D6	SR0D5	SR0D4	SR0D3	SR0D2	SR0D1	—	0000
03D0	SRCON1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR1D8(2)	—	SR1D6	SR1D5	SR1D4	SR1D3	SR1D2	SR1D1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on general purpose devices.

TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
16D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD4R<4:0>					0000
16D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD5R<4:0>					0000
16D8	RPD6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD6R<4:0>					0000
1700	RPE0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE0R<4:0>					0000
1704	RPE1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE1R<4:0>					0000
1738	RPE14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF14R<4:0>					0000
173C	RPE15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE15R<4:0>					0000
1740	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF0R<4:0>					0000
1744	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF1R<4:0>					0000
1780	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG0R<4:0>					0000
1784	RPG1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG1R<4:0>					0000
1798	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG6R<4:0>					0000
179C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG7R<4:0>					0000
17A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG8R<4:0>					0000
17A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG9R<4:0>					0000
17B0	RPG12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG12R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

14.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the low-power Secondary Oscillator (SOSC) for real-time clock applications.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

14.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers
- Asynchronous mode can be used with the SOSC to function as a real-time clock
- ADC event trigger

14.2 TImer1 Usage Model Guidelines

14.2.1 EXTERNAL CLOCK MODE OPERATION

When the Timer is operating with an external clock mode with the TCS bit (TxCON<1>) = 1, the mode bits of the TxCON register must be initialized using a separate Write operation from that used to enable the Timer. Specifically, the TCS, TSYNC, etc. bits must be written first, and then the ON bit (TxCON<15>) must be set in a subsequent write.

Once the ON bit is set, any writes to the TxCON register may cause erroneous counter operation.

Note: The ON bit should be clear when updates are made to any other bits in the TxCON register.

14.2.2 ASYNCHRONOUS MODE OPERATION

When writing the ON bit when the Timer is configured in Asynchronous mode or in an external clock mode with the prescaler enabled, the act of setting the ON bit does not take effect until two rising edges of the external clock input have occurred.

14.2.3 ASYNCHRONOUS MODE OPERATION WITH A PENDING TMRx REGISTER WRITE

When the Timer is configured in Asynchronous mode and the Timer is attempting to write to the TMRx register while a previous write is awaiting synchronization, the value written to the timer can become corrupted.

To ensure that writes will not cause the TMRx value to become corrupted, the TWDIS bit (TxCON<12>), when set, will ignore a write to the TMRx register when a previous write to the TMRx register is awaiting synchronization into the Asynchronous Timer Clock domain.

The TWIP bit (TxCON<11>) indicates when write synchronization is complete, and it is safe to write another value to the timer.

14.2.4 PRx REGISTER WRITES

Writing to the PRx register while the Timer is active, may cause erratic operation.

REGISTER 19-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER ('x' = 1-16)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT(1)	OCTSEL(2)	OCM<2:0>		

Legend:	HS = Set in hardware	HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(1)
- 1 = PWM Fault condition has occurred (cleared in HW only)
- 0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit(2)
- 1 = Timery is the clock source for this Output Compare module
- 0 = Timerx is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

Note 1: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

2: Refer to Table 19-1 for Timerx and Timery selections.

REGISTER 25-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 21 **DIFF10:** AN10 Mode bit
1 = Selects AN10 differential input pair as AN10+ and AN1-
0 = AN10 is using Single-ended mode

bit 20 **SIGN10:** AN10 Signed Data Mode bit
1 = AN10 is using Signed Data mode
0 = AN10 is using Unsigned Data mode

bit 19 **DIFF9:** AN9 Mode bit
1 = Selects AN9 differential input pair as AN9+ and AN1-
0 = AN9 is using Single-ended mode

bit 18 **SIGN9:** AN9 Signed Data Mode bit
1 = AN9 is using Signed Data mode
0 = AN9 is using Unsigned Data mode

bit 17 **DIFF8:** AN 8 Mode bit
1 = Selects AN8 differential input pair as AN8+ and AN1-
0 = AN8 is using Single-ended mode

bit 16 **SIGN8:** AN8 Signed Data Mode bit
1 = AN8 is using Signed Data mode
0 = AN8 is using Unsigned Data mode

bit 15 **DIFF7:** AN7 Mode bit
1 = Selects AN7 differential input pair as AN7+ and AN1-
0 = AN7 is using Single-ended mode

bit 14 **SIGN7:** AN7 Signed Data Mode bit
1 = AN7 is using Signed Data mode
0 = AN7 is using Unsigned Data mode

bit 13 **DIFF6:** AN6 Mode bit
1 = Selects AN6 differential input pair as AN6+ and AN1-
0 = AN6 is using Single-ended mode

bit 12 **SIGN6:** AN6 Signed Data Mode bit
1 = AN6 is using Signed Data mode
0 = AN6 is using Unsigned Data mode

bit 11 **DIFF5:** AN5 Mode bit
1 = Selects AN5 differential input pair as AN5+ and AN11-
0 = AN5 is using Single-ended mode

bit 10 **SIGN5:** AN5 Signed Data Mode bit
1 = AN5 is using Signed Data mode
0 = AN5 is using Unsigned Data mode

bit 9 **DIFF4:** AN4 Mode bit
1 = Selects AN4 differential input pair as AN4+ and AN10-
0 = AN4 is using Single-ended mode

bit 8 **SIGN4:** AN4 Signed Data Mode bit
1 = AN4 is using Signed Data mode
0 = AN4 is using Unsigned Data mode

bit 7 **DIFF3:** AN3 Mode bit
1 = Selects AN3 differential input pair as AN3+ and AN27-
0 = AN3 is using Single-ended mode

bit 6 **SIGN3:** AN3 Signed Data Mode bit
1 = AN3 is using Signed Data mode
0 = AN3 is using Unsigned Data mode

REGISTER 25-13: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	AIRDY27	AIRDY26	AIRDY25	AIRDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY23(1)	AIRDY22(1)	AIRDY21(1)	AIRDY20(1)	AIRDY19	AIRDY18	AIRDY17	AIRDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY15	AIRDY14	AIRDY13	AIRDY12	AIRDY11	AIRDY10	AIRDY9	AIRDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY7	AIRDY6	AIRDY5	AIRDY4	AIRDY3	AIRDY2	AIRDY1	AIRDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AIRDY27:AIRDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-14: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AIRDY53	AIRDY52	AIRDY51	AIRDY50	AIRDY49	AIRDY48
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	AIRDY47(1)	AIRDY46(1)	AIRDY45(1)	—	—	—	AIRDY41(1)	AIRDY40(1)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0
	AIRDY39(1)	AIRDY38(1)	AIRDY37(1)	AIRDY36(1)	AIRDY35(1)	AIRDY34(1)	AIRDY33(1)	—

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY53:AIRDY45:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

bit 12-10 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY41:AIRDY33:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-35: ADCEIEN2: ADC EARLY INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	EIEN53	EIEN52	EIEN51	EIEN50	EIEN49	EIEN48
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	EIEN47(1)	EIEN46(1)	EIEN45(1)	—	—	—	EIEN41(1)	EIEN40(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EIEN39(1)	EIEN38(1)	EIEN37(12)	EIEN36(1)	EIEN35(1)	EIEN34(1)	EIEN33(1)	—

Legend:	HS = Hardware Set	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-13 **EIEN53:EIEN45:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 44-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9-1 **EIEN41:EIEN33:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 44-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

REGISTER 26-1: CxCON: CAN MODULE CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 26-10: CxFLTCON0: CAN FILTER CONTROL REGISTER 0 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 33-3: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits
1xx = Allow CPU access to Permission Group 2 permission regions
x1x = Allow CPU access to Permission Group 1 permission regions
xx1 = Allow CPU access to Permission Group 0 permission regions
0xx = Deny CPU access to Permission Group 2 permission regions
x0x = Deny CPU access to Permission Group 1 permission regions
xx0 = Deny CPU access to Permission Group 0 permission regions

Note: When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

bit 10 **FSLEEP:** Flash Sleep Mode bit
1 = Flash is powered down when the device is in Sleep mode
0 = Flash power down is controlled by the VREGS bit (PWRCON<0>)

bit 9-7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
1 = Boot code and Exception code is MIPS32
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit(1)
1 = JTAG is enabled
0 = JTAG is disabled

Note: On Reset, this Configuration bit is copied into JTAGEN (CFGCON<3>). If JTAGEN (DEVCFG0<2>) = 0, the JTAGEN bit cannot be set to '1' by the user application at run-time, as JTAG is always disabled. However, if JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time as by simply writing JTAGEN (CFGCON<3> as required.

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
11 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Disabled
10 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Enabled
01 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Disabled
00 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Enabled

Note: When the FJTAGEN or JTAGEN bits are equal to '0', this prevents 4-wire JTAG debugging, but not PGECx/PGEDx debugging.

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

TABLE 36-29: OP AMP SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Comments**
OA1	VCMR	Common Mode Input Voltage Range	AVSS	—	AVDD	V	—
OA2	CMRR	Common Mode Rejection Ratio	—	70	—	dB	VCM = AVDD/2
OA3	VOFFSET	Op amp Offset Voltage	-5	—	5	mV	—
OA4	VGAINCL	Closed Loop Voltage Gain	8	—	—	V	Non-inverting configuration, RF/RI ≥ 8
OA5	ILKG	Input leakage current	—	—	See IIL in Table 36-9	nA	—
OA6	PSRR	Power Supply Rejection Ratio	—	-75	—	dB	—
OA7	VGAIN	Open Loop Voltage Gain	—	90	—	dB	—
OA8	VOH	Amplifier Output Voltage High	—	AVDD - 0.077	—	V	ISOURCE ≤ 500 µA
			—	AVDD - 0.037	—	V	ISOURCE ≤ 200 µA
			—	AVDD - 0.018	—	V	ISOURCE ≤ 100 µA
OA9	VOL	Amplifier Output Voltage Low	—	AVSS + 0.077	—	V	ISINK ≤ 500 µA
			—	AVSS + 0.037	—	V	ISINK ≤ 200 µA
			—	AVSS + 0.018	—	V	ISINK ≤ 100 µA
OA10	TON	Enable to Valid Output	—	10	—	µs	—
OA11	TOFF	Disable to Outputs Disabled	—	100	—	ns	—
OA11	IOS	Input Offset Current	—	See IIL in Table 36-9	—	—	—
OA13	IB	Input Bias Current	—	See IIL in Table 36-9	—	—	—
OA14	SR	Slew Rate	7.0	9.0	—	V/µs	Measured with a 0.5V to 2.5V step change
OA15	GBW	Gain Bandwidth	10.0	—	—	MHz	—
OA16	AV	Gain	8.0	—	—	V/V	Minimum op-amp stable gain
OA17	PM	Phase Margin	43	65	—	Degrees	—

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, Op amp/Comparator, and Comparator voltage reference, will have degraded performance. Refer to parameter BO10 in Table 36-5 for the minimum and maximum BOR values.

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.