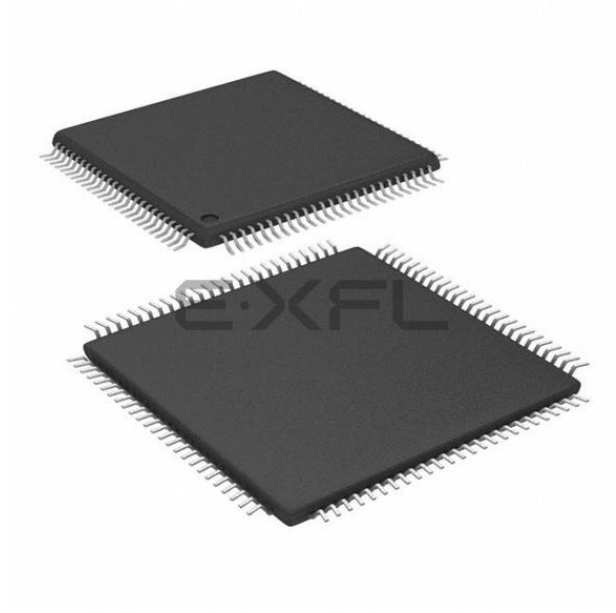
Microchip Technology - PIC32MK1024GPE100-E/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	77
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpe100-e-pt

TABLE 1-6: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTD					
RD1	6	—	I/O	ST	PORTD is a bidirectional I/O port
RD2	7	—	I/O	ST	
RD3	8	—	I/O	ST	
RD4	9	—	I/O	ST	
RD5	82	53	I/O	ST	
RD6	83	54	I/O	ST	
RD8(3)	68	42	I/O	ST	
RD12	79	—	I/O	ST	
RD13	80	—	I/O	ST	
RD14	47	—	I/O	ST	
RD15	48	—	I/O	ST	
PORTE					
RE0	52	—	I/O	ST	PORTE is a bidirectional I/O port
RE1	53	—	I/O	ST	
RE8	18	—	I/O	ST	
RE9	19	—	I/O	ST	
RE12	41	27	I/O	ST	
RE13	42	28	I/O	ST	
RE14	43	29	I/O	ST	
RE15	44	30	I/O	ST	
PORTF					
RF0	87	58	I/O	ST	PORTF is a bidirectional I/O port
RF1	88	59	I/O	ST	
RF5	61	—	I/O	ST	
RF6	91	—	I/O	ST	
RF7	92	—	I/O	ST	
RF9	28	—	I/O	ST	
RF10	29	—	I/O	ST	
RF12	40	—	I/O	ST	
RF13	39	—	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R/W-y
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC(1)
15:8	R-y	R-y	R-1	R-1	R-1	R-1	U-0	R-1
	ISA<1:0>(1)		ULRI	RXI	DSP2P	DSPP	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '1' to indicate the presence of the Config4 register

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8-bits in width

bit 20-18 **MMAR<2:0>:** microMIPS Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS® MCU™ ASE Implemented bit
1 = MCU ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit(1)
1 = microMIPS is used on entrance to an exception vector
0 = MIPS32 ISA is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits(1)
11 = Both MIPS32 and microMIPS are implemented; microMIPS is used when coming out of reset
10 = Both MIPS32 and microMIPS are implemented; MIPS32 ISA used when coming out of reset

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11 **DSP2P:** MIPS DSP ASE Revision 2 Presence bit
1 = DSP Revision 2 is present

bit 10 **DSPP:** MIPS DSP ASE Presence bit
1 = DSP is present

bit 9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace® hardware is present
1 = The iFlowtrace® 2.0 hardware is implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4 KB page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

Note 1: These bits are set based on the value of the BOOTISA Configuration bit (DEVCFG0<6>).

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1390	DCH4SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
13A0	DCH4DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
13B0	DCH4SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
13C0	DCH4DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
13D0	DCH4SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
13E0	DCH4DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
13F0	DCH4CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1400	DCH4CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1410	DCH4DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1420	DCH5CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1430	DCH5ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1440	DCH5INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1450	DCH5SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1460	DCH5DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1470	DCH5SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1480	DCH5DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1490	DCH5SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = All 16-bit of address are multiplexed with the 16-bits of data (PMA<15:0> or PMD<15:0>) using two phases
- 10 = All 16-bit of address are multiplexed with the lower 8-bits of data (PMA<15:8>, PMA<7:0>, or PMD<7:0>) using three phases
- 01 = Lower 8-bits of address are multiplexed with lower 8-bits of data (PMA<7:0> or PMD<7:0>)
- 00 = Address and data pins are not multiplexed

Note: The ADRMUX bits are independent of the MODE16 bit. Therefore, if ADDRMUX = 11 and MODE16 = 0, only the lower 8 bits of the address will be driven out. Additionally, if ADDRMUX = 10 and MODE16 = 1, the upper 8 bits of the data will be driven out on PMD<15:8>.

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port is enabled
- 0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
- 1 = PMRD/PMWR port is enabled
- 0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
- 11 = Reserved
- 10 = PMCS2/(a) and PMCS1/(a) used as Chip Select
- 01 = PMCS2/(a) used as Chip Select, PMCS1/(a) used as address bit 14 or (22 when EXADR = 1)
- 00 = PMCS2/(a) and PMCS1/(a) used as address bits (15 and 14) or (23 and 22 when EXADR = 1)

Note: When the CSx bit is used as an address, it is subject to auto-increment/decrement.

bit 5 **ALP:** Address Latch Polarity bit(2)
- 1 = Active-high (PMCS2) / (PMPCS2a)
- 0 = Active-low (PMCS2) / (PMPCS2a)

Note: When the PMCS2/(a) pin is used as an address pin, the setting of the CS2P bit does not affect the polarity.

bit 4 **CS2P:** Chip Select 1 Polarity bit(2)
- 1 = Active-high (PMCS2) / (PMPCS2a)
- 0 = Active-low (PMCS2) / (PMPCS2a)

When the PMCS2/PMPCS2a pin is used as an address pin, the setting of the CS2P bit does not affect the polarity.

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
- 1 = Active-high ($\overline{\text{PMCS1}}$) / (PMPCS1a)
- 0 = Active-low (PMCS1) / (PMPCS1a)

Note: When the PMCS1/PMPCS1a pin is used as an address pin, the setting of the CS1P bit does not affect the polarity.

bit 2 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 26-2: CxCFG: CAN BAUD RATE CONFIGURATION REGISTER ('x' = 1-4) (CONTINUED)

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits(3)
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits
111111 = TQ = (2 x 64) / PBCLK5
111110 = TQ = (2 x 63) / PBCLK5
•
•
•
000001 = TQ = (2 x 2) / PBCLK5
000000 = TQ = (2 x 1) / PBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

REGISTER 26-9: CxRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER ('x' = 1-4; 'n' = 0, 1, 2 OR 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SID<10:3>							
23:16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SID<2:0>			—	MIDE	—	EID<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include the SIDx bit in filter comparison
0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include the EIDx bit in filter comparison
0 = The EIDx bit is a 'don't care' in filter operation

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

REGISTER 26-18: CxFIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' ('x' = 1-4; 'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CxFIFOUAn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CxFIFOUAn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CxFIFOUAn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0(1)	R-0(1)
	CxFIFOUAn<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CxFIFOUAn<31:0>:** CANx FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 27-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation of all Op amp/Comparators when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op amp/Comparator 5 through Comparator 1 Output Status bit
When CPOL = 0:
1 = $V_{IN+} > V_{TH+}$
0 = $V_{IN+} < V_{TH-}$
When CPOL = 1:
1 = $V_{IN+} < V_{TH-}$
0 = $V_{IN+} > V_{TH+}$

NOTES:

REGISTER 30-5: VELxCNT: VELOCITY COUNTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **VELCNT<31:0>:** 32-bit Velocity Counter bits

The velocity counter is automatically cleared after every processor read of the velocity counter. It is not reset by the index input or otherwise affected by any of the PIMOD<2:0> specified modes. The contents of the counter represents the distance traveled during the time between samples. Velocity equals the distance traveled per unit of time. The velocity counter can save the application software the trouble of performing 32-bit math operations between current and previous position counter values to calculate velocity. If the velocity counter rolls over from 0x7FFFFFFF to 0x80000000, or from 0x80000000 to 0x7FFFFFFF, an overflow/underflow condition is detected. If the VELOVIEN bit is set in the QEISTAT register, an interrupt will be generated.

31.1 PWM Faults

The PWM module incorporates multiple external Fault inputs to include FLT1 and FLT2, which are remappable using the PPS feature, and FLT15, which has been implemented with Class B safety features, and is available on a fixed pin at reset for Fault detection.

Fault pins are selectable for active level (active high or low). FLT pins provide a safe and reliable way to shut down the PWM outputs, tri-state, when the Fault input is asserted. Therefore, the user should provide the necessary external pull-up or pull-down to disable the high or low side FETs in motor control applications.

31.1.1 PWM FAULTS AT RESET

During any reset event, the PWM module maintains ownership of the Class B fault FLT15. At reset, this fault is enabled in latched mode to guarantee the fail-safe power-up of the application. The application software must clear the PWM fault before enabling the High-Speed Motor Control PWM module. To clear the fault condition, the FLT15 pin must first be pulled low externally or the internal pull down resistor in the CNPDx register can be enabled.

Note:	The Fault mode may be changed using the FLTMOD<1:0> bits (IOCONx<17:16>) regardless of the state of FLT15.

31.1.2 WRITE-PROTECTED REGISTERS

Write protection is implemented for the IOCONx register. The write protection feature prevents any inadvertent writes. This protection feature can be controlled by the PWMLOCK Configuration bit (DEVCFG3<20>). The default state of the write protection feature is disabled (PWMLOCK = 1). The write protection feature can be enabled by configuring the PWMLOCK = 0.

To gain write access, the application software must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. Every write to the IOCONx register requires a prior unlock operation.

The unlocking sequence is described in Example 31-1.

Figure 31-2 shows the register interconnection diagram for the Motor Control PWM module.

EXAMPLE 31-1: PWM WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
Untested Code – For Information Purposes Only
; In the default Reset state, the FLT15 pin must be pulled low externally to clear and disable
; the fault.
; Writing to IOCONx register requires unlock sequence
di      v1
ehb                         ;Disable interrupts
mov     #0xXXXX,r3          ;Move desired IOCON4 register data to r3 register
mov     #0xabcd,r1          ;Load first unlock key to r1 register
mov     #0x4321,r2          ;Load second unlock key to r2 register
mov     r1, PWMKEY          ;Write first unlock key to PWMKEY register
mov     r2, PWMKEY          ;Write second unlock key to PWMKEY register
mov     r3,IOCON4           ;Write desired value to IOCON SFR for channel 4
mfc0    v0,c0_status
ori     v0,v0,0x1
mtc0    v0,c0_status
ehb                         ;Re-enable Interrupts
```

TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A9A0	AUXCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A9B0	PTMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A9C0	PWMCON10	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A9D0	IOCON10	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A9E0	PDC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A9F0	SDC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
AA00	PHASE10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
AA10	DTR10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<15:0>																0000
AA20	ALTDTR10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<15:0>																0000
AA30	DTCOMP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
AA40	TRIG10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
AA50	TRGCON10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
AA60	STRIG10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
AA70	CAP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
AA80	LEBCON10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
AA90	LEBDLY10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
AAA0	AUXCON10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: '—' = unimplemented; read as '0'.

REGISTER 31-1: PTCON: PWM PRIMARY TIME BASE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	HS/HC-0	U-0	U-0
	PTEN	—	PTSIDL	SESTAT(1)	SEIEN(3)	PWMRDY	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCLKDIV<2:0>(2)			SEVTPS<3:0>(2)			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

Note: Many of the PWM registers and/or bits as designated, do not allow updates once a PWM module is enabled. Therefore, it is recommended that the user application initialize all required PWM registers before setting the PTEN bit equal to '1'.

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit(1)
1 = Special Event Interrupt is pending
0 = Special Event Interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special Event Interrupt is enabled
0 = Special Event Interrupt is disabled

bit 10 **PWMRDY:** PWM Module Status bit
1 = PWM module is ready and operation has begun
0 = PWM module is not ready

bit 9-7 **Unimplemented:** Read as '0'

Note 1: The SESTAT bit is cleared by clearing the SEIEN bit and the corresponding bit in the IFSx register.

2: The SEVTPS<3:0> and PCLKDIV<2:0> bits should be changed only when the PTEN bit (PTCON<15>) = 0.

3: To clear the Primary Special Event Interrupt the user application must do the following:
1) Clear the SEIEN bit by setting it to '0'.
2) Clear the Primary Special Event Interrupt flag by setting IFS5<11> = 0.
3) Re-enabling the PTCON register by setting the SEIEN equal to '1' if desired.
The user application will not be able to clear the Primary Special Event Interrupt flag as long as the SEIEN bit is equal to '1'.

REGISTER 31-6: STPER: SECONDARY MASTER TIME BASE PERIOD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STPER<15:8>(1,2,4)							
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0(3)	R/W-0(3)	R/W-0(3)
	STPER<7:0>(1,2,4)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **STPER<15:0>:** Secondary Master Time Base Period Value bits(1,2,4)

Note 1: Minimum LSb = 1/FSYSCLK.

2: Minimum value is 0x0008.

3: If a period value lesser than 0x0008 is chosen, the internal hardware forcefully sets the period to a minimum value of 0x0008.

4: STPER = (FSYSCLK/(FPWM * PCLKDIV<2:0> bits (PTCON<6:4>)).
FPWM = User-desired PWM Frequency.

REGISTER 31-7: SSEVTCMP: PWM SECONDARY SPECIAL EVENT COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEVTCMP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEVTCMP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SSEVTCMP<15:0>:** Secondary Special Event Compare Value bits

The secondary special event trigger allows analog-to-digital conversions to be synchronized to the secondary master PWM time base. The analog-to-digital sampling and conversion time may be programmed to occur at any point within the PWM period.

FIGURE 36-14: QEI MODULE EXTERNAL CLOCK TIMING CHARACTERISTICS

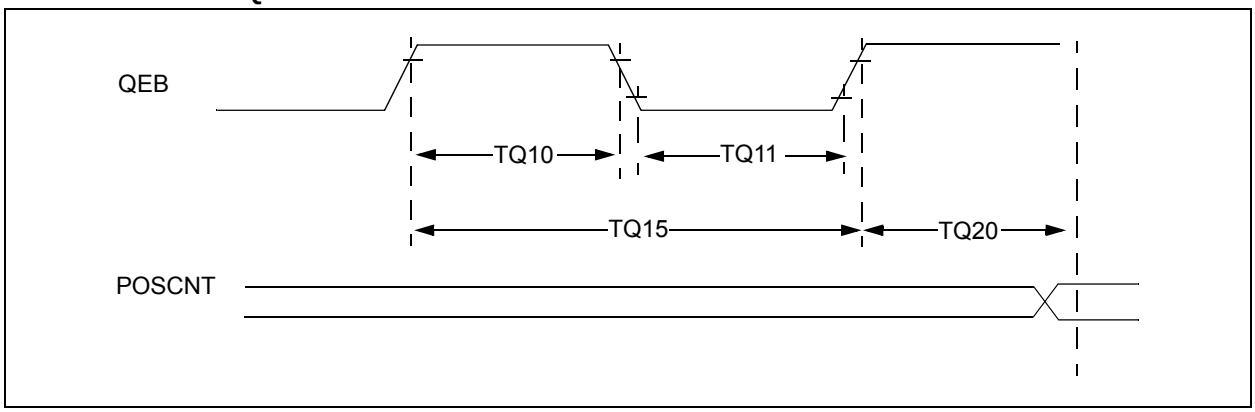


TABLE 36-36: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	[(12.5 or 0.5 TCY) / N] + 25	—	—	ns	Must also meet parameter TQ15. N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	[(12.5 or 0.5 TCY) / N] + 25	—	—	ns	Must also meet parameter TQ15. N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	[(25 or TCY) / N] + 50	—	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TCY	—	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: N = Index Channel Digital Filter Clock Divide Select bits.

TABLE 36-41: ADC SAMPLE TIMES WITH CVD ENABLED

AC CHARACTERISTICS[2]			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.[1]**	**Max.**	**Units**	**Conditions**
AD60a	TSAMP	Sample Time for ADC7 (Class 2 and Class 3 Inputs) with the CVDEN bit (ADCCON1<11>) = 1	8	—	—	TAD	Source Impedance ≤ 200Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001
			9				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			11				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			12				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			14				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			17				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			10	—	—	TAD	Source Impedance ≤ 500Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001
			12				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			14				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			18				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			19				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			21				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			13	—	—	TAD	Source Impedance ≤ 1 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			18				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			21				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			23				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			26				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			28				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			41	—	—	TAD	Source Impedance ≤ 5 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001
			48				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			56				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			63				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			70				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			78				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			85				CVDCPL<2:0> (ADCCON2<28:26>) = 111

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 36-43: CTMU CURRENT SOURCE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU CURRENT SOURCE							
CTMU0	RES	Resolution	-2	—	+2	ºC	3.3V @ -40ºC to 125ºC
CTMUI1	IOUT1	Base Range(1)	—	0.55	—	µA	CTMUCON<1:0> = 01
CTMUI2	IOUT2	10x Range(1)	—	5.5	—	µA	CTMUCON<1:0> = 10
CTMUI3	IOUT3	100x Range(1)	—	55	—	µA	CTMUCON<1:0> = 11
CTMUI4	IOUT4	1000x Range(1)	—	550	—	µA	CTMUCON<1:0> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage(1,2)	—	0.598	—	V	TA = +25ºC, CTMUCON<1:0> = 01
			—	0.658	—	V	TA = +25ºC, CTMUCON<1:0> = 10
			—	0.721	—	V	TA = +25ºC, CTMUCON<1:0> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change(1,2)	—	-1.92	—	mV/ºC	CTMUCON<1:0> = 01
			—	-1.74	—	mV/ºC	CTMUCON<1:0> = 10
			—	-1.56	—	mV/ºC	CTMUCON<1:0> = 11

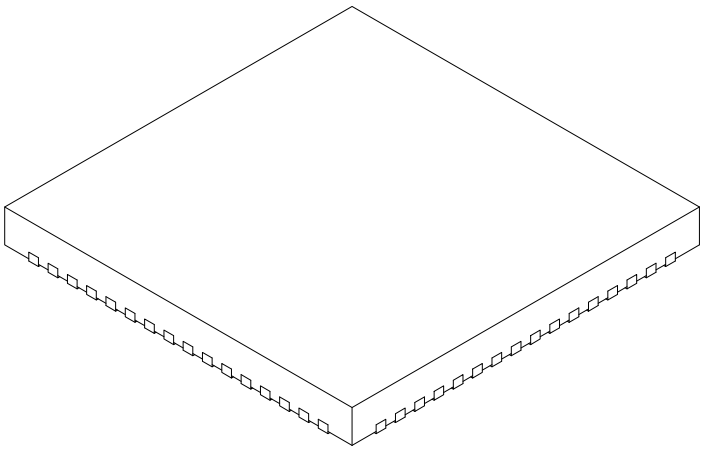
Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2