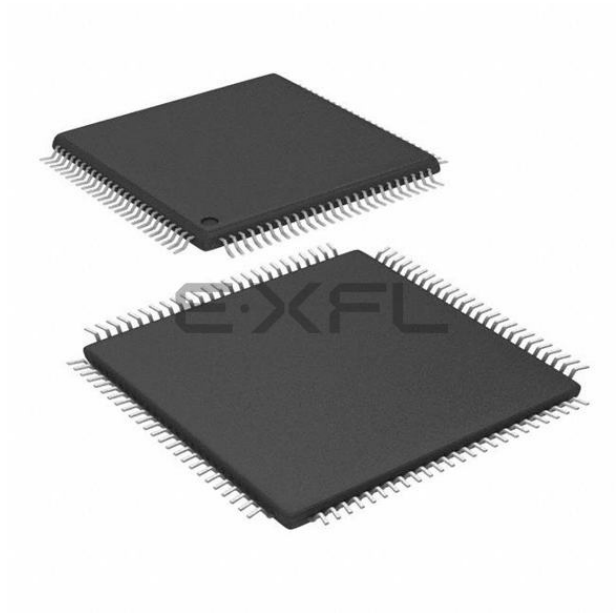
Microchip Technology - PIC32MK1024GPE100T-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	77
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024gpe100t-i-pt

TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MK0512GPD100
PIC32MK0512GPE100
PIC32MK1024GPD100
PIC32MK1024GPE100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/PMA23/RG15	36	VSS
2	VDD	37	VDD
3	TCK/RPA7/PMD5/RA7	38	AN35/RG11
4	RPB14/VBUSON1/PMD6/RB14	39	AN36/RF13
5	RPB15/PMD7/RB15	40	AN37/RF12
6	RD1	41(6)	AN12/C2IN2-/C5IN2-/PMA11/RE12
7	RD2	42(5)	AN13/C3IN2-/PMA10/RE13
8	RPD3/RD3	43	AN14/RPE14/PMA1/RE14
9	RPD4/RD4	44	AN15/RPE15/PMA0/RE15
10	AN19/RPG6/VBUSON2/PMA5/RG6	45	VSS
11	AN18/RPG7/1/PMA4/RG7(5)	46	VDD
12	AN17/RPG8//PMA3/RG8(6)	47	AN38/RD14
13	$\overline{\text{MCLR}}$	48	AN39/RD15
14	AN16/RPG9/PMA2/RG9	49	TDI/CDAC3/AN26/RPA8/PMA9/RA8(6)
15	VSS	50	RPB4/PMA8/RB4(5)
16	VDD	51	OA5IN+/CDAC1/AN24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
17	AN22/RG10	52	AN40/RPE0/RE0
18	AN21/RE8	53	AN41/RPE1/RE1
19	AN20/RE9	54	VBUS1
20	AN10/RPA12/RA12	55	VUSB3V3
21	AN9/RPA11/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGED3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGEC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/RF5
27	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/PMA7/RF9	63	OSC1/CLKI/AN49/RPC12/RC12
29	VREF+/AN34/PMA6/RF10	64	OSC2/CLKO/RPC15/RC15
30	AVDD	65	VSS
31	AVSS	66	AN46/RPA14/RA14
32	OA3OUT/AN6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/RPA15/RA15
33	OA3IN-/AN7/C3IN1-/C4IN1-/RPC1/RC1	68	VBAT(7)
34	OA3IN+/AN8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	69	PGED2/RPB5/USBID1/RB5(6)
35	AN11/C1IN2-/PMA12/RC11	70	PGEC2/RPB6/SCK2/PMA15/RB6(5)

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).
7: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

2.4 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS50001765
- *"MPLAB® ICD 3 Design Advisory"* DS50001764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) DS50001749

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.6 Trace

When present on select pin counts, the trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT

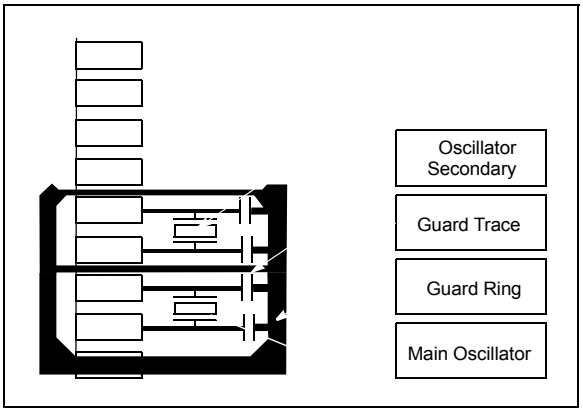
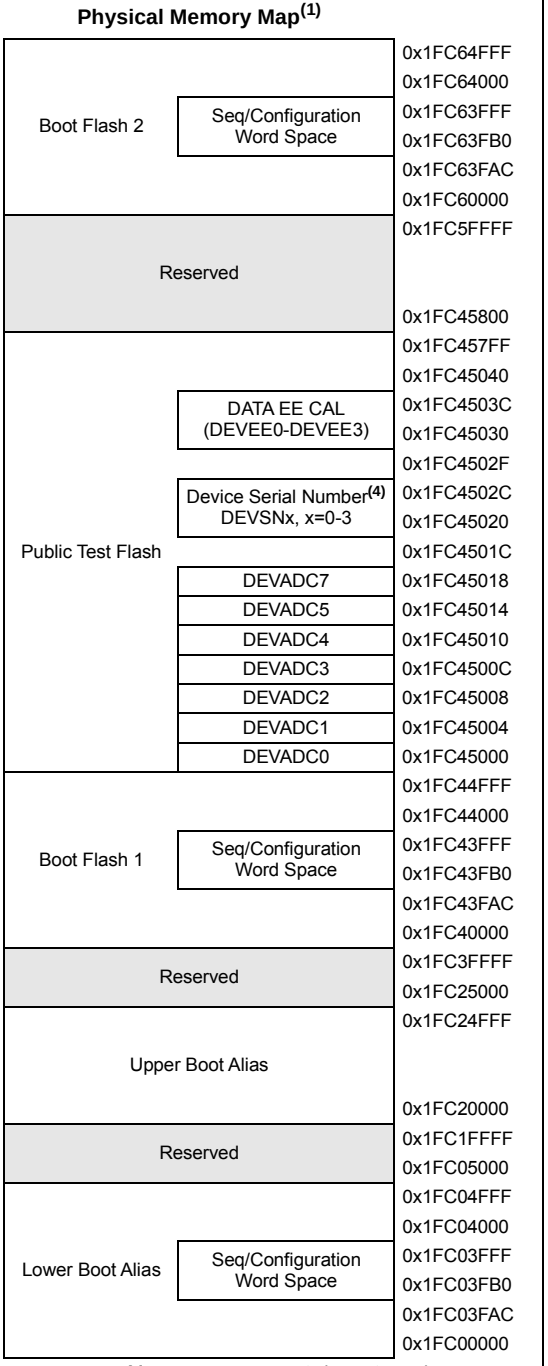


FIGURE 4-3: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.
2: Memory locations 0x1FC03FB0 through 0x1FC03FFC are used to initialize Configuration registers (see **33.0 "Special Features"**).
3: Refer to **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.
4: Memory locations 0x1FC5020 and 0x1FC502C contain a unique device serial number (see **33.0 "Special Features"**).
5: This configuration space cannot be used for executing code in the upper Boot Alias.

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
CFG-PMD	0xBF800000	0x0000
CACHE		0x0800
FC-NVM		0x0A00
WDT		0x0C00
DMT		0x0E00
ICD		0x1000
CRU		0x1200
PPS		0x1400
PLVD		0x1800
EVIC	0xBF810000	0x0000
DMA		0x1000
Timer1-Timer9	0xBF820000	0x0000
IC1-IC9		0x2000
OC1-OC9		0x4000
I2C1-I2C2		0x6000
SPI1-SPI2		0x7000
UART1-UART2		0x8000
DATAEE		0x9000
PWM1-PWM12		0xA000
QEI1-QEI6		0xB200
CMP		0xC000
CDAC1		0xC200
CTMU		0xD000
PMP		0xE000
IC10-IC16	0xBF840000	0x3200
OC10-OC16		0x5200
I2C3-I2C4		0x6400
SPI3-SPI6		0x7400
UART3-UART6		0x8400
CDAC2-CDAC3		0xC400
PORTA-PORTG	0xBF860000	0x0000
CAN1-CAN4	0xBF880000	0x0000
ADC		0x7000
USB1-USB2		0x9000
RTCC	0xBF8C0000	0x0000
Deep Sleep		0x0200
SSX CTL	0xBF8F0000	0x0000

Note 1: Refer to **4.2 "System Bus Arbitration"** for important legal information.

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-3; 'y' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **GROUP3:** Group 3 Read Permissions bits
- 1 = Privilege Group 3 has read permission
- 0 = Privilege Group 3 does not have read permission

bit 2 **GROUP2:** Group 2 Read Permissions bits
- 1 = Privilege Group 2 has read permission
- 0 = Privilege Group 2 does not have read permission

bit 1 **GROUP1:** Group 1 Read Permissions bits
- 1 = Privilege Group 1 has read permission
- 0 = Privilege Group 1 does not have read permission

bit 0 **GROUP0:** Group 0 Read Permissions bits
- 1 = Privilege Group 0 has read permission
- 0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.
2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

6.0 DATA EEPROM

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 58. "Data EEPROM"** (DS60001341), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Data EEPROM module provides the following features:

- 1K x 32-bit (4K x 8-bit) Emulated Data EEPROM using the 1K x 16 x 33-bit (66 KB)
- Register-based indirect access
- Register-based, non-memory mapped, SFR Program/Erase/Read interface
- Read:
  - Byte or Word read
  - Read start Control bit and read complete status flag
  - Read complete interrupt
- Program/Erase:
  - No user erase required prior to program
  - Hardware Word program verify
  - Automatic page erase as part of wear-leveling scheme
  - Hardware page erase verify
  - Bulk and page erase
  - Write complete and error interrupts
- Brown-out protection for all commands
- Concurrent Data EEPROM read with Program Flash read/write
- Endurance:
  - 160K program cycles per address location
  - Transparent wear-leveling scheme
  - No software overhead
  - Automatic page erase (once every 17 program write operations)
  - "Worn out" page detection and error flag
  - "Imminent Page Erase" prediction status flag to allow user to schedule wear leveling page erasure
- Low-power features:
  - Always in stand-by unless accessed
  - Power down in Sleep and/or Idle mode
  - Independent Data EEPROM Flash power down in Idle Control bit

6.1 Data EEPROM Flash

Table 6-1 provides the status of the Data EEPROM Flash.

TABLE 6-1: DATA EEPROM FLASH

Data EE Wait Status EEWS<7:0> bits (CFGCON2<7:0>) =	PBCLK (FSYSCLK / PBDIV<6:0> bits (PB2DIV<6:0>))
0	0-39 MHz
1	40-59 MHz
2	60-79 MHz
3	80-97 MHz
4	98-117 MHz
5	118-120 MHz

Note 1: The Data EEPROM Flash must have its calibration trim bits reinitialized after each cold power-up before any attempted accesses. Refer to **Section 58. "Data EEPROM"** (DS60001341) of the *"PIC32 Family Reference Manual"* for additional information.

2: Before any attempts to access the Data EEPROM module, the user application must configure the appropriate number of Wait states by configuring the EEWS<7:0> bits (CFGCON2< 7:0>) according to Table 6-1.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
08C8	OFF226	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08CC	OFF227	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08D0	OFF228	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08D4	OFF229	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08D8	OFF230	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0910	OFF244	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0914	OFF245	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0918	OFF246	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0938	OFF254	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

TABLE 9-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1350	PB6DIV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB7DIV(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1380	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
1390	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	UPLLRDY	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
2: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
3: The PB7DIV register is read-only.

REGISTER 9-4: UPLLCON: USB PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	UPOSCEN	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—					PLLIDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PLLRANGE<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **UPOSCEN:** Output Enable bit
1 = USB input clock is POSC
0 = USB input clock is UPLL

bit 28-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits
111 = Reserved
110 = Reserved
101 = PLL Divide by 32
100 = PLL Divide by 16
011 = PLL Divide by 8
010 = PLL Divide by 4
001 = PLL Divide by 2
000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 23 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the UPLL is selected as a clock source (COSC<2:0> = 001).

3: While the PLL is active, and if updating the PLL bits in the OSCCON register at run-time, the user application must remain within the following limits at all times for all nodes in the PLL clock tree. Therefore, the order in which the PLL values may be modified, (i.e., PLLODIV, PLLMULT, PLLODIV) becomes important. Failure to maintain PLL nodes within min/max ranges may result in unstable PLL and system behavior.

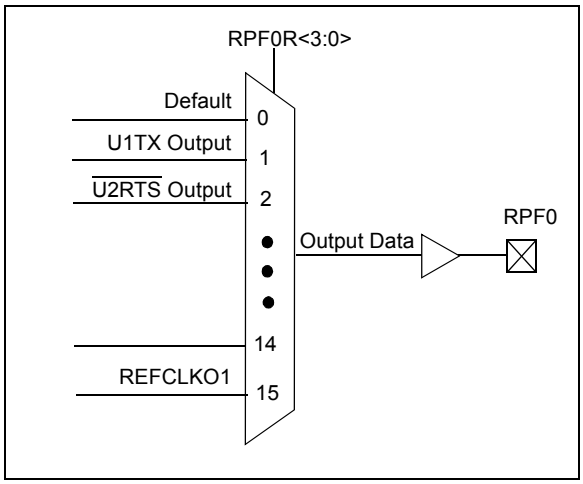
- Output and input to PLLIDIV block (i.e., FPLLI) 5 MHz to 64 MHz (min/max at all times)
- VCO output, (i.e., FVCO) 350 MHz to 700 MHz (min/max at all times)
- Output of PLLODIV, (i.e., FPLL) 10 MHz to 120 MHz (min/max at all times)

13.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 13-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 13-2 and Figure 13-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 13-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



13.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The PIC32MK GP/MC devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

13.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting the IOLOCK bit prevents writes to the control registers and clearing the IOLOCK bit allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

13.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If the IOLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

TABLE 13-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA1	RPA1R	RPA1R<4:0>	00000 = Off 00001 = U3RTS 00010 = U4TX 00011 = SDO1 00100 = SDO2 00101 = OC2 00110 = OC8 00111 = C3OUT 01000 = OC9 01001 = OC12 01010 = OC16 01011 = U6RTS 01100 = C4TX 01101 = Reserved 01110 = SDO3 01111 = SDO4 10000 = SDO5 10001 = SCK6 10010 = REFCLKO3 10011 = Reserved 10100 = QEICMP2 10101 = QEICMP6 10110 = Reserved . . . 11111 = Reserved
RPB5	RPB5R	RPB5R<4:0>	
RPB1	RPB1R	RPB1R<4:0>	
RPB11	RPB11R	RPB11R<4:0>	
RPA8	RPA8R	RPA8R<4:0>	
RPC8	RPC8R	RPC8R<4:0>	
RPB12	RPB12R	RPB12R<4:0>	
RPA12	RPA12R	RPA12R<4:0>	
RPD6	RPD6R	RPD6R<4:0>	
RPG7	RPG7R	RPG7R<4:0>	
RPG0(1)	RPG0R(1)	RPG0R<4:0> (1)	
RPE1(1)	RPE1R(1)	RPE1R<4:0> (1)	
RPA14(1)	RPA14R(1)	RPA14R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-5: PORTB REGISTER MAP FOR 64-PIN AND 100-PIN DEVICES

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSB9	—	ANSB7	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	008F
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEB15	CNNEB14	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB15	CNFB14	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB6	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	0000
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0B15	SR0B14	SR0B13	SR0B12	SR0B11	SR0B10	—	—	SR0B7	SR0B6	—	SR0B4	—	—	—	—	0000
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1B15	SR1B14	SR1B13	SR1B12	SR1B11	SR1B10	—	—	SR1B7	SR1B6	—	SR1B4	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1500	IC12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC12R<3:0>				0000
1504	IC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC13R<3:0>				0000
1508	IC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC14R<3:0>				0000
150C	IC15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC15R<3:0>				0000
1510	IC16R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC16R<3:0>				0000
1514	SCK5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK5R<3:0>				
1518	SDI5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
151C	SS5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
1520	SCK6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK6R<3:0>				
1524	SDI6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000
1528	SS6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
152C	C3RXR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C3RXR<3:0>				0000
1530	C4RXR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C4RXR<3:0>				0000
1534	QEA3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA3R<3:0>				0000
1538	QEB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

3: This register is only available on PIC32MKXXXGPEXXX devices.

REGISTER 18-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1-16)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit
1 = Module enabled
0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
1 = Halt in CPU Idle mode
0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
1 = Capture rising edge first
0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
1 = 32-bit timer resource capture
0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')(1)
0 = Timery is the counter source for capture
1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty; at least one more capture value can be read
0 = Input capture buffer is empty

Note 1: Refer to Table 18-1 for Timerx and Timery selections.

REGISTER 26-1: CxCON: CAN MODULE CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 26-9: CxRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER ('x' = 1-4; 'n' = 0, 1, 2 OR 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SID<10:3>							
23:16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SID<2:0>			—	MIDE	—	EID<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include the SIDx bit in filter comparison
0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include the EIDx bit in filter comparison
0 = The EIDx bit is a 'don't care' in filter operation

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

27.0 OP AMP/COMPARATOR MODULE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 39. "Op amp/Comparator"** (DS60001178), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

Depending on the device, the Op amp/Comparator module consists of a Comparator and Op amp modules. When available, the Op amps can be independently enabled or disabled from the Comparator.

Key features of the Comparator include:

- Differential inputs
- Rail-to-rail operation
- Selectable output and trigger event polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal voltage reference via a 12-bit CDAC output or an external pin
- Output debounce or Digital noise filter with these selectable clocks:
  - Peripheral Bus Clock (PBCLK2)
  - System Clock (SYSCLK)
  - Reference Clock 3 (REFCLK3)
  - PBCLK2/Timer PRx ('x' = 2-5)
  - PWM Secondary Special Event
- Outputs can be internally configured as trigger sources

The following are key features of the Op amps:

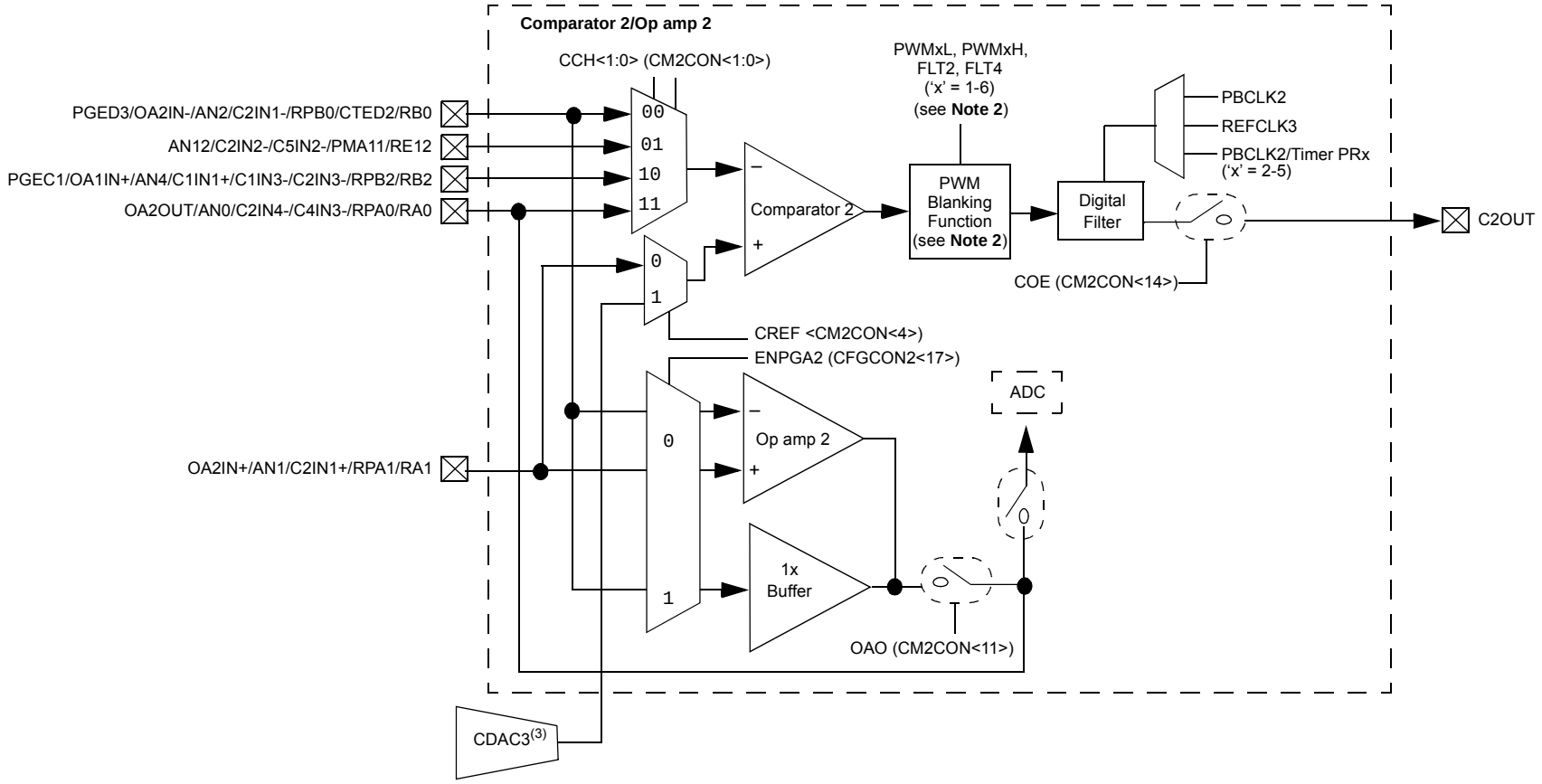
- Inverting and non-inverting Inputs and output accessible on pins
- Rail-to-rail operation ($3V \leq AV_{DD} \leq 3.6V$)
- Internal connection to ADC Sample and Hold circuits/SAR cores
- Special voltage follower mode for buffering signals

Please refer to the PIC32MK GP Family Features in **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the actual number of available Op amp/ Comparator modules on your specific device.

Block diagrams of the Op amp/Comparator module are illustrated in Figure 27-1 through Figure 27-5.

Note: The Op amps are disabled by default (i.e., OPAxMD bit in the PMD2 register is equal to '1') on any Reset. Before use or access to any corresponding Op amp, ensure that the OPAxMD bit is equal to '0'.

FIGURE 27-2: OP AMP 2/COMPARATOR 2 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is available only on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

REGISTER 29-1: DACxCON: CDAC CONTROL REGISTER 'x' ('x' = 1 THROUGH 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DACDAT<11:8>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DACDAT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON(1)	—	—	—	—	—	—	DACOE(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>(1,2)	

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-16 **DACDAT<11:0>:** CDAC Data Port bits(1)
Data input register bits for the CDAC.

bit 15 **ON:** CDAC Enable bit
1 = The CDAC is enabled
0 = The CDAC is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** CDAC Output Buffer Enable bit
1 = Output is enabled; CDAC voltage is connected to the pin
0 = Output is disabled; drive to pin is floating

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** Reference Source Select bits(1,2)
11 = Positive reference voltage = AVDD
10 = No reference selected (no reference current consumption)
01 = No reference selected (no reference current consumption)
00 = No reference selected (no reference current consumption)

Note 1: To minimize CDAC start-up output transients, configure the DACDATA<15:0>, DACOE, and REFSEL<1:0> bits prior to enabling the CDAC (prior to making DACON = 1). Also, remember to wait TON time, after enabling the CDAC. This time is required to allow the CDAC output to stabilize. Refer to **Section 36.0 "Electrical Characteristics"** for the TON specification.

2: If the ON bit is '0', the reference source is disconnected from the internal resistor network.

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 18 **FLTPOL:** Fault Polarity bits for PWM Generator 'x'(2)
1 = The selected fault source is active-low
0 = The selected fault source is active-high

bit 17-16 **FLTMOD<1:0>:** Fault Mode bits for PWM Generator 'x'(4)
11 = Fault input is disabled, no fault overrides possible. (fault interrupts can still be generated)
10 = Reserved
01 = Selected fault source forces PWMxH, PWMxL pins to FLTDAT<1:0> values (cycle by cycle)
00 = Selected fault source forces PWMxH, PWMxL pins to FLTDAT<1:0> values (Latched condition)
Changes take effect on the next PWM cycle boundary following PWM being enabled, and subsequently on each PWM cycle boundary. When updating FLTMOD<1:0> from '00' or '01' to '11' (disabled), if the fault input is still active the fault override condition will not be removed. If enabled, Faults will override the CLMOD bit setting.

bit 15 **PENH:** PWMxH Output Pin Ownership bit(1)
1 = PWM module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit(1)
1 = PWM module controls PWMxL pin
0 = GPIO module controls PWMxL pin

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

32.2.3 DEEP SLEEP MODE

Deep Sleep mode brings the device into its lowest power consumption state without requiring the use of external switches to remove power from the device.

- **Deep Sleep**
  In this mode, the CPU, RAM and most peripherals are powered down. Power is maintained to the DSGPR0 register and one or more of the RTCC, DSWDT and DSGPR1 through DSGPR32 registers.

Which of these peripherals is active depends on the state of the following register bits when Deep Sleep mode is entered:

- **RTCDIS (DSCON<12>)**
  This bit must be set to disable the RTCC in Deep Sleep mode (Register 32-1).
- **DSWDTEN (DEVCFG2<27>)**
  This Configuration bit must be set to enable the DSWDT register in Deep Sleep mode (Register 41-5)
- **DSGPREN (DSCON<13>)**
  This bit must be set to enable the DSGPR1 through DSGPR32 registers in Deep Sleep mode and will only maintain their value through deep sleep if enabled. (Register 32-1).

Note:	The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, the Deep Sleep Control registers and DSGPR1-32 must be written twice as part of a silicon anti-corruption check in case of a write during a power fail.

In addition to the conditionally enabled peripherals described above, $\overline{\text{MCLR}}$ and INT0 pin are enabled in Deep Sleep mode.

32.2.4 VBAT MODE

VBAT mode is similar to Deep Sleep mode, except that the device is powered from the V_{BAT} pin. VBAT mode is controlled strictly by hardware, without any software intervention. VBAT mode is initiated when V_{DD} falls below V_{POR} (refer to the **36.0 "Electrical Characteristics"** chapter for definitions of V_{DD} and V_{POR}). An external power source must be connected to the V_{BAT} pin before power is removed from V_{DD} to enter VBAT mode. VBAT is the lowest battery-powered mode that can maintain an RTCC. Wake-up from VBAT mode can only occur when V_{DD} is reapplied. The wake-up will appear to be a POR to the rest of the device.

In VBAT mode, the Deep Sleep Watchdog Timer is disabled. The RTCC and DSGPR1 through DSGPR32 registers may be enabled or disabled depending on the state of the RTCDIS bit (DSCON<12>) and the DSGPREN bit (DSCON<13>), respectively. Deep Sleep Persistent General Purpose Register 0 (DSGPR0) is always enabled in VBAT mode.

32.2.5 POWER-SAVING MODES

Figure 32-1 shows a block diagram and the related power-saving features. The various blocks are controlled by the following Configuration bit settings and SFRs:

- DSBOREN (DEVCFG2<20>)
- DSEN (DSCON<15>)
- DSGPREN (DSCON<13>)
- DSWDTEN (DEVCFG2<27>)
- DSWDTOSC (DEVCFG2<26>)
- RELEASE (DSCON<0>)
- RTCCLKSEL (RTCCON <9:8>)
- RTCDIS (DSCON<12>)
- SLPEN (OSCCON<4>)
- VREGS (PWRCON<0>)