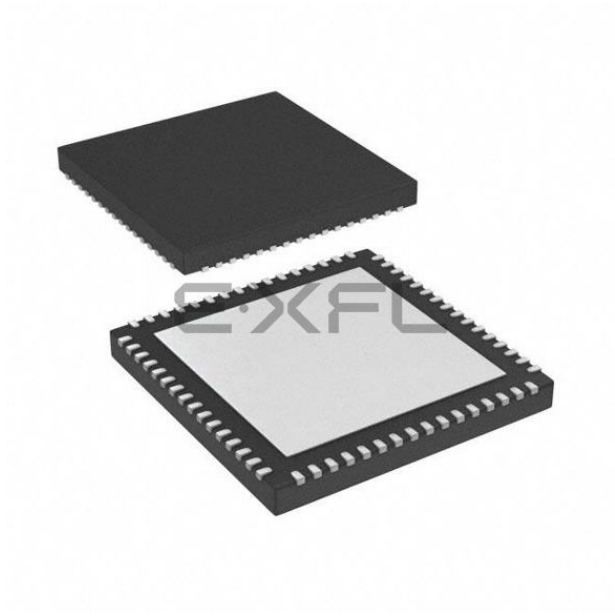

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Program Memory Type	FLASH
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Supplier Device Package	64-QFN (9x9)
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REGISTER 3-4: CONFIG4: CONFIGURATION REGISTER 4; CP0 REGISTER 16, SELECT 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	M	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	KScr Exist<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	—	—	—

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **M:** Config5 Register Present bit
1 = Config5 register is present
0 = Config5 register is not present

bit 30-24 **Unimplemented:** Read as '0'

bit 23-16 **KScr Exist<7:0>:** Number of Scratch Registers Available to Kernel Mode bits
Indicates how many scratch registers are available to Kernel mode software within CP0 Register 31. Each bit represents a select for Coprocessor0 Register 31. Bit 16 represents Select 0. Bit 23 represents Select 7. If the bit is set, the associated scratch register is implemented and is available for Kernel mode software.

Note: These bits are read-only, and this field is all zeros on these products, as is read as '0'.

bit 15-0 **Reserved:** Read/write as '0'

NOTES:

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6.0 DATA EEPROM

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 58. "Data EEPROM"** (DS60001341), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Data EEPROM module provides the following features:

- 1K x 32-bit (4K x 8-bit) Emulated Data EEPROM using the 1K x 16 x 33-bit (66 KB)
- Register-based indirect access
- Register-based, non-memory mapped, SFR Program/Erase/Read interface
- Read:
  - Byte or Word read
  - Read start Control bit and read complete status flag
  - Read complete interrupt
- Program/Erase:
  - No user erase required prior to program
  - Hardware Word program verify
  - Automatic page erase as part of wear-leveling scheme
  - Hardware page erase verify
  - Bulk and page erase
  - Write complete and error interrupts
- Brown-out protection for all commands
- Concurrent Data EEPROM read with Program Flash read/write
- Endurance:
  - 160K program cycles per address location
  - Transparent wear-leveling scheme
  - No software overhead
  - Automatic page erase (once every 17 program write operations)
  - "Worn out" page detection and error flag
  - "Imminent Page Erase" prediction status flag to allow user to schedule wear leveling page erasure
- Low-power features:
  - Always in stand-by unless accessed
  - Power down in Sleep and/or Idle mode
  - Independent Data EEPROM Flash power down in Idle Control bit

6.1 Data EEPROM Flash

Table 6-1 provides the status of the Data EEPROM Flash.

TABLE 6-1: DATA EEPROM FLASH

Data EE Wait Status EEWS<7:0> bits (CFGCON2<7:0>) =	PBCLK (FSYSCLK / PBDIV<6:0> bits (PB2DIV<6:0>))
0	0-39 MHz
1	40-59 MHz
2	60-79 MHz
3	80-97 MHz
4	98-117 MHz
5	118-120 MHz

Note 1: The Data EEPROM Flash must have its calibration trim bits reinitialized after each cold power-up before any attempted accesses. Refer to **Section 58. "Data EEPROM"** (DS60001341) of the *"PIC32 Family Reference Manual"* for additional information.

2: Before any attempts to access the Data EEPROM module, the user application must configure the appropriate number of Wait states by configuring the EEWS<7:0> bits (CFGCON2< 7:0>) according to Table 6-1.

TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0370	IPC35	31:16	—	—	—	AD1D37IP<2:0>			AD1D37IS<1:0>		—	—	—	AD1D36IP<2:0>			AD1D36IS<1:0>		0000
		15:0	—	—	—	AD1D35IP<2:0>			AD1D35IS<1:0>		—	—	—	AD1D34IP<2:0>			AD1D34IS<1:0>		0000
0380	IPC36	31:16	—	—	—	AD1D41IP<2:0>			AD1D41IS<1:0>		—	—	—	AD1D40IP<2:0>			AD1D40IS<1:0>		0000
		15:0	—	—	—	AD1D39IP<2:0>			AD1D39IS<1:0>		—	—	—	AD1D38IP<2:0>			AD1D38IS<1:0>		0000
0390	IPC37	31:16	—	—	—	AD1D45IP<2:0>			AD1D45IS<1:0>		—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
03A0	IPC38	31:16	—	—	—	AD1D49IP<2:0>			AD1D49IS<1:0>		—	—	—	AD1D48IP<2:0>			AD1D48IS<1:0>		0000
		15:0	—	—	—	AD1D47IP<2:0>			AD1D47IS<1:0>		—	—	—	AD1D46IP<2:0>			AD1D46IS<1:0>		0000
03B0	IPC39	31:16	—	—	—	AD1D53IP<2:0>			AD1D53IS<1:0>		—	—	—	AD1D52IP<2:0>			AD1D52IS<1:0>		0000
		15:0	—	—	—	AD1D51IP<2:0>			AD1D51IS<1:0>		—	—	—	AD1D50IP<2:0>			AD1D50IS<1:0>		0000
03C0	IPC40	31:16	—	—	—	—	—	—	—	—	—	—	—	CMP5IP<2:0>			CMP5IS<1:0>		0000
		15:0	—	—	—	CMP4IP<2:0>			CMP4IS<1:0>		—	—	—	CMP3IP<2:0>			CMP3IS<1:0>		0000
03D0	IPC41	31:16	—	—	—	CAN1IP<2:0>(3)			CAN1IS<1:0>(3)		—	—	—	U6TXIP<2:0>			U6TXIS<1:0>		0000
		15:0	—	—	—	U6RXIP<2:0>			U6RXIS<1:0>		—	—	—	U6EIP<2:0>			U6EIS<1:0>		0000
03E0	IPC42	31:16	—	—	—	PWMPEVTIP<2:0>			PWMSEVTIP<1:0>		—	—	—	QEI2IP<2:0>			QEI2SIP<1:0>		0000
		15:0	—	—	—	QEI1IP<2:0>			QEI1SIP<1:0>		—	—	—	CAN2IP<2:0>(3)			CAN2IS<1:0>(3)		0000
03F0	IPC43	31:16	—	—	—	PWM3IP<2:0>			PWM3SIP<1:0>		—	—	—	PWM2IP<2:0>			PWM2SIP<1:0>		0000
		15:0	—	—	—	PWM1IP<2:0>			PWM1SIP<1:0>		—	—	—	PWMSEVTIP<2:0>			PWMSEVTSIP<1:0>		0000
0400	IPC44	31:16	—	—	—	—	—	—	—	—	—	—	—	PWM6IP<2:0>			PWM6SIP<1:0>		0000
		15:0	—	—	—	PWM5IP<2:0>			PWM5SIP<1:0>		—	—	—	PWM4IP<2:0>			PWM4SIP<1:0>		0000
0410	IPC45	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>		—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0420	IPC46	31:16	—	—	—	CAN3IP<2:0>(3)			CAN3IS<1:0>(3)		—	—	—	DATAEEIP<2:0>			DATAEEIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>		—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0430	IPC47	31:16	—	—	—	QEI5IP<2:0>			QEI5SIP<1:0>		—	—	—	QEI4IP<2:0>			QEI4SIP<1:0>		0000
		15:0	—	—	—	QEI3IP<2:0>			QEI3SIP<1:0>		—	—	—	CAN4IP<2:0>(3)			CAN4IS<1:0>(3)		0000
0440	IPC48	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	QEI6IP<2:0>			QEI6SIP<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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10.2 Prefetch Control Registers

TABLE 10-1: PREFETCH REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	CHECON	31:16	—	—	—	—	—	PERCHEEN	DCHEEN	ICHEEN	—	PERCHEINV	DCHEINV	ICHEINV	—	PERCHECOH	DCHECOH	ICHECOH	0700
		15:0	—	—	—	CHEPERFEN	—	—	—	PFMAWSEN	—	—	PREFEN<1:0>		—	PFMWS<2:0>			0107
0820	CHEHIT	31:16	CHEHIT<31:16>																0000
		15:0	CHEHIT<15:0>																0000
0830	CHEMIS	31:16	CHEMIS<31:16>																0000
		15:0	CHEMIS<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 11-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPIGN<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
	CHBUSY	—	CHIPGNEN	—	CHPATLEN	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a "don't care" when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a "don't care" when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as '0'

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 12-7: UxIE: USB INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) / DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
- 1 = STALL interrupt is enabled
- 0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit
- 1 = ATTACH interrupt is enabled
- 0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
- 1 = RESUME interrupt is enabled
- 0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt is enabled
- 0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt is enabled
- 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt is enabled
- 0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB Error interrupt is enabled
- 0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt is enabled
- 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (UxIE<1>) must be set.
2: Device mode.
3: Host mode.

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TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1500	IC12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC12R<3:0>				0000
1504	IC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC13R<3:0>				0000
1508	IC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC14R<3:0>				0000
150C	IC15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC15R<3:0>				0000
1510	IC16R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC16R<3:0>				0000
1514	SCK5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK5R<3:0>				
1518	SDI5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
151C	SS5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
1520	SCK6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK6R<3:0>				
1524	SDI6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000
1528	SS6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
152C	C3RXR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C3RXR<3:0>				0000
1530	C4RXR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C4RXR<3:0>				0000
1534	QEA3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA3R<3:0>				0000
1538	QEB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

3: This register is only available on PIC32MKXXXGPEXXX devices.

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20.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

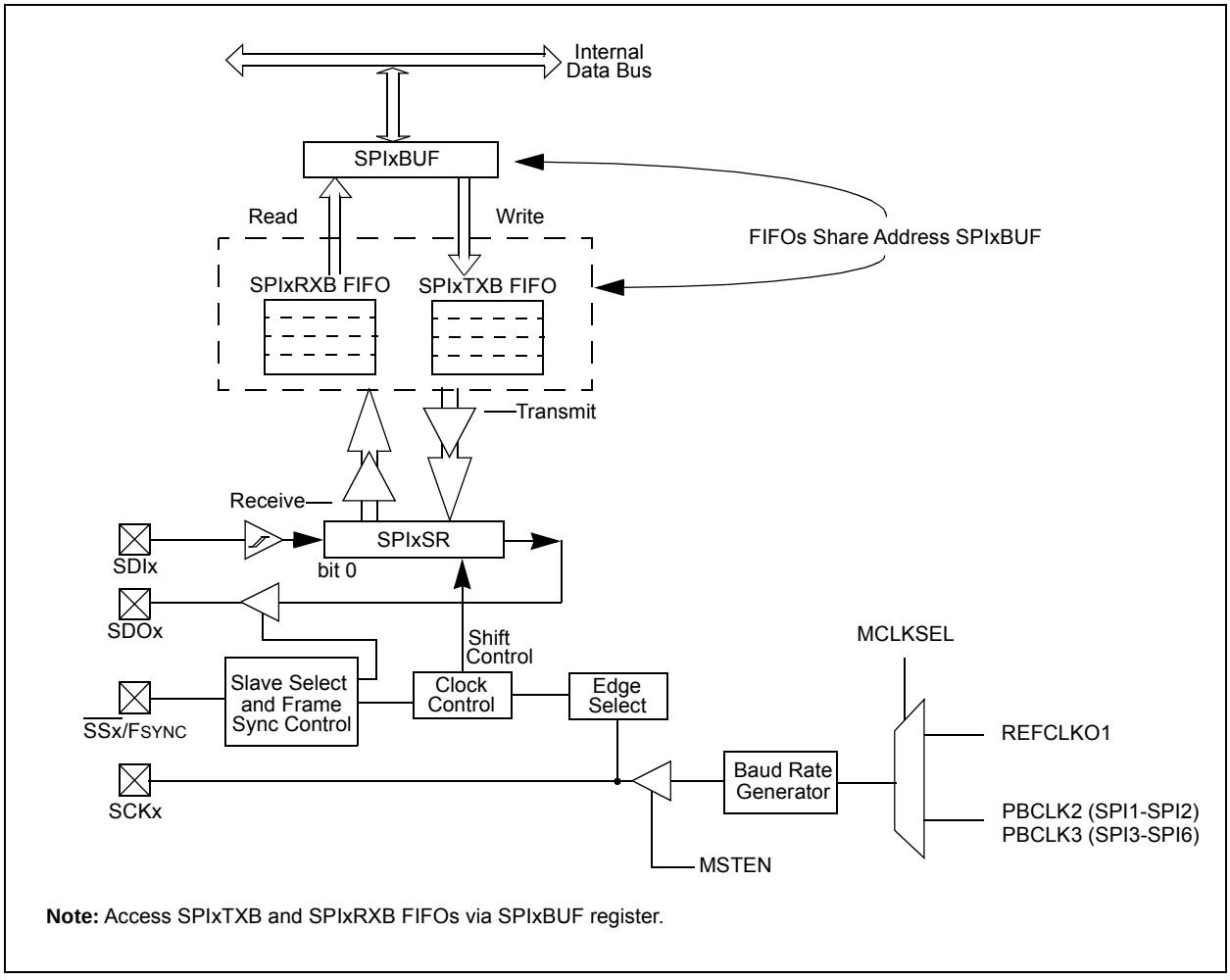
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, analog-to-digital converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 32/24/16/8-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/24/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio codec support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 20-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

REGISTER 20-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0, HS, HC	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0, HS, HC	R/C-0, HS	R-1, HS, HC	U-0	R-1, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	HC = Cleared in hardware	HS = Set in hardware	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

REGISTER 25-8: ADCIMCON4: ADC INPUT MODE CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DIFF49	SIGN49	DIFF48	SIGN48

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **DIFF49:** AN49 Mode bit
1 = Selects AN49 differential input pair as AN49+ and AN1-
0 = AN49 is using Single-ended mode

bit 2 **SIGN49:** AN41 Signed Data Mode bit
1 = AN49 is using Signed Data mode
0 = AN49 is using Unsigned Data mode

bit 1 **DIFF48:** AN48 Mode bit
1 = Selects AN40 differential input pair as AN48+ and AN1-
0 = AN48 is using Single-ended mode

bit 0 **SIGN48:** AN48 Signed Data Mode bit
1 = AN48 is using Signed Data mode
0 = AN48 is using Unsigned Data mode

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REGISTER 25-12: ADCCSS2: ADC COMMON SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	CSS53(2)	CSS52(2)	—	CSS50(2)	CSS49	CSS48
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	CSS47(1)	CSS46(1)	CSS45(1)	—	—	—	CSS41(1)	CSS40(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	CSS39(1)	CSS38(1)	CSS37(1)	CSS36(1)	CSS35(1)	CSS34(1)	CSS33(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-20 **CSS53:CSS52:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

bit 19 **Unimplemented:** Read as '0'

bit 21-20 **CSS50:CSS45:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

bit 9-1 **CSS41:CSS33:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.
2: CSS50-CSS53 are internal analog inputs with respect to (IVREF, IVREF Temp, VBAT/2, and CTMU Temp).

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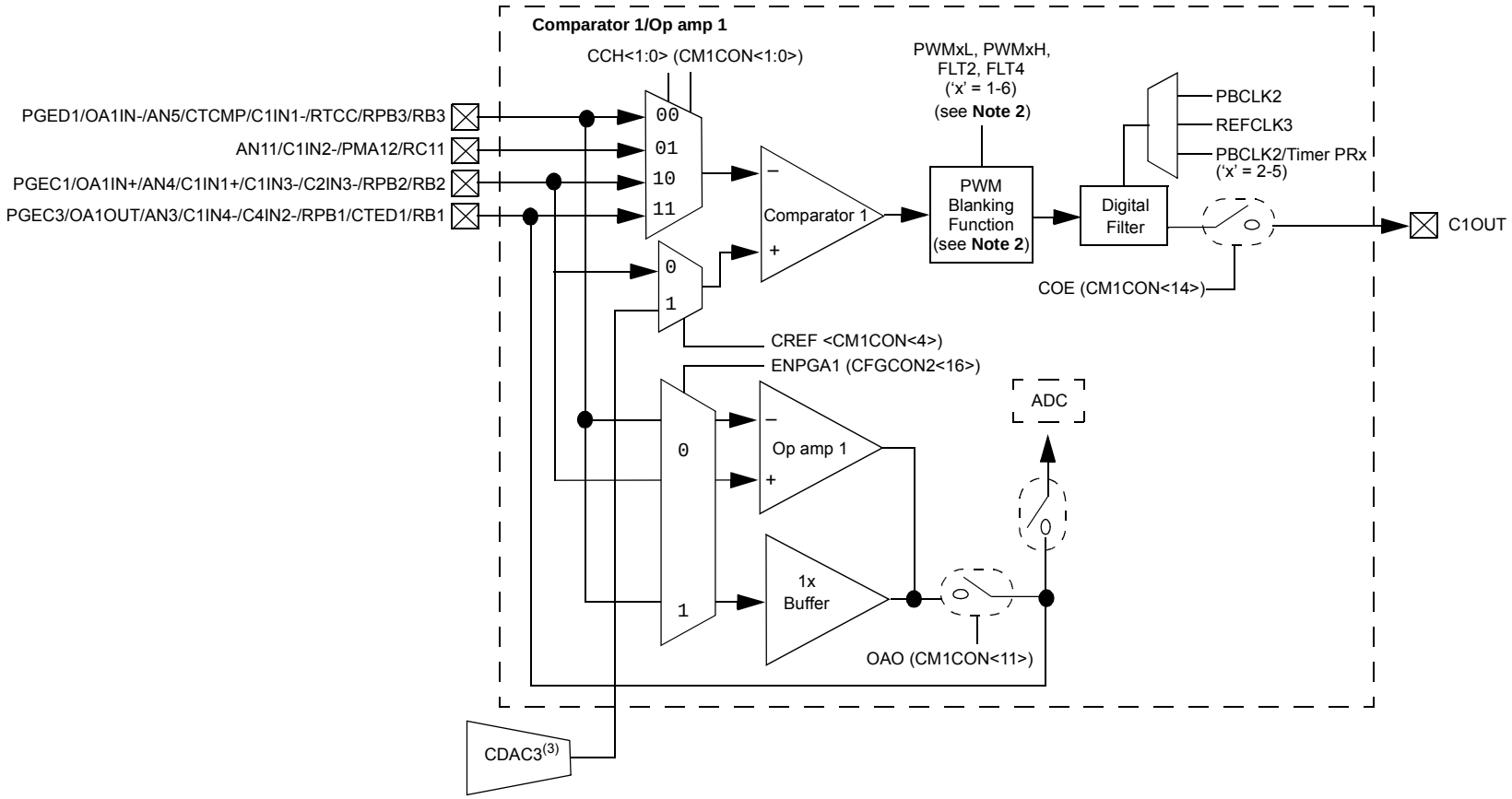
FIGURE 27-1: OP AMP 1/COMPARATOR 1 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is available only on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

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27.8 Op amp/Comparator Control Registers

TABLE 27-2: OP AMP/COMPARATOR REGISTER MAP

Virtual Address (BF82)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT	0000
C010	CM1CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C020	CM1MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C030	CM2CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C040	CM2MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C050	CM3CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C060	CM3MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C070	CM4CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C080	CM4MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C090	CM5CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C0A0	CM5MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register is only available on PIC32MKXXMCXX devices.

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REGISTER 30-5: VELxCNT: VELOCITY COUNTER REGISTER

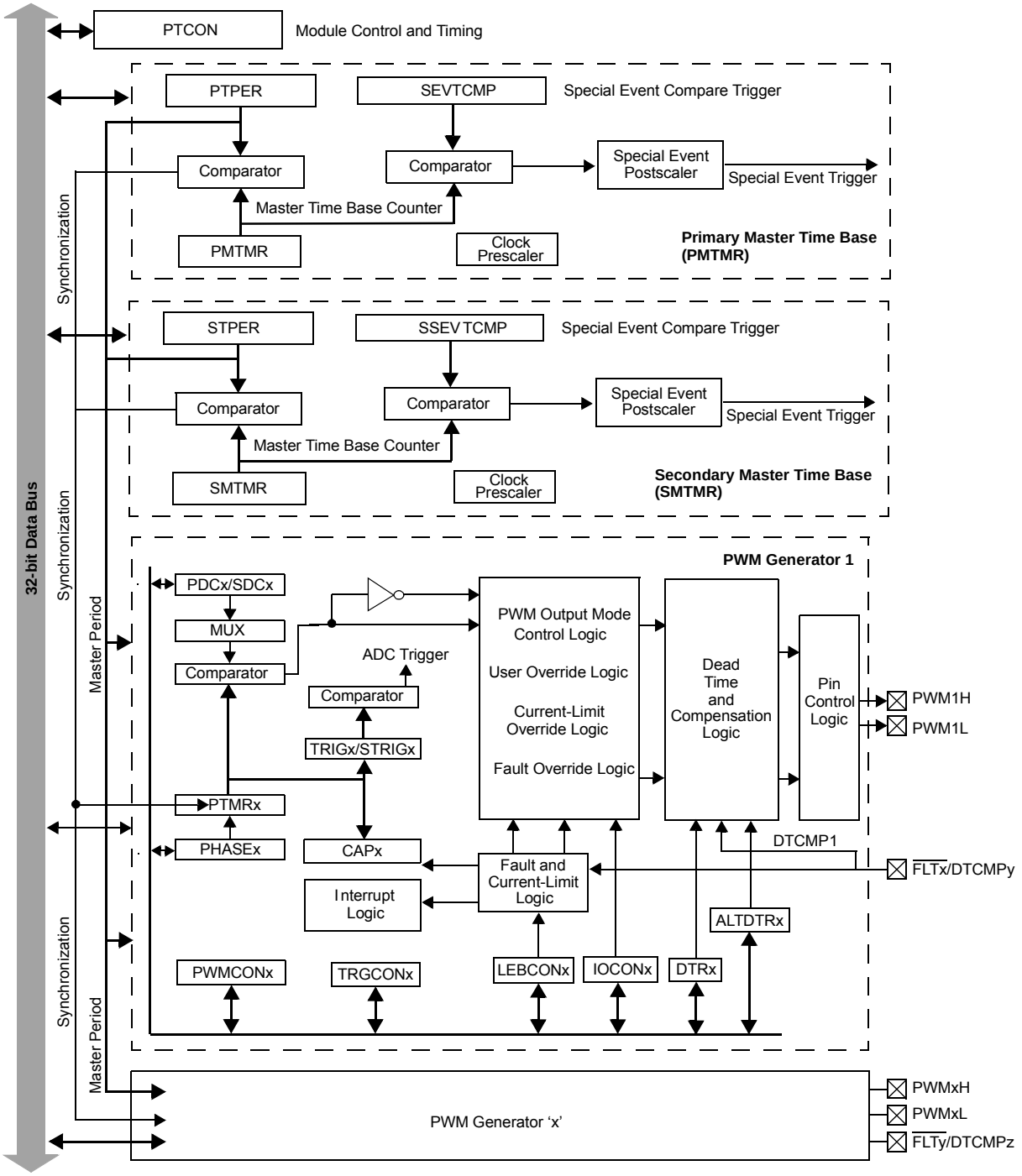
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **VELCNT<31:0>:** 32-bit Velocity Counter bits

The velocity counter is automatically cleared after every processor read of the velocity counter. It is not reset by the index input or otherwise affected by any of the PIMOD<2:0> specified modes. The contents of the counter represents the distance traveled during the time between samples. Velocity equals the distance traveled per unit of time. The velocity counter can save the application software the trouble of performing 32-bit math operations between current and previous position counter values to calculate velocity. If the velocity counter rolls over from 0x7FFFFFFF to 0x80000000, or from 0x80000000 to 0x7FFFFFFF, an overflow/underflow condition is detected. If the VELOVIEN bit is set in the QEISTAT register, an interrupt will be generated.

FIGURE 31-2: MOTOR CONTROL PWM MODULE REGISTER INTERCONNECTION DIAGRAM



Legend:

'x' = 1 through 12.
'y' = 1 through 8 and 15.
'z' = 3 through 8.

Note: Since DTCMPx and $\overline{\text{FLTx}}$ share the same digital input pins, their availability is mutually exclusive.

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REGISTER 33-5: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	r-1	R/P	R/P	R/P	R/P	R/P	R/P
	UPLLEN	—	BORSEL	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:3>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	DSWDTPS<2:0>			DSBOREN	VBAT-BOREN	FPLLODIV<2:0>		
15:8	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	FPLLMULT<6:0>						
7:0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **UPLLEN:** USB PLL Enable bit
1 = USB PLL is disabled
0 = USB PLL is enabled

bit 30 **Reserved:** Write as '1'

bit 29 **BORSEL:** Brown-out Reset Select Trip Voltage bit
1 = BOR trip voltage 2.1V (non-Op amp device operation)
0 = BOR trip voltage 2.8V (Op amp device operation)

Note: The user application should select the greatest BORSEL voltage to enable the highest trip voltage possible that is still less than VDD application operating voltage.

bit 28 **FDSEN:** Deep Sleep Bit Enable bit
1 = DS bit (DSCON<15>) is enabled on a WAIT command
0 = DS bit (DSCON<15>) is disabled

bit 27 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
1 = Enable DSWDT during Deep Sleep
0 = Disable DSWDT during Deep Sleep

bit 26 **DSWDTOSC:** Deep Sleep Watchdog Timer Reference Clock Select bit
1 = Select LPRC as DSWDT reference clock
0 = Select SOSC as DSWDT reference clock

TABLE 36-40: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

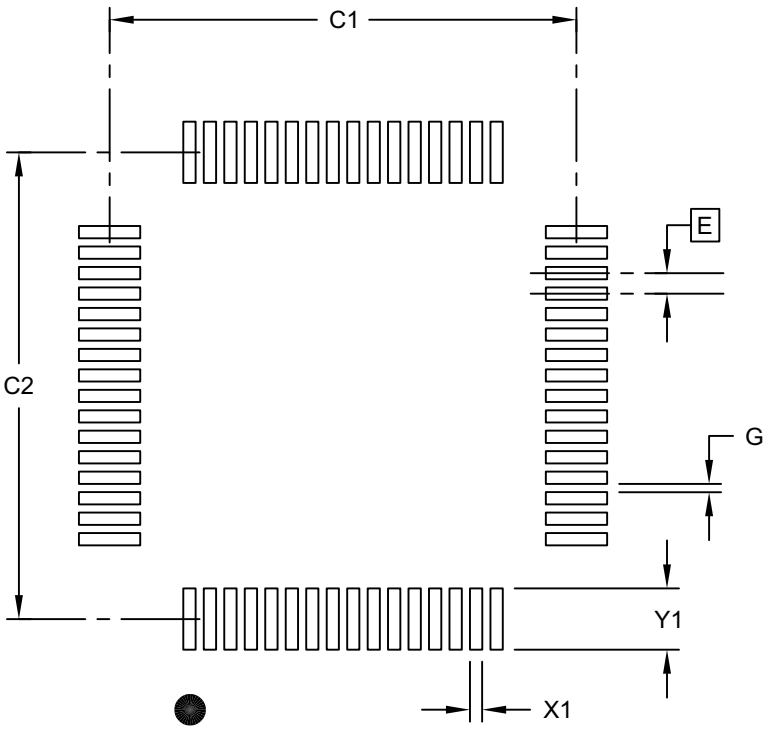
AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	16.667	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC5 (Class 1 Inputs)	— — — —	— — — —	3.75 4.284 4.992 6	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	3.53 4.00 4.615 5.45	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC5 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	See Table 36-41	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD µs	Lesser of 500 TAD or 20 µs

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

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