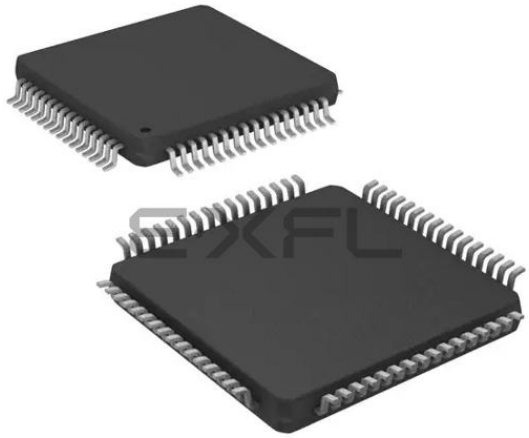
Microchip Technology - PIC32MK1024MCF064-E/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 27x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024mcf064-e-pt

TABLE 4: PIN NAMES FOR 64-PIN MOTOR CONTROL (MCF) DEVICES

64-PIN QFN(4) AND TQFP (TOP VIEW)

PIC32MK0512MCF064
PIC32MK1024MCF064

64 1 **QFN(4)** 64 1 **TQFP**

Pin #	Full Pin Name	Pin #	Full Pin Name
1	TCK/RPA7/PWM10H/PWM4L/PMPD5/RA7	33	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/T1G/RA4
2	RPB14/PWM1H/VBUSON1/PMPD6/RB14	34	VBUS
3	RPB15/PWM7H/PWM1L/PMPD7/RB15	35	VUSB3V3
4	AN19/CVD19/RPG6/PMPA5/RG6	36	D-
5	AN18/CVD18/RPG7/PMPA4/RG7(6)	37	D+
6	AN17/CVD17/RPG8/PMPA3/RG8(7)	38	VDD
7	MCLR	39	OSCI/CLKI/AN49/CVD49/RPC12/RC12
8	AN16/CVD16/RPG9/PMPA2/RG9	40	OSCO/CLKO/RPC15/RC15
9	VSS	41	VSS
10	VDD	42	RD8
11	AN10/CVD10/RPA12/RA12	43	PGED2/RPB5/USBID1/RB5(7)
12	AN9/CVD9/RPA11/USBOEN1/RA11	44	PGEC2/RPB6/SCK2/PMPA15/RB6(6)
13	OA2OUT/ANO/C2IN4-/C4IN3-/RPA0/RA0	45	DAC2/AN48/CVD48/RPC10/PMPA14/PSPCS/RC10
14	OA2IN+/AN1/C2IN1+/RPA1/RA1	46	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7
15	PGED3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	47	SOSCI/RPC13(5)/RC13(5)
16	PGEC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/RPB1/CTED1/PMPA6/RB1	48	SOSCO/RPB8(5)/RB8(5)
17	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	49	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9
18	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	50	TRCLK/RPC6/PWM6H/RC6
19	AVDD	51	TRD0/RPC7/PWM12H/PWM6L/RC7
20	AVSS	52	TRD1/RPC8/PWM5H/PMPWR/PSPWR/RC8
21	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	53	TRD2/RPD5/PWM12H/PMPRD/PSPRD/RD5
22	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/PMPA7/RC1	54	TRD3/RPD6/PWM12L/RD6
23	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMPA13/RC2	55	RPC9/PWM11H/PWM5L/RC9
24	AN11/CVD11/C1IN2-/FLT4/PMPA12/RC11	56	VSS
25	VSS	57	VDD
26	VDD	58	RPF0/PWM11H/RF0
27	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMPA11/RE12(7)	59	RPF1/PWM11L/RF1
28	AN13/CVD13/C3IN2-/FLT6/PMPA10/RE13(6)	60	RPB10/PWM3H/PMPD0/RB10
29	AN14/CVD14/RPE14/FLT7/PMPA1/PSPA1/RE14	61	RPB11/PWM9H/PWM3L/PMPD1/RB11
30	AN15/CVD15/RPE15/FLT8/PMPA0/PSPA0/RE15	62	RPB12/PWM2H/PMPD2/RB12
31	TDI/DAC3/AN26/CVD26/RPA8/PMPA9/RA8(7)	63	RPB13/PWM8H/PWM2L/CTPLS/PMPD3/RB13
32	FLT15/RPB4/PMPA8/RB4(6)	64	TDO/PWM4H/PMPD4/RA10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
5: Functions are restricted to input functions only and inputs will be slower than standard inputs.
6: The I^2C Library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
7: The I^2C Library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

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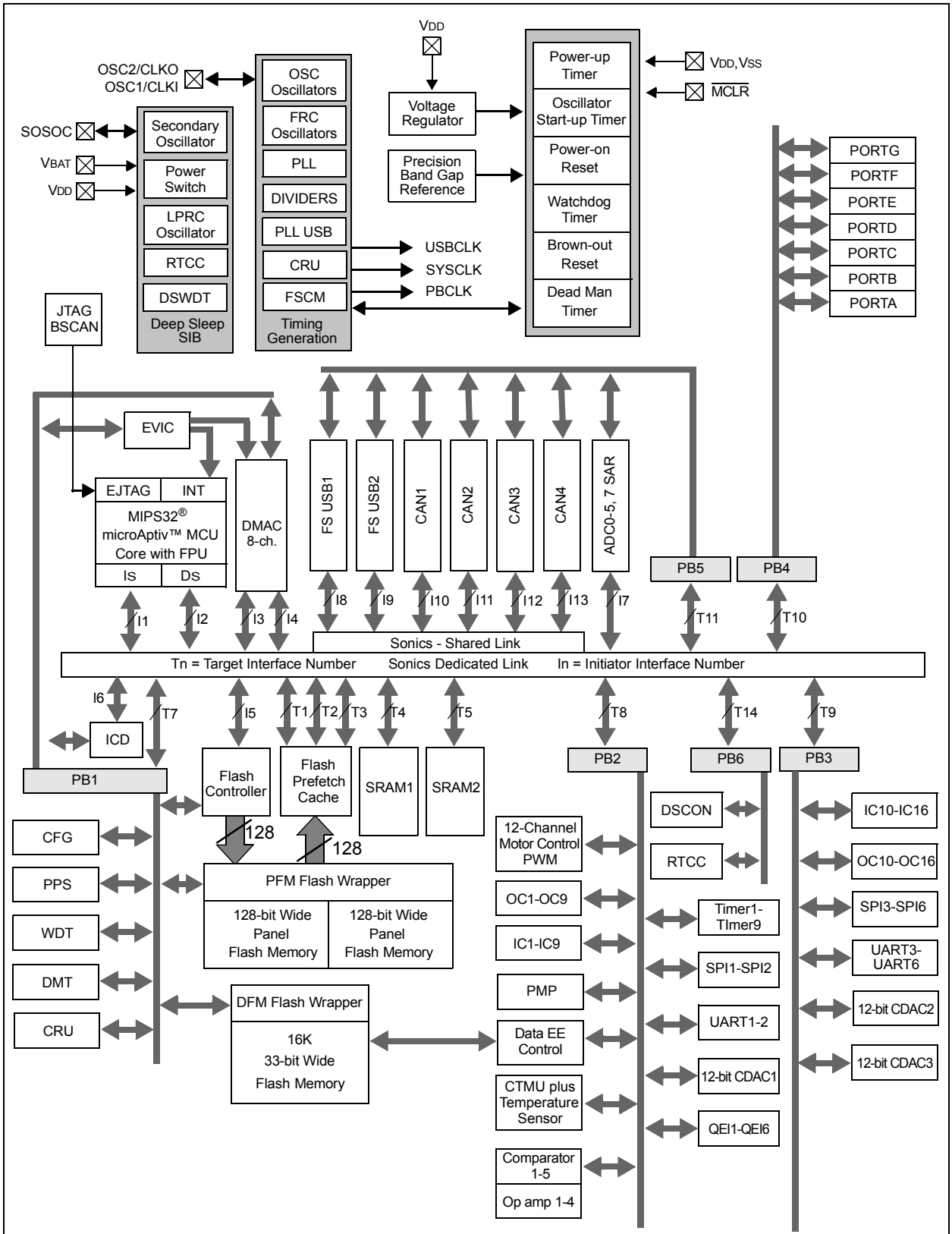
FIGURE 1-1: PIC32MK GP/MC FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to the family feature tables (Table 1 and Table 2) for the list of available features by device.

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TABLE 1-20: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Power and Ground					
AVDD	30	19	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	31	20	P	P	Ground reference for analog modules. This pin must be connected at all times.
VDD	2, 16, 37, 46, 62, 86	10, 26, 38, 57	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VSS	15, 36, 45, 65, 75, 85	9, 25, 41, 56	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
VBAT(1)	68	42	P	P	Battery backup for selected peripherals; otherwise connect to VDD.
Voltage Reference					
VREF+	29	16	I	Analog	Analog Voltage Reference (High) Input
VREF-	28	15	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

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5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				0000
0A10	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
0A20	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
0A30	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
0A40	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
0A50	NVMDATA2	31:16	NVMDATA2<31:0>																0000
		15:0																	0000
0A60	NVMDATA3	31:16	NVMDATA3<31:0>																0000
		15:0																	0000
0A70	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
0A80	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
0A90	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LBWPULOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPULOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF
0AA0	NVMCON2(1)	31:16	ERSCNT<3:0>				—	—	—	—	—	—	—	LPRDWS<4:0>					001F
		15:0	LPRD	—	CREAD1	VREAD1	—	—	ERETRY<1:0>		SWAPLOCK<1:0>		—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
01B0	IPC7	31:16	—	—	—	FCEIP<2:0>			FCEIS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
01C0	IPC8	31:16	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	USB1IP<2:0>			USB1IS<1:0>		0000
		15:0	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
01D0	IPC9	31:16	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
		15:0	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
01E0	IPC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
01F0	IPC11	31:16	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
0200	IPC12	31:16	—	—	—	PMPIP<2:0>			PMPIS<1:0>		—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
		15:0	—	—	—	CNFIP<2:0>			CNFIS<1:0>		—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
0210	IPC13	31:16	—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		0000
		15:0	—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		0000
0220	IPC14	31:16	—	—	—	—	—	—	—	—	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		0000
		15:0	—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
0230	IPC15	31:16	—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		—	—	—	U3EIP<2:0>			U3EIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0240	IPC16	31:16	—	—	—	U4TXIP<2:0>			U4TXIS<1:0>		—	—	—	U4RXIP<2:0>			U4RXIS<1:0>		0000
		15:0	—	—	—	U4EIP<2:0>			U4EIS<1:0>		—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		0000
0250	IPC17	31:16	—	—	—	CTMUIP<2:0>			CTMUIS<1:0>		—	—	—	U5TXIP<2:0>			U5TXIS<1:0>		0000
		15:0	—	—	—	U5RXIP<2:0>			U5RXIS<1:0>		—	—	—	U5EIP<2:0>			U5EIS<1:0>		0000
0260	IPC18	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
0270	IPC19	31:16	—	—	—	OC6IP<2:0>			OC6IS<1:0>		—	—	—	IC6IP<2:0>			IC6IS<1:0>		0000
		15:0	—	—	—	IC6EIP<2:0>			IC6EIS<1:0>		—	—	—	T6IP<2:0>			T6IS<1:0>		0000
0280	IPC20	31:16	—	—	—	OC7IP<2:0>			OC7IS<1:0>		—	—	—	IC7IP<2:0>			IC7IS<1:0>		0000
		15:0	—	—	—	IC7EIP<2:0>			IC7EIS<1:0>		—	—	—	T7IP<2:0>			T7IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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9.2 Oscillator Control Registers

TABLE 9-2: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1200	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			DRMEN	—	SLP2SPD	—	—	—	—	—	0xx0
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	UFRCEN	SOSCEN	OSWEN	xxxx
1210	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0020
1220	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							0xxx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			PLLICLK	—	—	—	—	PLLRANGE<2:0>			0xxx
1230	UPLLCON	31:16	—	—	UPOSCEN	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							0xxx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			—	—	—	—	—	PLLRANGE<2:0>			0x0x
1280	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
1290	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12A0	REFO2CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12B0	REFO2TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12C0	REFO3CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12D0	REFO3TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12E0	REFO4CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12F0	REFO4TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1300	PB1DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1310	PB2DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1320	PB3DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1330	PB4DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
2: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
3: The PB7DIV register is read-only.

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TABLE 13-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT4	INT4R<3:0>	INT4R	0000 = RPA0
T2CK	T2CKR<3:0>	T2CKR	0001 = RPB3
T6CK	T6CKR<3:0>	T6CKR	
IC4	IC4R<3:0>	IC4R	0010 = RPB4
IC7	IC7R<3:0>	IC7R	0011 = RPB15
IC12	IC12R<3:0>	IC12R	
IC15	IC15R<3:0>	IC15R	0100 = RPB7
U3RX	U3RXR<3:0>	U3RXR	0101 = RPC7
$\overline{\text{U4CTS}}$	U4CTSR<3:0>	U4CTSR	
U6RX	U6RXR<3:0>	U6RXR	0110 = RPC0
SDI1	SDI1R<3:0>	SDI1R	0111 = Reserved
SDI3	SDI3R<3:0>	SDI3R	
SCK4	SCK4R<3:0>	SCK4R	1000 = RPA11
SDI5	SDI5R<3:0>	SDI5R	1001 = RPD5
$\overline{\text{SS6}}$	SS6R<3:0>	SS6R	
QEA1	QEA1R<3:0>	QEA1R	1010 = RPG6
HOME2	HOME2R<3:0>	HOME2R	1011 = RPF1
QAEA3	QAEA3R<3:0>	QEA3R	
HOME4	HOME4R<3:0>	HOME4R	1100 = RPE0(1)
QEA5	QEA5R<3:0>	QEA5R	1101 = RPA15(1)
HOME6	HOME6R<3:0>	HOME6R	
FLT1	FLT1R<3:0>	FLT1R	1110 = Reserved
C3RX	C3RXR<3:0>	C3RXR	
REFCLKI	REFIR<3:0>	REFIR	1111 = Reserved

Note 1: This selection is not available on 64-pin devices.

REGISTER 16-5: DMTCNT: DEADMAN TIMER COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **COUNTER<31:0>:** Read current contents of DMT counter

REGISTER 16-6: DMTPSCNT: POST STATUS CONFIGURE DMT COUNT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<15:8>							
7:0	R-0	R-0	R-0	R-y	R-y	R-y	R-y	R-y
	PSCNT<7:0>							

Legend:		y= Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSCNT<31:0>:** DMT Instruction Count Value Configuration Status bits
This is always the value of the DMTCNT<4:0> bits in the DEVCFG1 Configuration register.

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TABLE 18-3: INPUT CAPTURE 10 THROUGH INPUT CAPTURE 16 REGISTER MAP

Virtual Address BF84_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3200	IC10CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3210	IC10BUF	31:16	IC10BUF<31:0>																xxxx
		15:0																	xxxx
3400	IC11CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3410	IC11BUF	31:16	IC11BUF<31:0>																xxxx
		15:0																	xxxx
3600	IC12CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3610	IC12BUF	31:16	IC12BUF<31:0>																xxxx
		15:0																	xxxx
3800	IC13CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3810	IC13BUF	31:16	IC13BUF<31:0>																xxxx
		15:0																	xxxx
3A00	IC14CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3A10	IC14BUF	31:16	IC14BUF<31:0>																xxxx
		15:0																	xxxx
3C00	IC15CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3C10	IC15BUF	31:16	IC15BUF<31:0>																xxxx
		15:0																	xxxx
3E00	IC16CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3E10	IC16BUF	31:16	IC16BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 20-4: SPIxBUF: SPIx BUFFER REGISTER ('x' = 1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>** FIFO Data bits
When MODE32 or MODE16 selects 32-bit data, the SPI uses DATA<31:0>.
When MODE32 or MODE16 selects 24-bit data, the SPI only uses DATA<24:0>.
When MODE32 or MODE16 selects 16-bit data, the SPI only uses DATA<15:0>.
When MODE32 or MODE16 selects 8-bit data, the SPI only uses DATA<7:0>.

REGISTER 20-5: SPIxBRG: SPIx BAUD RATE GENERATOR REGISTER ('x' = 1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	BRG<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BRG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **BRG<12:0>** Baud Rate Generator Divisor bits
Baud Rate = FPBCLKx / (2 * (SPIxBRG + 1)), where x = 2 and 3, (FPBCLK2 for SPI1-SPI2, FPBCLK3 for SPI3-SPI6.) Therefore, the maximum baud rate possible is FPBCLKx / 2 (SPIXBRG = 0) and the minimum baud rate possible is FPBCLKx / 16384.

Note: Changing the BRG value when the ON bit is equal to '1' causes undefined behavior.

NOTES:

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
76E0	ADCDATA14	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76F0	ADCDATA15	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7700	ADCDATA16	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7710	ADCDATA17	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7720	ADCDATA18	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7730	ADCDATA19	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7740	ADCDATA20(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7750	ADCDATA21(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7760	ADCDATA22(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7770	ADCDATA23(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7780	ADCDATA24	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7790	ADCDATA25	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
77A0	ADCDATA26	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
77B0	ADCDATA27	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7810	ADCDATA33(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7820	ADCDATA34(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7830	ADCDATA35(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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REGISTER 25-17: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6) (CONTINUED)

bit 24 **AFRDY:** Digital Filter 'x' Data Ready Status bit
1 = Data is ready in the FLTRDATA<15:0> bits
0 = Data is not ready

Note: This bit is cleared by reading the FLTRDATA<15:0> bits or by disabling the Digital Filter module (by setting AFEN to '0').

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **CHNLID<4:0>:** Digital Filter Analog Input Selection bits
These bits specify the analog input to be used as the oversampling filter data source.
11111 = Reserved
•
•
•
11100 = Reserved
11011 = AN27 input
11010 = AN26 input
11001 = AN25 input
11000 = AN24 input
10111 = AN23(1) input
10110 = AN22(1) input
10101 = AN21(1) input
10100 = AN20(1) input
10011 = AN19 input
•
•
•
10110 = AN6 input
00101 = ADC5 Module
00100 = ADC4 Module
00011 = ADC3 Module
00010 = ADC2 Module
00001 = ADC1 Module
00000 = ADC0 Module

Note: Only the first 32 analog inputs (Class 1 and Class 2) can use a digital filter.

bit 15-0 **FLTRDATA<15:0>:** Digital Filter 'x' Data Output Value bits
The filter output data is as per the fractional format set in the FRACT (ADCCON1<23>) bit. The FRACT bit should not be changed while the filter is enabled. Changing the state of the FRACT bit after the operation of the filter ended will not update the value of FLTRDATA<15:0> to reflect the new format.

Note 1: This selection is not available on 64-pin devices.

REGISTER 25-21: ADCTRG4: ADC TRIGGER SOURCE 4 REGISTER

bit 20-16 **TRGSRC14<4:0>:** Trigger Source for Conversion of Analog Input AN14 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC13<4:0>:** Trigger Source for Conversion of Analog Input AN13 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC12<4:0>:** Trigger Source for Conversion of Analog Input AN12 Select bits
See bits 28-24 for bit value definitions.

29.0 CONTROL DIGITAL-TO-ANALOG CONVERTER (CDAC)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MK GP/MC Family Control Digital-to-Analog Converter (CDAC) generates analog voltage corresponding to the digital inputs. The voltage can be used as a reference source for comparators or can be used as an offset to an Op amp. This module is targeted for control applications, as opposed to other DAC modules, which are used for audio applications.

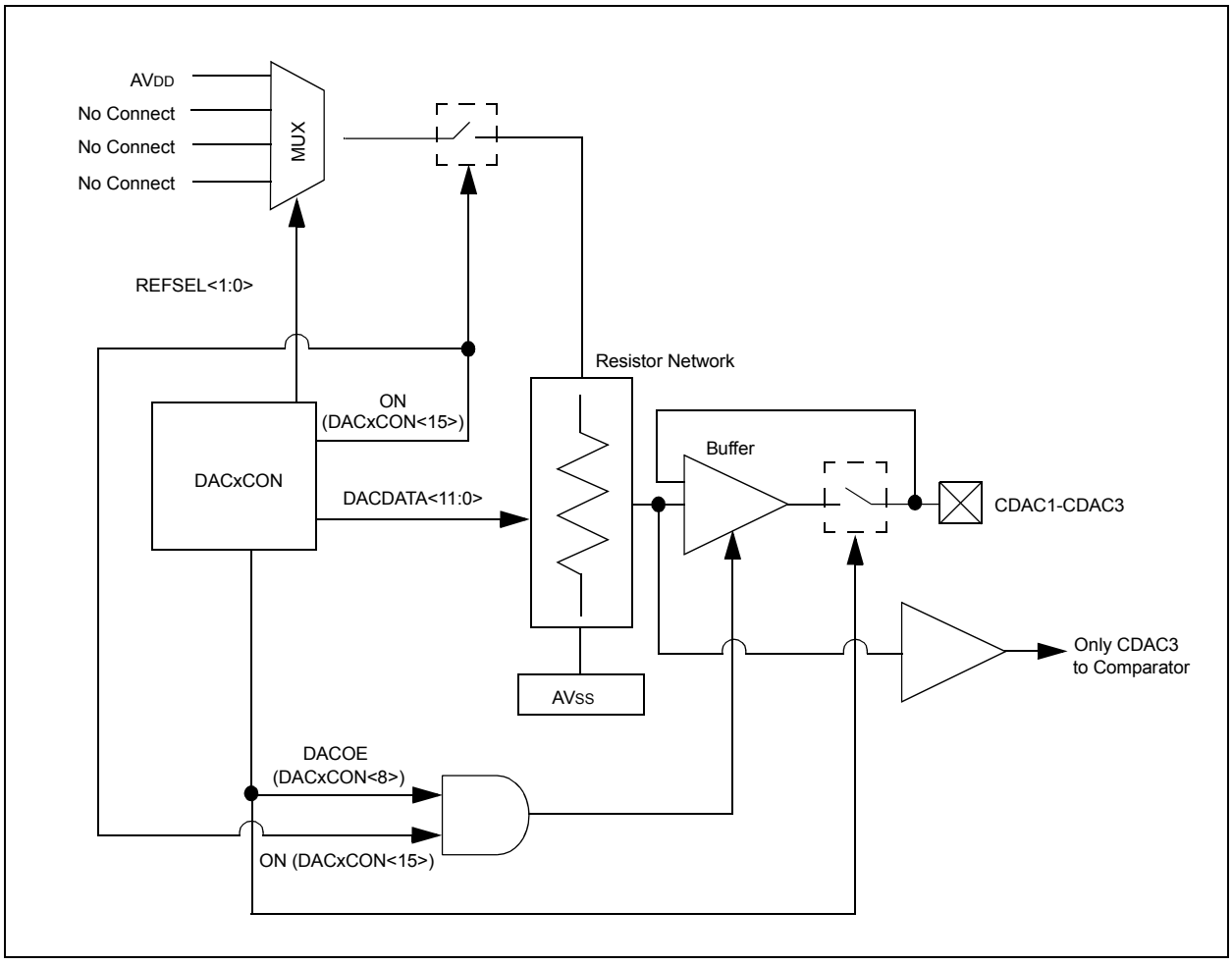
The following are key features of the CDAC module:

- Wide voltage range (1.8V to 3.6V)
- 12-bit resolution
- Fast conversion times, 1 Msps
- Buffered output for comparator use

Note: For additional information on conversion time, sampling rate, module turn-on time and glitch reduction circuit characteristics, refer to **Section 36.0 "Electrical Characteristics"**.

Figure 29-1 illustrates the functional block diagram of the CDAC module.

FIGURE 29-1: CDAC BLOCK DIAGRAM



30.0 QUADRATURE ENCODER INTERFACE (QEI)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 43. "Quadrature Encoder Interface (QEI)"** (DS60001346), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The QEI module consists of the following major features:

- Four input pins: two phase signals, an index pulse and a home pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- Count direction status
- 4x count resolution
- Index (INDX) pulse to reset the position counter
- General purpose 32-bit Timer/Counter mode
- Interrupts generated by QEI or counter events
- 32-bit velocity counter
- 32-bit position counter
- 32-bit index pulse counter
- 32-bit interval timer
- 32-bit position Initialization/Capture register
- 32-bit Compare Less Than and Greater Than registers
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Interval Timer mode

Figure 30-1 illustrates the QEI block diagram.

32.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes the power-saving features on the PIC32MK GP devices. These devices have multiple power domains and offer various methods and modes that allow the user to balance the power consumption with device performance.

32.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the speed of PBCLK7, or selecting a lower power clock source (i.e., LPRC or SOSC).

In addition, the Peripheral Bus Scaling mode is available for each peripheral bus where peripherals are clocked at reduced speed by selecting a higher divider for the associated PBCLKx, or by disabling the clock completely.

32.2 Power-Saving with CPU Halted

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

32.2.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted and the associated clocks are disabled. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the peripheral bus clocks will start running and the device will enter into Idle mode.

32.2.2 IDLE MODE

In Idle mode, the CPU is Halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

NOTES:

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TABLE 36-17: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-5	—	+5	%	0°C ≤ TA ≤ +70°C
		-10	—	+10	%	-40°C ≤ TA ≤ +125°C

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE 36-18: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal LPRC @ 32.768 kHz(1)						
F21	LPRC	-8	—	+8	%	0°C ≤ TA ≤ +85°C
		-25	—	+25	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

TABLE 36-43: CTMU CURRENT SOURCE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU CURRENT SOURCE							
CTMU0	RES	Resolution	-2	—	+2	ºC	3.3V @ -40ºC to 125ºC
CTMUI1	IOUT1	Base Range(1)	—	0.55	—	µA	CTMUCON<1:0> = 01
CTMUI2	IOUT2	10x Range(1)	—	5.5	—	µA	CTMUCON<1:0> = 10
CTMUI3	IOUT3	100x Range(1)	—	55	—	µA	CTMUCON<1:0> = 11
CTMUI4	IOUT4	1000x Range(1)	—	550	—	µA	CTMUCON<1:0> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage(1,2)	—	0.598	—	V	TA = +25ºC, CTMUCON<1:0> = 01
			—	0.658	—	V	TA = +25ºC, CTMUCON<1:0> = 10
			—	0.721	—	V	TA = +25ºC, CTMUCON<1:0> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change(1,2)	—	-1.92	—	mV/ºC	CTMUCON<1:0> = 01
			—	-1.74	—	mV/ºC	CTMUCON<1:0> = 10
			—	-1.56	—	mV/ºC	CTMUCON<1:0> = 11

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

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