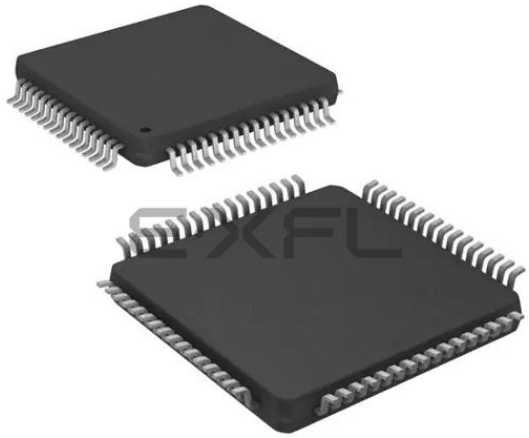

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 27x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024mcf064-i-pt

TABLE 1-21: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

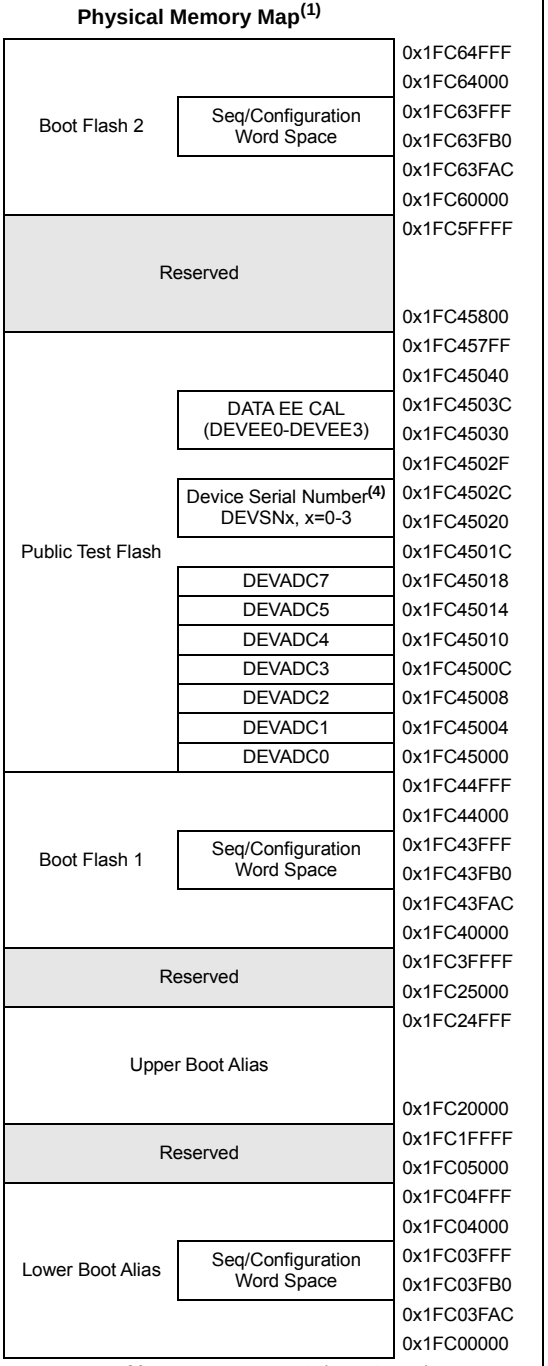
Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
JTAG					
TCK	3	1	I	ST	JTAG Test Clock Input Pin
TDI	49	31	I	ST	JTAG Test Data Input Pin
TDO	100	64	O	—	JTAG Test Data Output Pin
TMS	76	49	I	ST	JTAG Test Mode Select Pin
Trace					
TRCLK	91	50	O	CMOS	Trace Clock
TRD0	97	54	O	CMOS	Trace Data bits 0-3 Trace support is available through the MPLAB® REAL ICE™ In-circuit Emulator.
TRD1	96	53	O	CMOS	
TRD2	95	52	O	CMOS	
TRD3	92	51	O	CMOS	
Programming/Debugging					
PGED1	27	18	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	26	17	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	69	43	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	70	44	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	24	15	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
PGEC3	25	16	I	ST	Clock input pin for Programming/Debugging Communication Channel 3
$\overline{\text{MCLR}}$	13	7	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	Reserved	Reserved in the PIC32MK GP Family core.
18	Reserved	Reserved in the PIC32MK GP Family core.
19	Reserved	Reserved in the PIC32MK GP Family core.
20-22	Reserved	Reserved in the PIC32MK GP Family core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	Reserved	Reserved in the PIC32MK GP Family core.
27	Reserved	Reserved in the PIC32MK GP Family core.
28	Reserved	Reserved in the PIC32MK GP Family core.
29	Reserved	Reserved in the PIC32MK GP Family core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

FIGURE 4-3: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.
2: Memory locations 0x1FC03FB0 through 0x1FC03FFC are used to initialize Configuration registers (see **33.0 "Special Features"**).
3: Refer to **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.
4: Memory locations 0x1FC5020 and 0x1FC502C contain a unique device serial number (see **33.0 "Special Features"**).
5: This configuration space cannot be used for executing code in the upper Boot Alias.

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
CFG-PMD	0xBF800000	0x0000
CACHE		0x0800
FC-NVM		0x0A00
WDT		0x0C00
DMT		0x0E00
ICD		0x1000
CRU		0x1200
PPS		0x1400
PLVD		0x1800
EVIC	0xBF810000	0x0000
DMA		0x1000
Timer1-Timer9	0xBF820000	0x0000
IC1-IC9		0x2000
OC1-OC9		0x4000
I2C1-I2C2		0x6000
SPI1-SPI2		0x7000
UART1-UART2		0x8000
DATAEE		0x9000
PWM1-PWM12		0xA000
QEI1-QEI6		0xB200
CMP		0xC000
CDAC1		0xC200
CTMU		0xD000
PMP		0xE000
IC10-IC16	0xBF840000	0x3200
OC10-OC16		0x5200
I2C3-I2C4		0x6400
SPI3-SPI6		0x7400
UART3-UART6		0x8400
CDAC2-CDAC3		0xC400
PORTA-PORTG	0xBF860000	0x0000
CAN1-CAN4	0xBF880000	0x0000
ADC		0x7000
USB1-USB2		0x9000
RTCC	0xBF8C0000	0x0000
Deep Sleep		0x0200
SSX CTL	0xBF8F0000	0x0000

Note 1: Refer to **4.2 "System Bus Arbitration"** for important legal information.

REGISTER 10-3: CHEMIS: CACHE MISS STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEMIS<31:0>:** Instruction Cache Miss Count bits

When the CHEPERFEN bit (CHECON<12>) = 1, the CHEMIS<31:0> bits increment each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

The CHEMIS<31:0> bits are reset on a '0' to '1' transition of the CHEPERFEN bit.

TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14A0	DCH5DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
14B0	DCH5CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
14C0	DCH5CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
14D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
14E0	DCH6CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
14F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1510	DCH6SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1520	DCH6DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
15A0	DCH7CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-12: PORTF REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CN STATF1	CN STATF0	0000
05A0	CNNEF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNNEF1	CNNEF0	0000
05B0	CNFF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNFF1	CNFF0	0000
05C0	SRCON0F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR0F1	SR0F0	0000
05D0	SRCON1F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR1F1	SR1F0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-13: PORTG REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSG15	—	—	—	ANSG11	ANSG10	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	8FC0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	TRISG11	TRISG10	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	TRISG1	TRISG0	FFC3
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	RG11	RG10	RG9	RG8	RG7	RG6	—	—	—	—	RG1	RG0	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	LATG11	LATG10	LATG9	LATG8	LATG7	LATG6	—	—	—	—	LATG1	LATG0	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	ODCG11	ODCG10	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	ODCG1	ODCG0	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUG15	CNPUG14	CNPUG13	CNPUG12	CNPUG11	CNPUG10	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	CNPUG1	CNPUG0	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDG15	CNPDG14	CNPDG13	CNPDG12	CNPDG11	CNPDG10	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	CNPDG1	CNPDG0	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEG15	CNIEG14	CNIEG13	CNIEG12	CNIEG11	CNIEG10	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	CNIEG1	CNIEG0	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATG15	CN STATG14	CN STATG13	CN STATG12	CN STATG11	CN STATG10	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	CN STATG1	CN STATG0	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEG15	CNNEG14	CNNEG13	CNNEG12	CNNEG11	CNNEG10	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	CNNEG1	CNNEG0	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFG15	CNFG14	CNFG13	CNFG12	CNFG11	CNFG10	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	CNFG1	CNFG0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

14.3 Timer1 Control Register

TABLE 14-1: TIMER1 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

20.1 SPI Control Registers

TABLE 20-1: SPI1 AND SPI2 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7010	SPI1STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7020	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7030	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7040	SPI1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00
7200	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7210	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7220	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7230	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7240	SPI2CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
73E0	ADCEISTAT1	31:16	—	—	—	—	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23(1)	EIRDY22(1)	EIRDY21(1)	EIRDY20(1)	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
73F0	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	EIRDY53	EIRDY52	—	EIRDY50	EIRDY49	EIRDY48	0000
		15:0	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIRDY41(1)	EIRDY40(1)	EIRDY39(1)	EIRDY38(1)	EIRDY37(1)	EIRDY36(1)	EIRDY35(1)	EIRDY34(1)	EIRDY33(1)	—	0000
7400	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	WKIEN5	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	WKRDY5	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	ANEN5	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
7600	ADCDATA0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7610	ADCDATA1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7620	ADCDATA2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7630	ADCDATA3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7640	ADCDATA4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7650	ADCDATA5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7660	ADCDATA6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7670	ADCDATA7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7680	ADCDATA8	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7690	ADCDATA9	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76A0	ADCDATA10	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76B0	ADCDATA11	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76C0	ADCDATA12	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76D0	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., V_{BAT}, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

REGISTER 25-2: ADCCON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						

Legend:	HC = Hardware Set	HS = Hardware Cleared	r = Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **BGVRRDY:** Band Gap Voltage/ADC Reference Voltage Status bit
1 = Both band gap voltage and ADC reference voltages (VREF) are ready
0 = Either or both band gap voltage and ADC reference voltages (VREF) are not ready

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to '0' when ON (ADCCON1<15>) = 0.

bit 30 **REFFLT:** Band Gap/VREF/AVDD BOR Fault Status bit
1 = Fault in band gap or the VREF voltage while the ON bit (ADCCON1<15>) was set. Most likely a band gap or VREF fault will be caused by a BOR of the analog VDD supply.
0 = Band gap and VREF voltage are working properly

This bit is cleared when the ON bit (ADCCON1<15>) = 0 and the BGVRRDY bit = 1.

bit 29 **EOSRDY:** End of Scan Interrupt Status bit
1 = All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning
0 = Scanning has not completed

This bit is cleared when ADCCON2<31:24> are read in software.

bit 28-26 **CVDCPL<2:0>:** Capacitor Voltage Divider (CVD) Setting bits
111 = 7 * 2.5 pF = 17.5 pF
110 = 6 * 2.5 pF = 15 pF
101 = 5 * 2.5 pF = 12.5 pF
100 = 4 * 2.5 pF = 10 pF
011 = 3 * 2.5 pF = 7.5 pF
010 = 2 * 2.5 pF = 5 pF
001 = 1 * 2.5 pF = 2.5 pF
000 = 0 * 2.5 pF = 0 pF

Note: These bits are available only on shared ADC7 inputs AN6-AN49. Once enabled (CVDCPL<2:0>) > 000), the internal capacitors are internally connected to all ADC7 inputs. To determine user ADC sampling time requirements (SAMC<9:0> bits (ADCCON2<25:16>)) with CVDCPL selection, refer to **Table 36-41: "ADC Sample Times with CVD Enabled"**.

REGISTER 25-18: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of ADC3 Module Select bits
- 11111 = Reserved
- 11110 = Reserved
- 11101 = PWM Generator 6 Current-Limit (Motor Control Variants Only)
- 11100 = PWM Generator 5 Current-Limit (Motor Control Variants Only)
- 11011 = PWM Generator 4 Current-Limit (Motor Control Variants Only)
- 11010 = PWM Generator 3 Current-Limit (Motor Control Variants Only)
- 11001 = PWM Generator 2 Current-Limit (Motor Control Variants Only)
- 11000 = PWM Generator 1 Current-Limit (Motor Control Variants Only)
- 10111 = Reserved
- 10110 = Reserved
- 10101 = Reserved
- 10100 = CTMU trip
- 10011 = Output Compare 4 (Rising Edge Only)
- 10010 = Output Compare 3 (Rising Edge Only)
- 10001 = Output Compare 2 (Rising Edge Only)
- 10000 = Output Compare 1 (Rising Edge Only)
- 01111 = PWM Generator 6 trigger (Motor Control Variants Only)
- 01110 = PWM Generator 5 trigger (Motor Control Variants Only)
- 01101 = PWM Generator 4 trigger (Motor Control Variants Only)
- 01100 = PWM Generator 3 trigger (Motor Control Variants Only)
- 01011 = PWM Generator 2 trigger (Motor Control Variants Only)
- 01010 = PWM Generator 1 trigger (Motor Control Variants Only)
- 01001 = Secondary Special Event trigger (Motor Control Variants Only)
- 01000 = Primary Special Event trigger (Motor Control Variants Only)
- 00111 = General Purpose Timer5
- 00110 = General Purpose Timer3
- 00101 = General Purpose Timer1
- 00100 = INT0
- 00011 = Scan trigger (see **Note**)
- 00010 = Software level trigger
- 00001 = Software edge trigger
- 00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

27.1 Op amp Interface

PIC32MK GP devices implement a total of five comparators and four Op amps. The Op amp Comparator module 4 does not implement the associated Op amp. The Op amp can be configured to operate in two different modes: Regular Op amp mode and Unity Gain mode.

When an Op amp is available on a Op amp/Comparator module, both of its inputs and output are accessible at the device pins. The Op amp's Unity Gain mode is the only exception to this rule, which is described in **27.6 "Op amp Unity Gain Mode"**. The Op amp is disabled at reset and has to be enabled by writing a '1' to the OAO bit (CMxCON <11>), followed by enabling the Op amp by writing a '1' to the AMPMOD bit (CMxCON <10>).

The Op amp outputs are capable of rail-to-rail operation, which are limited by the maximum output load current. Refer to **36.0 "Electrical Characteristics"** for the Op amp minimum gain requirements and VOH/VOL loading specifications.

Note:	The exception to the minimum gain specification is the special internal Unity Gain buffer mode.

Table 27-1 provides the different SFR bits and their logic states to set the Op amp in two different modes of operation.

TABLE 27-1: OP AMP OPERATION STATES

Configuration	OAO bit (CMxCON<11>)	AMPMOD bit (CMxCON<10>)	ENPGAx bits (CFGCON2<4, 2:0>)
Op amp	1	1	0
Unity Gain Buffer	1	1	1
No function/disabled	0	0	0
Reserved	Don't care	0	1

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 25 **CLPOL:** Current-Limit Polarity bits for PWM Generator 'x'(2,4)
1 = The selected current-limit source is active-low
0 = The selected current-limit source is active-high

bit 24 **CLMOD:** Current-Limit Mode Enable bit for PWM Generator 'x'(2,4)
1 = Current-limit function is enabled
0 = Current-limit function is disabled, current-limit overrides disabled (current-limit interrupts can still be generated). If Faults are enabled, FLTMOD will override the CLMOD bit.
Changes take effect on the next PWM cycle boundary following PWM being enabled, and subsequently on each PWM cycle boundary. When updating CLMOD from '1' to '0', if the current-limit input is still active, the current-limit override condition will not be removed.

bit 23 **Unimplemented:** Read as '0'

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 33-5: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 25-21 **DSWDTPS<4:0>:** Deep Sleep Watchdog Timer Postscale Select bits
The DS WDT prescaler is 32; this creates an approximate base time unit of 1 ms.
11111 = 1:236 (25.7 days)
11110 = 1:235 (12.8 days)
11101 = 1:234 (6.4 days)
11100 = 1:233 (77.0 hours)
11011 = 1:232 (38.5 hours)
11010 = 1:231 (19.2 hours)
11001 = 1:230 (9.6 hours)
11000 = 1:229 (4.8 hours)
10111 = 1:228 (2.4 hours)
10110 = 1:227 (72.2 minutes)
10101 = 1:226 (36.1 minutes)
10100 = 1:225 (18.0 minutes)
10011 = 1:224 (9.0 minutes)
10010 = 1:223 (4.5 minutes)
10001 = 1:222 (135.3 s)
10000 = 1:221 (67.7 s)
01111 = 1:220 (33.825 s)
01110 = 1:219 (16.912 s)
01101 = 1:218 (8.456 s)
01100 = 1:217 (4.228 s)
01011 = 1:65536 (2.114 s)
01010 = 1:32768 (1.057 s)
01001 = 1:16384 (528.5 ms)
01000 = 1:8192 (264.3 ms)
00111 = 1:4096 (132.1 ms)
00110 = 1:2048 (66.1 ms)
00101 = 1:1024 (33 ms)
00100 = 1:512 (16.5 ms)
00011 = 1:256 (8.3 ms)
00010 = 1:128 (4.1 ms)
00001 = 1:64 (2.1 ms)
00000 = 1:32 (1 ms)

bit 20 **DSBOREN:** Deep Sleep Zero-Power BOR Enable bit
1 = Enable ZPBOR during deep sleep
0 = Disable ZPBOR during deep sleep

bit 19 **VBATBOREN:** VBAT Zero-Power BOR Enable bit
1 = Enable ZPBOR during VBAT mode
0 = Disable ZPBOR during VBAT mode

bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits
111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2

bit 15 **Reserved:** Write as ‘1’

36.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MK GP/MC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MK GP/MC devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on V_{BAT} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on V_{DD} with respect to V_{USB3V3} ..... V_{USB3V3} -0.3V to V_{USB3V3} +0.3V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} +0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to V_{USB3V3} ..... Vss -0.3V to V_{USB3V3} +0.3V
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 200 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 200 mA
Maximum current sunk/sourced by any 4x I/O pin **(Note 4)** ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin **(Note 4)** ..... 25 mA
Maximum current sunk by all ports ..... 150 mA
Maximum current sourced by all ports **(Note 2)** ..... 150 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 36-2).

3: See the pin name tables (Table 3 and Table 5) for the 5V tolerant pins.

4: Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x and 8x I/O pin lists.

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

37.0 AC AND DC CHARACTERISTICS GRAPHS

Note: The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 37-1: VOH – 4x DRIVER PINS

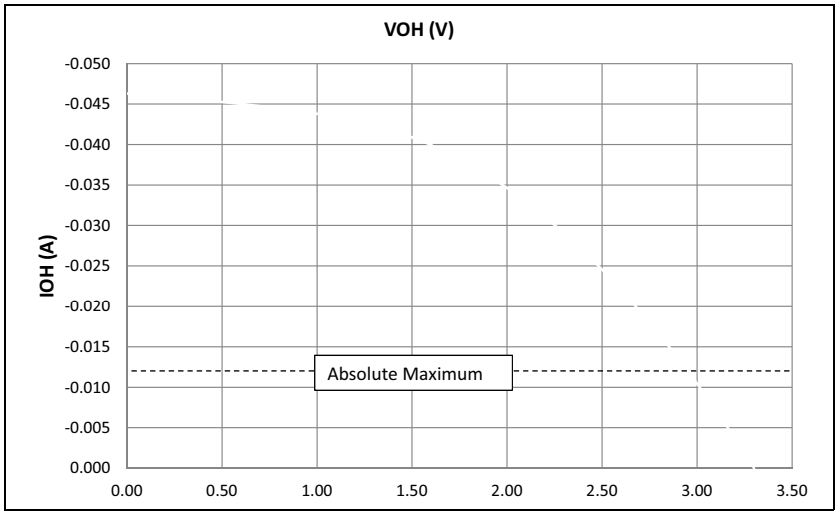


FIGURE 37-2: VOL – 4x DRIVER PINS

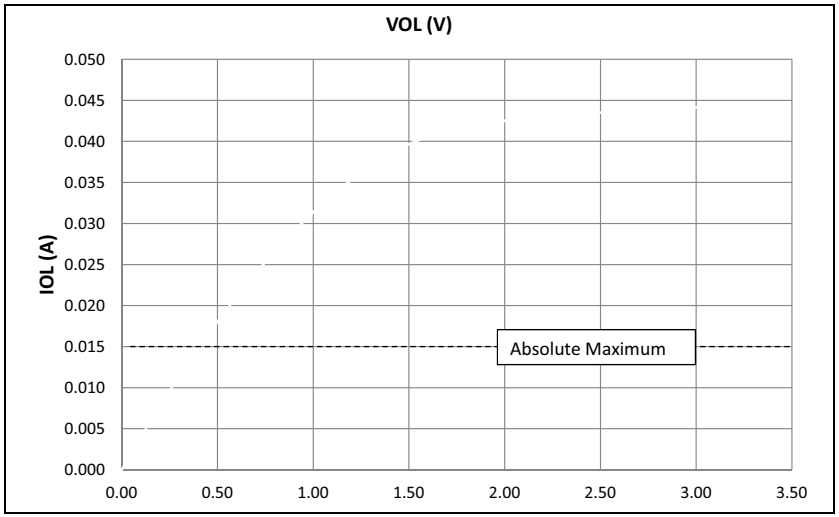


FIGURE 37-3: VOH – 8x DRIVER PINS

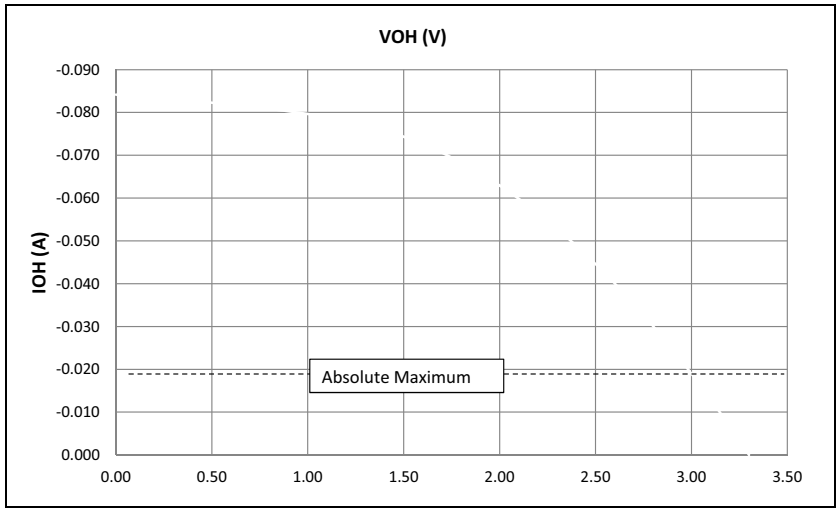
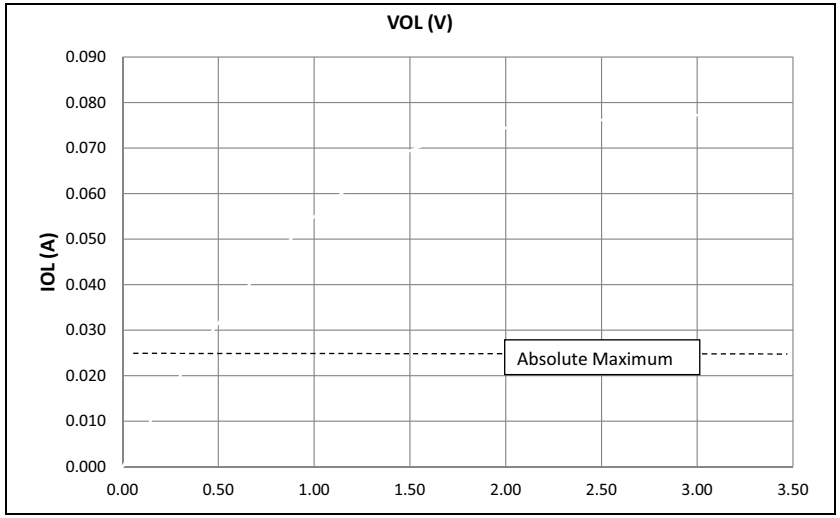
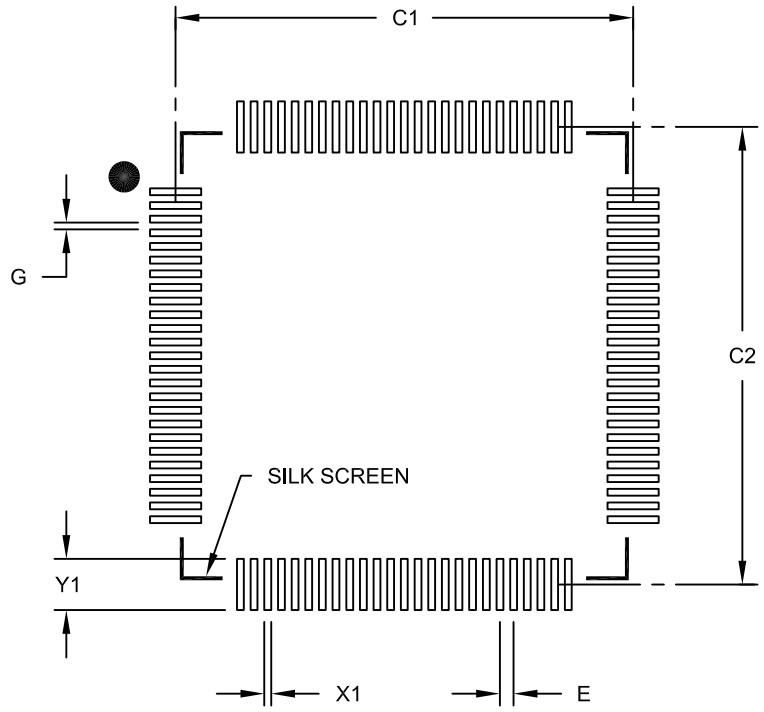


FIGURE 37-4: VOL – 8x DRIVER PINS



100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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