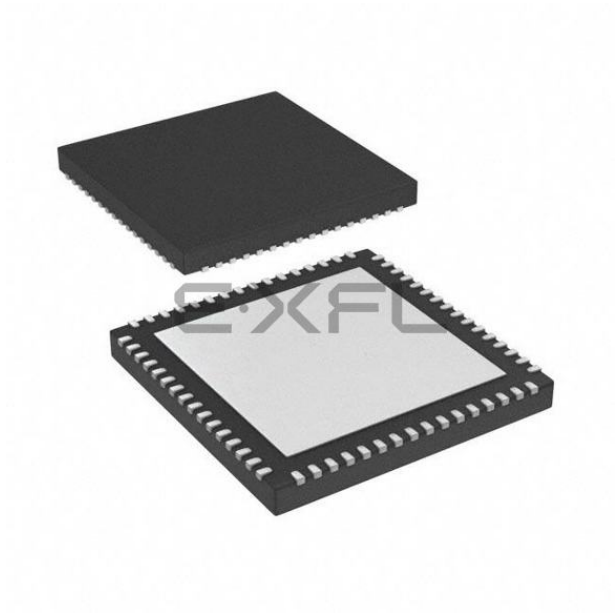
Microchip Technology - PIC32MK1024MCF064T-I/MR Datasheet



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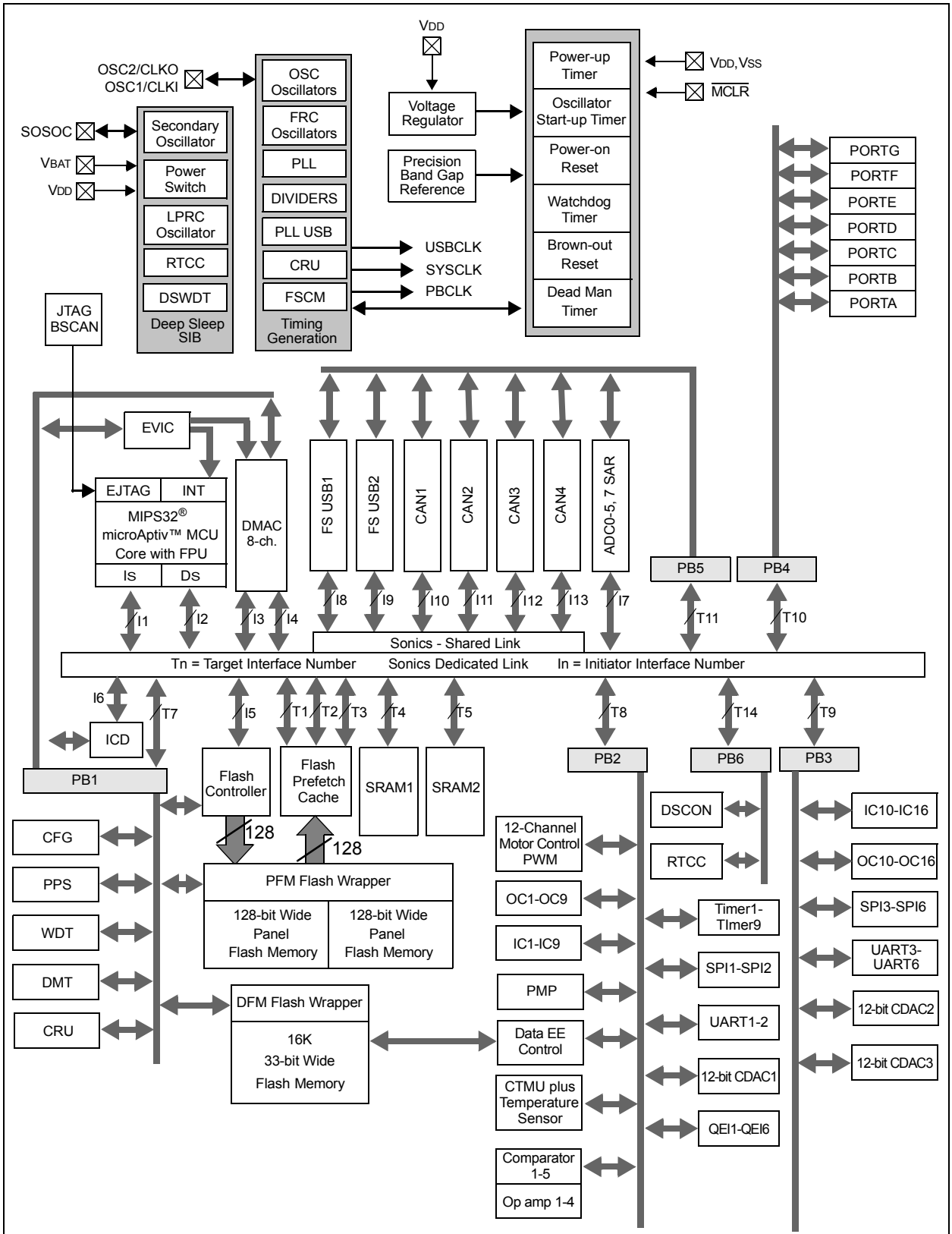
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 27x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024mcf064t-i-mr

FIGURE 1-1: PIC32MK GP/MC FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to the family feature tables (Table 1 and Table 2) for the list of available features by device.

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CLKI	63	39	I	ST	External clock source input. Always associated with OSC1 pin function.
CLKO	64	40	O	CMOS	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	63	39	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	64	40	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	73	47	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	74	48	O	CMOS	32.768 low-power oscillator crystal output.
REFCLKI	PPS	PPS	I	—	One of several alternate REFCLKOx user-selectable input clock sources.
REFCLKO1	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO2	PPS	PPS	O	—	
REFCLKO3	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-3: IC1 THROUGH IC16 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Input Capture					
IC1	PPS	PPS	I	ST	Input Capture Inputs 1-6
IC2	PPS	PPS	I	ST	
IC3	PPS	PPS	I	ST	
IC4	PPS	PPS	I	ST	
IC5	PPS	PPS	I	ST	
IC6	PPS	PPS	I	ST	
IC7	PPS	PPS	I	ST	
IC8	PPS	PPS	I	ST	
IC9	PPS	PPS	I	ST	
IC10	PPS	PPS	I	ST	
IC11	PPS	PPS	I	ST	
IC12	PPS	PPS	I	ST	
IC13	PPS	PPS	I	ST	
IC14	PPS	PPS	I	ST	
IC15	PPS	PPS	I	ST	
IC16	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 7-1: RCON: RESET CONTROL REGISTER

bit 5 **DMTO:** Deadman Timer Time-out Flag bit
1 = A DMT time-out has occurred
0 = A DMT time-out has not occurred

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

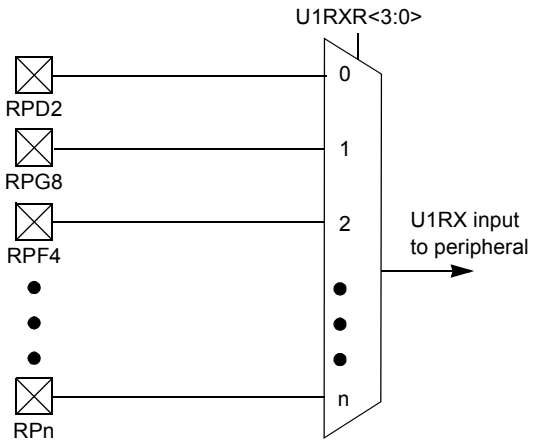
Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Reserved	—	233	—	—	—	—	—	—
Reserved	—	234	—	—	—	—	—	—
Reserved	—	235	—	—	—	—	—	—
Reserved	—	236	—	—	—	—	—	—
Reserved	—	237	—	—	—	—	—	—
PWM7 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM7_VECTOR	238	OFF238<17:1>	IFS7<14>	IEC7<14>	IPC59<20:18>	IPC59<17:16>	Yes
PWM8 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM8_VECTOR	239	OFF239<17:1>	IFS7<15>	IEC7<15>	IPC59<28:26>	IPC59<25:24>	Yes
PWM9 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM9_VECTOR	240	OFF240<17:1>	IFS7<16>	IEC7<16>	IPC60<4:2>	IPC60<1:0>	Yes
PWM10 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM10_VECTOR	241	OFF241<17:1>	IFS7<17>	IEC7<17>	IPC60<12:10>	IPC60<9:8>	Yes
PWM11 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM11_VECTOR	242	OFF242<17:1>	IFS7<18>	IEC7<18>	IPC60<20:18>	IPC60<17:16>	Yes
PWM12 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM12_VECTOR	243	OFF243<17:1>	IFS7<19>	IEC7<19>	IPC60<28:26>	IPC60<25:24>	Yes
USB2 Combined Interrupt(2)	_USB_2_VECTOR	244	OFF244<17:1>	IFS7<20>	IEC7<20>	IPC61<4:2>	IPC61<1:0>	Yes
ADC Digital Comparator 3	_ADC_DC3_VECTOR	245	OFF245<17:1>	IFS7<21>	IEC7<21>	IPC61<12:10>	IPC61<9:8>	Yes
ADC Digital Comparator 4	_ADC_DC4_VECTOR	246	OFF246<17:1>	IFS7<22>	IEC7<22>	IPC61<20:18>	IPC61<17:16>	Yes
Reserved	—	247	—	—	—	—	—	—
Reserved	—	248	—	—	—	—	—	—
Reserved	—	249	—	—	—	—	—	—
Reserved	—	250	—	—	—	—	—	—
Reserved	—	251	—	—	—	—	—	—
Reserved	—	252	—	—	—	—	—	—
Reserved	—	253	—	—	—	—	—	—
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	254	OFF254<17:1>	IFS7<30>	IEC7<30>	IPC63<20:18>	IPC63<17:16>	—
Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	255	OFF255<17:1>	IFS7<31>	IEC7<31>	IPC63<28:26>	IPC63<25:24>	—
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

FIGURE 13-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 13-4: PORTA REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ANSA12	ANSA11	—	—	ANSA8	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0623
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TRISA12	TRISA11	TRISA10	—	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	06FF
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	RA12	RA11	RA10	—	RA8	RA7	—	—	RA4	—	—	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LATA12	LATA11	LATA10	—	LATA8	LATA7	—	—	LATA4	—	—	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ODCA12	ODCA11	ODCA10	—	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNPUA12	CNPUA11	CNPUA10	—	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNPDA12	CNPDA11	CNPDA10	—	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNIEA12	CNIEA11	CNIEA10	—	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CN STATA12	CN STATA11	CN STATA10	—	CN STATA8	CN STATA7	—	—	CN STATA4	—	—	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNNEA12	CNNEA11	CNNEA10	—	CNNEA8	CNNEA7	—	—	CNNEA4	—	—	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNFA12	CNFA11	CNFA10	—	CNFA8	CNFA7	—	—	CNFA4	—	—	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR0A10	—	SR0A8	SR0A7	—	—	—	—	—	—	—	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR1A10	—	SR1A8	SR1A7	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 13-6: PORTC REGISTER MAP FOR 64-PIN AND 100-PIN DEVICES

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ANSC12	ANSC11	ANSC10	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	1007
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	TRISC11	TRISC10	TRIS92	TRISC8	TRISC7	TRISC6	—	—	—	TRISC2	TRISC1	TRISC0	FFC7
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	—	—	—	RC2	RC1	RC0	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	—	—	—	LATC2	LATC1	LATC0	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	—	—	—	ODCC2	ODCC1	ODCC0	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	—	—	—	CNPUC2	CNPUC1	CNPUC0	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	—	—	—	CNPDC2	CNPDC1	CNPDC0	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC7	—	—	—	CNIEC2	CNIEC1	CNIEC0	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATC15	CN STATC14	CN STATC13	CN STATC12	CN STATC11	CN STATC10	CN STATC9	CN STATC8	CN STATC7	CN STATC6	—	—	—	CN STATC2	CN STATC1	CN STATC0	0000
02A0	CNNEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	CNNEC11	CNNEC10	CNNEC9	CNNEC8	CNNEC7	CNNEC6	—	—	—	CNNEC2	CNNEC1	CNNEC0	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	CNFC11	CNFC10	CNFC9	CNFC8	CNFC7	CNFC6	—	—	—	CNFC2	CNFC1	CNFC0	0000
02C0	SRCON0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0C15	—	—	—	SR0C11	—	SR0C9	SR0C8	SR0C7	SR0C6	—	—	—	—	—	—	0000
02D0	SRCON1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1C15	—	—	—	SR1C11	—	SR1C9	SR1C8	SR1C7	SR1C6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

NOTES:

REGISTER 18-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1-16)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit
1 = Module enabled
0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
1 = Halt in CPU Idle mode
0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
1 = Capture rising edge first
0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
1 = 32-bit timer resource capture
0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')(1)
0 = Timery is the counter source for capture
1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty; at least one more capture value can be read
0 = Input capture buffer is empty

Note 1: Refer to Table 18-1 for Timerx and Timery selections.

19.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

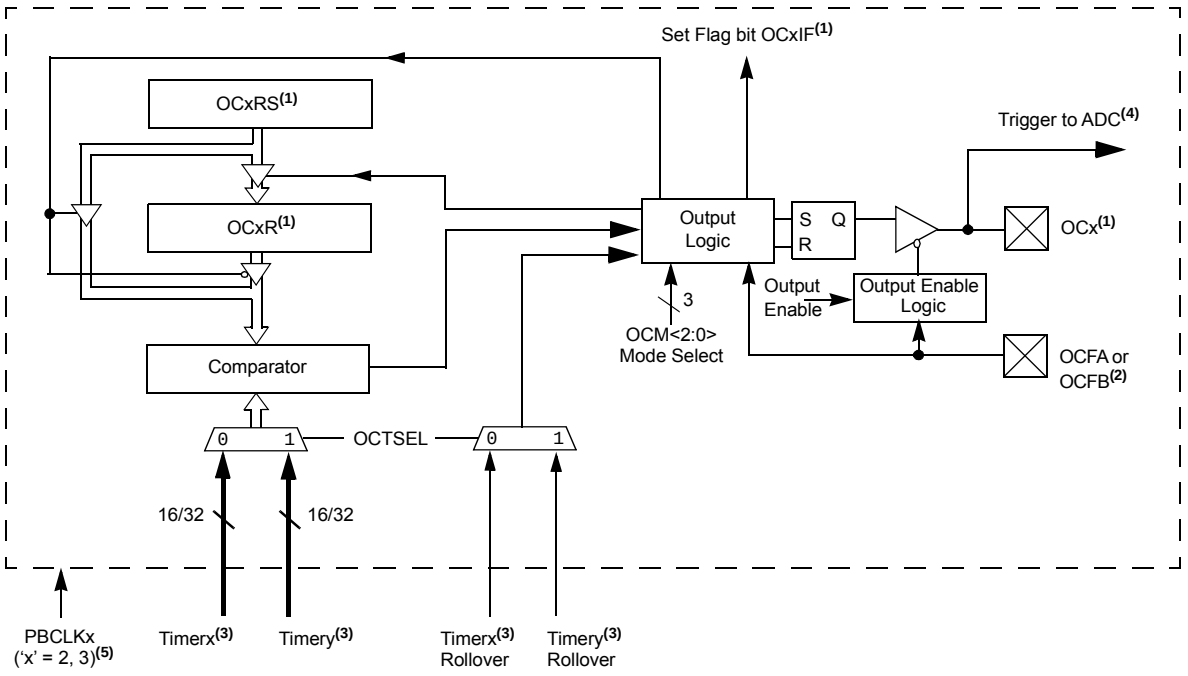
The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events.

For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features of the Output Compare:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base
- ADC event trigger for OC1 through OC4

FIGURE 19-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 9.

2: The OCFA pin controls the OCMP1-OCMP3, OCMP7-OCMP9, and OCMP13-OCMP15 channels. The OCFB pin controls the OCMP4-OCMP6, OCMP10-OCMP12, and OCMP16 channels.

3: Refer to Table 19-1 for Timerx and Timery selections.

4: The ADC event trigger is only available on OC1 through OC4.

5: PBCLK2 = Output Compare 1 through Output Compare 9; PBCLK3 = Output Compare 10 through Output Compare 16.

22.3 Module Operation

22.3.1 INITIALIZATION

Clearing the ON bit (i.e, = 0), which disables the UART module, will do the following:

- Aborts all pending transmissions and receptions and resets the module, as follows:
  - Reset the RX/TX buffers/FIFO to empty states (any data characters in the buffers are lost)
  - Resets the baud rate counter (UxBRG is not affected, only the counter)
  - Resets all error and status flags: URXDA, OERR, FERR, PERR, UTXBRK, UTXBF are cleared and RIDLE, TRMT are set
- Stop clocks to the entire module with the exception of the SFRs, saving power
- Surrenders control of the module I/O pins

Note:	Once the ON bit is set, it should not be cleared until the CLKRDY bit is read to be a logic '1'. This allows proper synchronization of the status and output signals. Otherwise, glitches in the status signals or BRG clock can occur.

Setting the ON bit (i.e., = 1), which enables the UART module, will do the following:

- The UART module controls the I/O pins as defined by the UEN bits, overriding the port TRIS and LATCH register bit settings
- UxTX is forced as an output driving the idle state defined by the UTXINV bit, when no transmissions are taking place
- UxRX is configured as an input
- If CTS and RTS are enabled, CTS is forced as an input and the RTS/BCLK pin functions as RTS output
- If BCLK is enabled, the RTS/BCLK output drives the 16x baud clock output

Note:	The ON bit should not be set (i.e., = 1) unless the CLKRDY bit is read to be a logic '0'.

22.4 Serial Protocols Usage

22.4.1 DATA TERMINAL EQUIPMENT (DTE) WITH FLOW CONTROL

When connecting to the DTE (typically a PC) and flow control is desired, set the UEN bit = 10 to enable CTS and RTS, and set the RTSMD bit = 0.

22.4.2 IEEE-485

To use the UART module in the IEEE-485 protocol, use the address detection feature to detect message frames. Normally, set the UEN bit = '01' to drive the RTS pin and control the bus driver, and set the RTSMD bit = 1.

22.4.3 LIN BUS

To transmit on a LIN bus, the transmitter must send a frame in 8,N,1 format consisting of a break, a synchronization character (0x55), and the message body. The module has extensive support for the LIN protocol including bus wake-up for a slave node as well as auto-baud detection and BREAK character transmit for master nodes. When in LIN mode, the software should program the BRGH bit = 0, which insures a 16x baud clock is used with majority detect.

26.0 CONTROLLER AREA NETWORK (CAN)

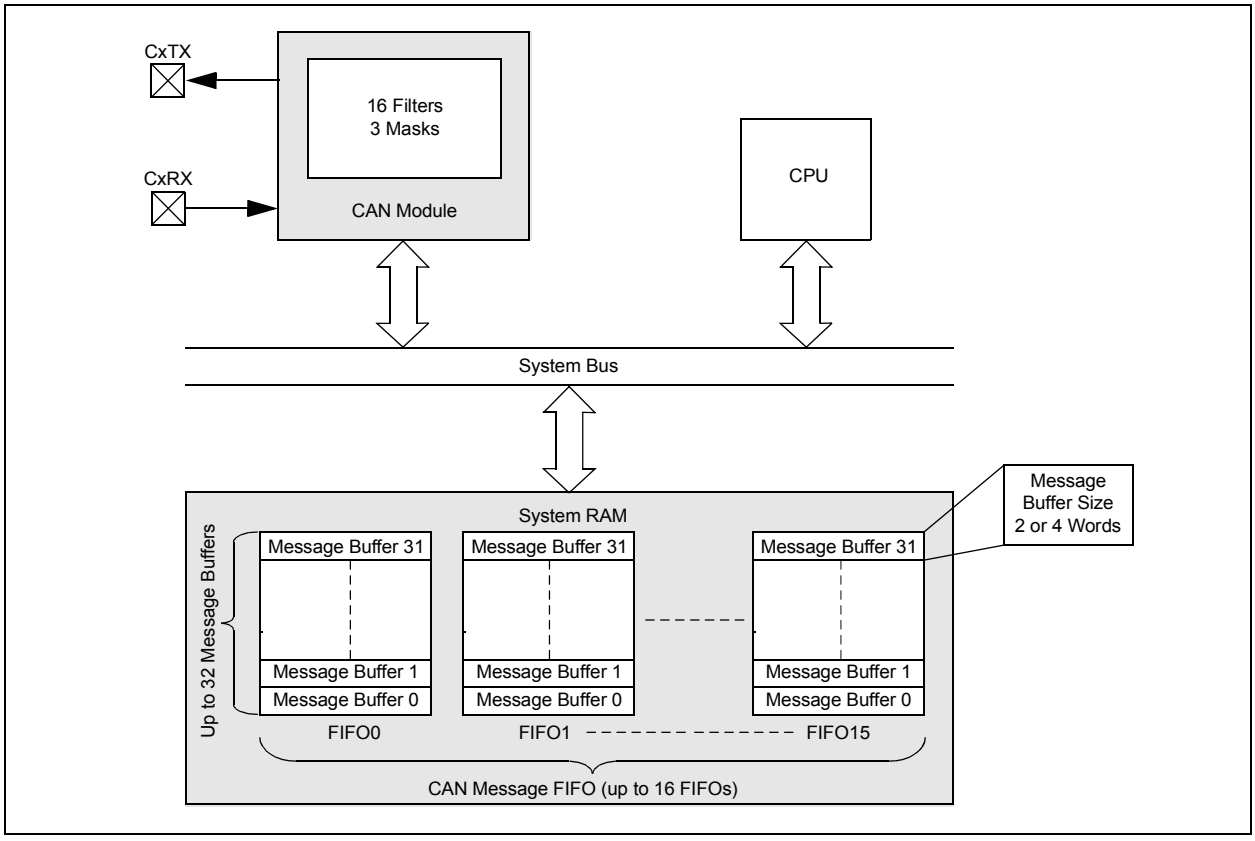
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 16 message FIFOs
  - Each FIFO can have up to 32 messages for a total of 512 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 16 acceptance filters for message filtering
  - Three acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32MK system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 26-1 illustrates the general structure of the CAN module.

FIGURE 26-1: PIC32MK CAN MODULE BLOCK DIAGRAM



REGISTER 30-6: VELxHLD: VELOCITY HOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **VELHLD<31:0>:** 32-bit Velocity Hold bits
When VELxCNT is read, the contents are captured at the same time into the VELxHLD register.

REGISTER 30-7: INTxHLD: INTERVAL TIMER HOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **INTHLD<31:0>:** 32-bit Index Counter Hold bits
When the next count pulse is detected, the current contents of the interval timer (INTxTMR) are transferred to the Interval Hold register (INTxHLD) and the interval timer is cleared and the process repeats.

REGISTER 30-10: QEIxICC: QEIx INITIALIZE/CAPTURE/COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ICCH<31:0>:** 32-bit Initialize/Capture/Compare High bits

REGISTER 30-11: QEIxCMPL: CAPTURE LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CMPL<31:0>:** 32-bit Compare Low Value bits

REGISTER 31-19: TRIGx: PWM PRIMARY TRIGGER COMPARE VALUE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGCMP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGCMP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **TRGCMP<15:0>:** Trigger Compare Value bits

These bits specify the value to match against the local time base register PTMRx to generate a trigger to the ADC module, and an interrupt if the TRGIEN bit (PWMCONx<21>) is set.

Note: To generate a trigger at the PWM period boundary, set the compare value = 0.

33.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MK GP/MC devices is designed to operate at a nominal 1.2V. To simplify system designs, devices in the PIC32MK GP/MC family incorporate an on-chip regulator providing the required core logic voltage from VDD.

33.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

33.3.2 ON-CHIP REGULATOR AND BOR

PIC32MK GP/MC devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **36.1 "DC Characteristics"**.

33.4 On-chip Temperature Sensor

PIC32MK GP/MC devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **36.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

33.5 Programming and Diagnostics

PIC32MK GP/MC devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32MK devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 33-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS

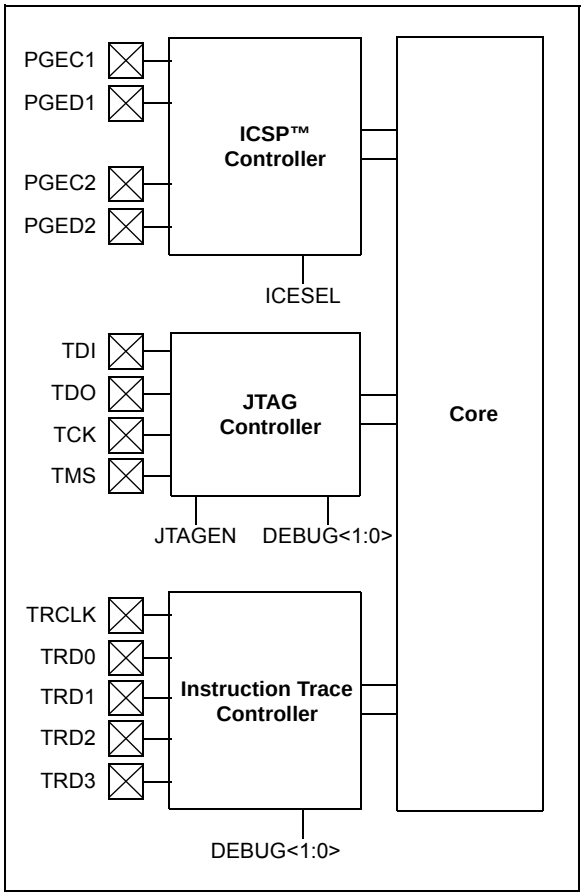
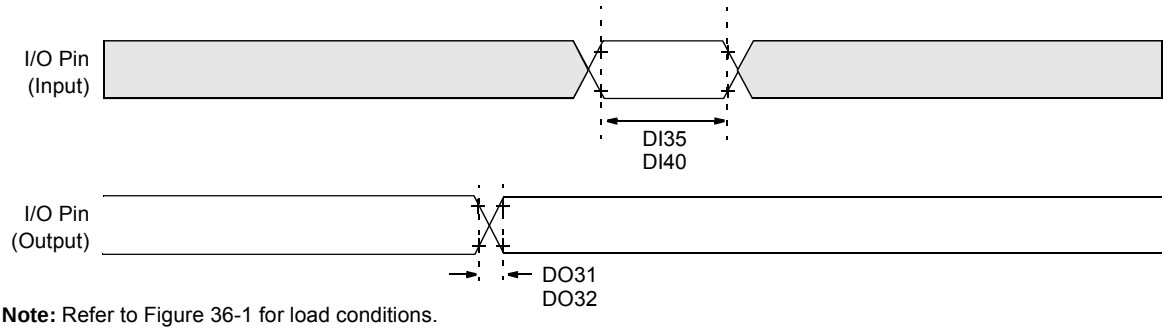


FIGURE 36-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-22: I/O TIMING REQUIREMENTS

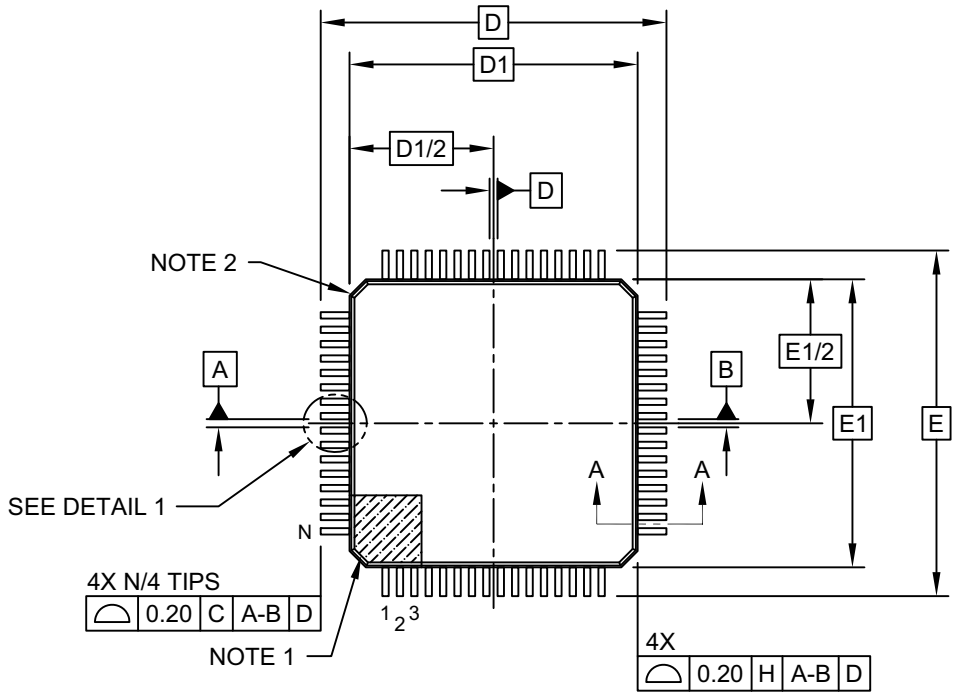
AC CHARACTERISTICS		**Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	**Port Output Rise Time** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15, RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5-RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - Replace 8x Source Driver pins with: RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6-RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

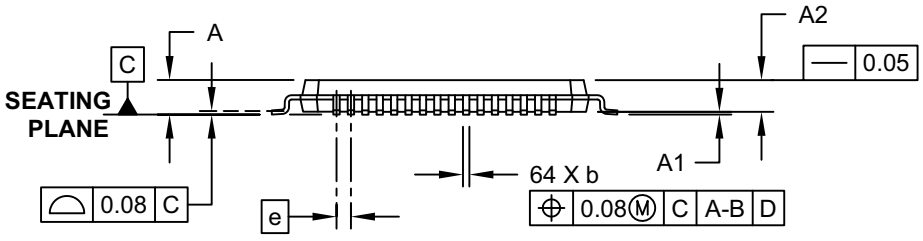
2: This parameter is characterized, but not tested in manufacturing.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

Section Name	Update Description
27.0 "Op Amp/Comparator Module"	The Digital Filter Interconnect Block Diagram was updated (see Figure 27-7). The PSIDL bit was renamed SIDL, and the C5EVT-C1EVT bits were removed in the register summary (see Table 27-2). The bit value '010' definition was updated to from Reserved to PWM Secondary Special Event in the CFSEL<2:0> bits of the Op amp/Comparator 'x' Control Register (see Register 27-2).
28.0 "Charge Time Measurement Unit (CTMU)"	The bit value definitions were updated in the IRNG<1:0> bits of the CTMU Control Register and Notes 5 and 6 were added (see Register 28-1).
32.0 "Power-Saving Features"	The All Resets value in the register summary for bits 15:0 of the PMD2 register was changed to '0000' (see Table 32-2).
36.0 "Electrical Characteristics"	The Maximum value of the Power-Down Current DC Characteristics parameter DC41 was updated (see Table 36-8). The Minimum value of the Internal LPRC Accuracy for parameter F21 was updated (see Table 36-18). The Temperature Sensor Specifications were removed (was Table 36-43). Parameter AD51 in the Analog-to-Digital Conversion Timing Requirements was updated (see Table 36-40). The CTMU Current Source Specification conditions were updated (see Table 36-43).
37.0 "AC and DC Characteristics Graphs"	The Typical CTMU Temperature Sensor Voltage graph was removed (was Figure 37-5).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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