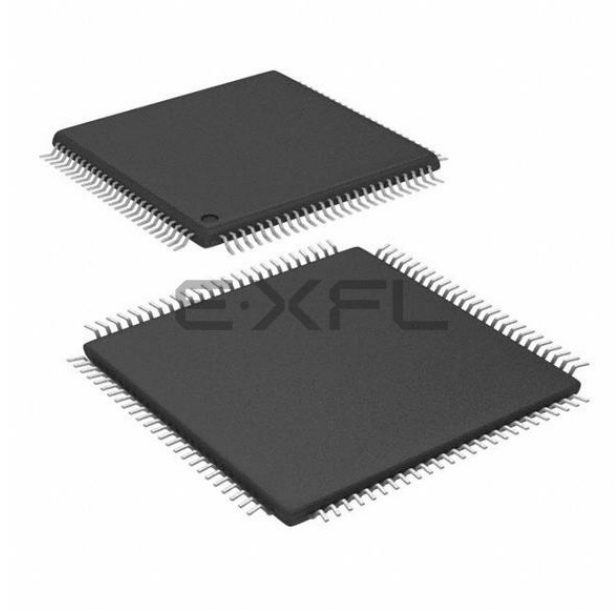
Microchip Technology - PIC32MK1024MCF100T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, IrDA, LINbus, PMP, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, Motor Control PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 42x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mk1024mcf100t-i-pt

3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: The microAptiv™ CPU core resources are available at: www.imgtec.com.

The MIPS32® microAptiv™ MCU Core is the heart of the PIC32MK GP/MC family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

Key features include:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 5):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
  - Virtual memory support
- microMIPS™ compatible instruction set:
  - Improves code size density over MIPS32, while maintaining MIPS32 performance.
  - Supports all MIPS32 instructions (except branch-likely instructions)
  - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
  - Stack pointer implicit in instruction
  - MIPS32 assembly and ABI compatible
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x32 multiply per clock
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - Hardware breakpoint supports both address match and address range triggering.
  - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
  - Real-time instruction program counter
  - Special events trace capability
  - Two performance counters with 34 user-selectable countable events
  - Disabled if the processor enters Debug mode
  - Program Counter sampling
- DSP ASE Extension:
  - Native fractional format data type operations
  - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
  - GPR-based shift
  - Bit manipulation
  - Compare-Pick
  - DSP Control Access
  - Indexed-Load
  - Branch
  - Multiplication of complex operands
  - Variable bit insertion and extraction
  - Virtual circular buffers
  - Arithmetic saturation and overflow handling
  - Zero-cycle overhead saturation and rounding operations
- Floating Point Unit (FPU):
  - 1985 IEEE-754 compliant Floating Point Unit
  - Supports single and double precision datatypes
  - 2008 IEEE-754 compatibility control of NaN handling and Abs/Neg instructions
  - Runs at 1:1 core/FPU clock ratio

TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
PWM3 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM3_VECTOR	175	OFF175<17:1>	IFS5<15>	IEC5<15>	IPC43<28:26>	IPC43<25:24>	Yes
PWM4 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM4_VECTOR	176	OFF176<17:1>	IFS5<16>	IEC5<16>	IPC44<4:2>	IPC44<1:0>	Yes
PWM5 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM5_VECTOR	177	OFF177<17:1>	IFS5<17>	IEC5<17>	IPC44<12:10>	IPC44<9:8>	Yes
PWM6 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM6_VECTOR	178	OFF178<17:1>	IFS5<18>	IEC5<18>	IPC44<20:18>	IPC44<17:16>	Yes
Reserved	—	179	—	—	—	—	—	—
Reserved	—	180	—	—	—	—	—	—
Reserved	—	181	—	—	—	—	—	—
DMA Channel 4	_DMA4_VECTOR	182	OFF182<17:1>	IFS5<22>	IEC5<22>	IPC45<20:18>	IPC45<17:16>	Yes
DMA Channel 5	_DMA5_VECTOR	183	OFF183<17:1>	IFS5<23>	IEC5<23>	IPC45<28:26>	IPC45<25:24>	Yes
DMA Channel 6	_DMA6_VECTOR	184	OFF184<17:1>	IFS5<24>	IEC5<24>	IPC46<4:2>	IPC46<1:0>	Yes
DMA Channel 7	_DMA7_VECTOR	185	OFF185<17:1>	IFS5<25>	IEC5<25>	IPC46<12:10>	IPC46<9:8>	Yes
Data EEPROM Global Interrupt	_DATA_EE_VECTOR	186	OFF186<17:1>	IFS5<26>	IEC5<26>	IPC46<20:18>	IPC46<17:16>	Yes
CAN3 Global Interrupt	_CAN3_VECTOR	187	OFF187<17:1>	IFS5<27>	IEC5<27>	IPC46<28:26>	IPC46<25:24>	Yes
CAN4 Global Interrupt	_CAN4_VECTOR	188	OFF188<17:1>	IFS5<28>	IEC5<28>	IPC47<4:2>	IPC47<1:0>	Yes
QEI3 Interrupt	_QEI2_VECTOR	189	OFF189<17:1>	IFS5<29>	IEC5<29>	IPC47<12:10>	IPC47<9:8>	Yes
QEI4 Interrupt	_QEI3_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
QEI5 Interrupt	_QEI5_VECTOR	191	OFF191<17:1>	IFS5<31>	IEC5<31>	IPC47<28:26>	IPC47<25:24>	Yes
QEI6 Interrupt	_QEI6_VECTOR	192	OFF192<17:1>	IFS6<0>	IEC6<0>	IPC48<4:2>	IPC48<1:0>	Yes
Reserved	—	193	—	—	—	—	—	—
Reserved	—	194	—	—	—	—	—	—
Reserved	—	195	—	—	—	—	—	—
Reserved	—	196	—	—	—	—	—	—
Input Capture 10 Error	_INPUT_CAPTURE_10_ERROR_VECTOR	197	OFF197<17:1>	IFS6<5>	IEC6<5>	IPC49<12:10>	IPC49<9:8>	Yes
Input Capture 10	_INPUT_CAPTURE_10_VECTOR	198	OFF198<17:1>	IFS6<6>	IE6<6>	IPC49<20:18>	IPC49<17:16>	Yes
Output Compare 10	_OUTPUT_COMPARE_10_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
Input Capture 11 Error	_INPUT_CAPTURE_11_ERROR_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
Input Capture 11	_INPUT_CAPTURE_11_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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REGISTER 9-7: PBxDIV: PERIPHERAL BUS 'x' CLOCK DIVISOR CONTROL REGISTER ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	R-1	U-0	U-0	U-0
	ON(1)	—	—	—	PBDIVRDY	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1(2)
	—	PBDIV<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Peripheral Bus 'x' Output Clock Enable bit(1)
- 1 = Output clock is enabled
- 0 = Output clock is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **PBDIVRDY:** Peripheral Bus 'x' Clock Divisor Ready bit
- 1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written
- 0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-7 **Unimplemented:** Read as '0'

bit 6-0 **PBDIV<6:0>:** Peripheral Bus 'x' Clock Divisor Control bits
- 1111111 = PBCLKx is SYSCLK divided by 128
- 1111110 = PBCLKx is SYSCLK divided by 127
- •
- •
- •
- 0000011 = PBCLKx is SYSCLK divided by 4 (default value for x = 6)
- 0000010 = PBCLKx is SYSCLK divided by 3
- 0000001 = PBCLKx is SYSCLK divided by 2 (default value for x < 6)
- 0000000 = PBCLKx is SYSCLK divided by 1 (default value for x = 7)

Note 1: The clock for Peripheral Bus 1 and Peripheral Bus 7 cannot be turned off. Therefore, the ON bit in the PB1DIV register and the PB7DIV register cannot be written as a '0'.

2: The default value for CPU clock PB7DIV Lsb = 0, where PB7CLK = SYSCLK (PB7DIV is read-only).

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

12.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32MK USB OTG module is presented in Figure 12-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32MK USB module includes the following features:

- USB full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, and other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

16.0 DEADMAN TIMER (DMT)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

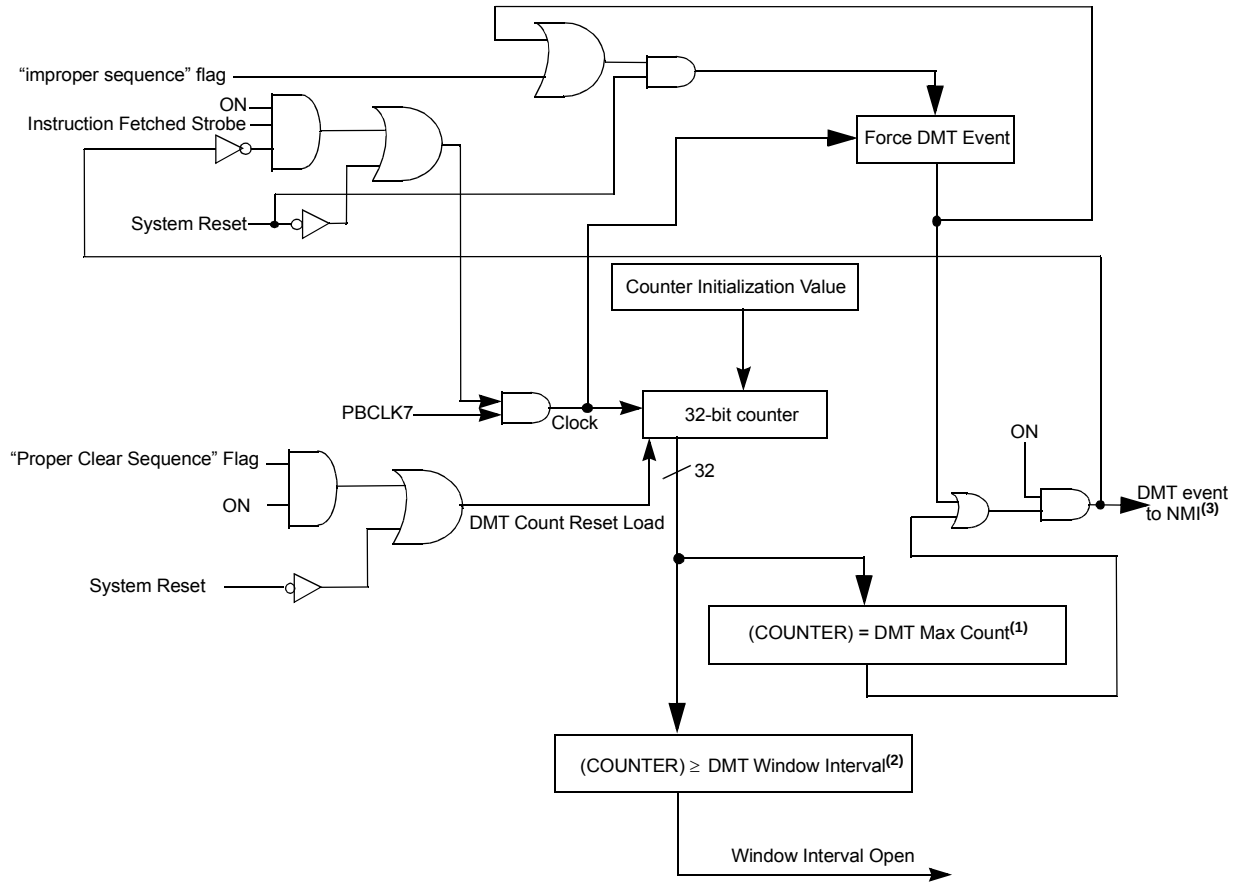
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

The DMT consists of a 32-bit counter with a time-out count match value as specified by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.

A Deadman Timer is typically used in mission critical and safety critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 16-1 shows a block diagram of the Deadman Timer module.

FIGURE 16-1: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.
2: DMT Window Interval is controlled by the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.
3: Refer to **7.0 "Resets"** for more information.

The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register and the C32 bit in the ICxCON register. The available configurations are shown in Table 18-1.

TABLE 18-1: TIMER SOURCE CONFIGURATIONS

ICx	ICACLK (CFGCON<17)>	C32 ICxCON<8>	ICTMR ICxCON<7>	Timerx	Timery	ICxBUF Contents
IC1-IC3	0	0	0	—	TMR3<15:0>	TMR3<15:0>
			1	TMR2<15:0>	—	TMR2<15:0>
	0	1	x	TMR2<31:0>	TMR2<31:0>	TMR2<31:0>
	1	0	0	—	TMR5<15:0>	TMR5<15:0>
			1	TMR4<15:0>	—	TMR4<15:0>
	1	1	x	TMR4<31:0>	TMR4<31:0>	TMR4<31:0>
IC4-IC6, IC13-IC16	0	0	0	—	TMR3<15:0>	TMR3<15:0>
			1	TMR2<15:0>	—	TMR2<15:0>
	0	1	x	TMR2<31:0>	TMR2<31:0>	TMR2<31:0>
	1	0	0	—	TMR3<15:0>	TMR3<15:0>
			1	TMR2<15:0>	—	TMR2<15:0>
	1	1	x	TMR2<31:0>	TMR2<31:0>	TMR2<31:0>
IC7-IC9	0	0	0	—	TMR3<15:0>	TMR3<15:0>
			1	TMR2<15:0>	—	TMR2<15:0>
	0	1	x	TMR2<31:0>	TMR2<31:0>	TMR2 <31:0>
	1	0	0	—	TMR7<15:0>	TMR7<15:0>
			1	TMR6<15:0>	—	TMR6<15:0>
	1	1	x	TMR6<31:0>	TMR6<31:0>	TMR6<31:0>
IC10-IC12	0	0	0	—	TMR3<15:0>	TMR3<15:0>
			1	TMR2 <15:0>	—	TMR2<15:0>
	0	1	x	TMR2 <31:0>	TMR2<31:0>	TMR2<31:0>
	1	0	0	—	TMR9<15:0>	TMR9<15:0>
			1	TMR8<15:0>	—	TMR8<15:0>
	1	1	x	TMR8<31:0>	TMR8<31:0>	TMR8 <31:0>

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REGISTER 23-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Hardware Set	SC = Software Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7D10	ADC1CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D20	ADC2CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D30	ADC3CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D40	ADC4CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D50	ADC5CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D70	ADC7CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., V_{BAT}, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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REGISTER 25-10: ADCGIRQEN2: ADC GLOBAL INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	AGIEN53	AGIEN52	AGIEN51	AGIEN50	AGIEN49	AGIEN48
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	AGIEN47(1)	AGIEN46(1)	AGIEN45(1)	—	—	—	AGIEN41(1)	AGIEN40(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	AGIEN39(1)	AGIEN38(1)	AGIEN37(1)	AGIEN36(1)	AGIEN35(1)	AGIEN34(1)	AGIEN33(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-13 **AGIEN53:AGIEN45** ADC Global Interrupt Enable bits

1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT2 register)

0 = Interrupts are disabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9-1 **AGIEN41:AGIEN33** ADC Global Interrupt Enable bits

1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT2 register)

0 = Interrupts are disabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

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REGISTER 25-25: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<15:8>							
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<7:0>							
15:8	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AINID<5:0>					
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CVDDATA<15:0>:** CVD Data Status bits
In CVD mode, these bits obtain the CVD differential output data (subtraction of CVD positive and negative measurement), whenever a Digital Comparator interrupt is generated. The value in these bits is compliant with the FRACT bit (ADCCON1<23>) and is always signed.

bit 15-14 **Unimplemented:** Read as '0'

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REGISTER 25-33: ADCxTIME: DEDICATED HIGH-SPEED ADCx TIMING REGISTER (CONTINUED) ('x' = 0 THROUGH 5)

bit 9-0 **SAMC<9:0>:** ADCx Sample Time bits

Where TADx = period of the ADC conversion clock for the dedicated ADC controlled by the ADCDIV<6:0> bits.

1111111111 = 1025 TADx
.
.
.
0000000001 = 3 TADx
0000000000 = 2 TADx

Note: The SAMC sample time is always enforced regardless even if the conversion trigger occurs before SAMC expiration. The conversion trigger event is persistent and will be acknowledged and start the conversion if true, immediately after the SAMC period. ADC0-ADC5 will remain indefinitely in the sample state even after the expiration of SAMC until the trigger event, which will end sampling and start conversion, except when either of the following are true:

- The ADC filter is enabled and the DFMODE bit in the ADCFLTRx register = 0
- The TRGSRC3 bit in the ADCTRG1 register = Global level software trigger

27.2 Comparator Interface

The Comparators also have both their inverting and non-inverting inputs accessible via device pins. The non-inverting input pins can be connected to an internal 12-bit CDAC to generate a precise reference or to an external reference through a pin. These references can be individually selected for each comparator module. The inverting inputs can be connected to one of four external pins or internally to outputs of the Op amps. The Comparator outputs can be entirely disabled from appearing on the output pins, which relieves a pin for other uses, remapped to different pins via the peripheral pin select module, and selected to active-high or active-low polarity.

In Comparator modules that do not implement the Op amp, the Comparator module has a different input selection configuration.

The stand-alone Comparator implements a 4 x 1 multiplexer at the inverting input to enable selection of the desired signal to compare against the non-inverting input. Up to three outputs of Op amps can be internally connected to the Comparator via the multiplexer.

The Comparator may be enabled or disabled using the corresponding ON bit (CMxCON<15>) in the Op amp/ Comparator Control register. When the Comparator is disabled, the corresponding trigger and interrupt generation is disabled as well.

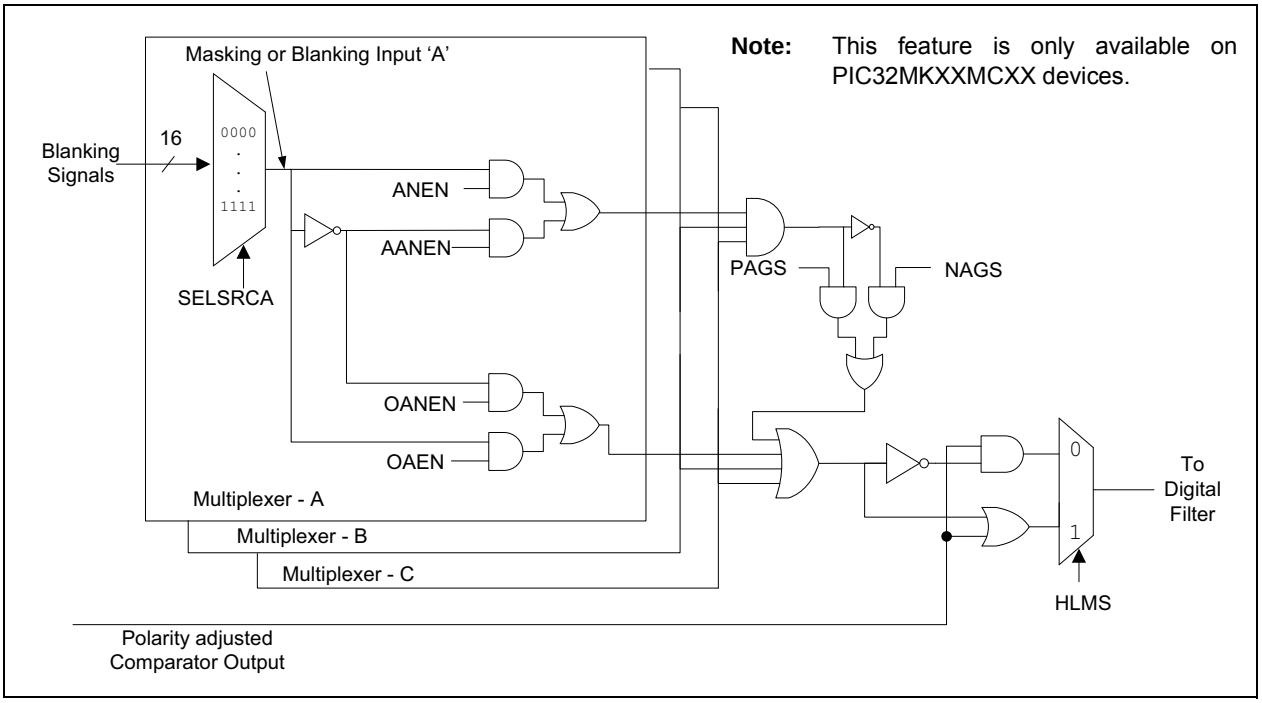
It is recommended to first configure the CMxCON register with all bits to the desired value, and then set the ON bit. When not used, the Comparator should be disabled expressly by writing a '0' to the ON bit.

27.3 Comparator Output Blanking

Comparator output blanking is a feature that is only available on PIC32MK Motor Control (i.e., PIC32MKXXMCXX) devices. The outputs of the Comparators can be further blanked/masked based on external events for programmable durations. This feature can be very useful in reducing the interrupt or trigger frequencies. It is primarily used to select Comparator events (interrupts and triggers) synchronized to desired edge transitions on external digital signals such as the PWM outputs from the MCPWM module. A prudent choice of these external signals has potential to greatly simplify software where otherwise extra software logic will be needed to arbitrate for the desired event source. Refer to the Comparator Mask Control Register, CMxMSKCON (Register 27-3), for details on the 16 different external signals that can be used for masking.

The logic AND, logic OR and multiplexer blocks shown in Figure 27-6 can be visualized as built-in programmable array logic used to reject the unwanted transitions of the comparator output. For each Comparator, the multiplexers A, B, and C can logically AND or OR either the positive or negative levels (edges) of the 16 different external signals. The outputs of the multiplexers can then be ANDed or ORed together with the AND logic outputs of the multiplexers being further capable of selection for positive or negative transitions as shown in the diagram. For a detailed usage of the output blanking feature, refer to **Section 39. "Op Amp/Comparator"** (DS60001178) of the *"PIC32 Family reference Manual"*.

FIGURE 27-6: USER PROGRAMMABLE BLANKING FUNCTION DIAGRAM



Note: This feature is only available on PIC32MKXXMCXX devices.

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REGISTER 27-3: CMxMSKCON: COMPARATOR 'x' MASK CONTROL REGISTER ('x' = 1-5) (CONTINUED)

bit 12 **OCNEN:** OR Gate "C" Input Inverted Enable bit
1 = "C" input (inverted) enabled as input to OR gate
0 = "C" input (inverted) disabled as input to OR gate

bit 11 **OBEN:** OR Gate "B" Input Enable bit
1 = "B" input enabled as input to OR gate
0 = "B" input disabled as input to OR gate

bit 10 **OBNEN:** OR Gate "B" Input Inverted Enable bit
1 = "B" input (inverted) enabled as input to OR gate
0 = "B" input (inverted) disabled as input to OR gate

bit 9 **OAEN:** OR Gate "A" Input Enable bit
1 = "A" input enabled as input to OR gate
0 = "A" input disabled as input to OR gate

bit 8 **OANEN:** OR Gate "A" Input Inverted Enable bit
1 = "A" input (inverted) enabled as input to OR gate
0 = "A" input (inverted) disabled as input to OR gate

bit 7 **NAGS:** Negative AND Gate Output Select bit
1 = The negative (inverted) output of the AND gate to the OR gate is enabled
0 = The negative (inverted) output of the AND gate to the OR gate is disabled

bit 6 **PAGS:** Positive AND Gate Output Select bit
1 = The positive output of the AND gate to the OR gate is enabled
0 = The positive output of the AND gate to the OR gate is disabled

bit 5 **ACEN:** AND Gate "C" Input Enable bit
1 = "C" input enabled as input to AND gate
0 = "C" input disabled as input to AND gate

bit 4 **ACNEN:** AND Gate "C" Inverted Input Enable bit
1 = "C" input (inverted) enabled as input to AND gate
0 = "C" input (inverted) disabled as input to AND gate

bit 3 **ABEN:** AND Gate "B" Input Enable bit
1 = "B" input enabled as input to AND gate
0 = "B" input disabled as input to AND gate

bit 2 **ABNEN:** AND Gate "B" Inverted Input Enable bit
1 = "B" input (inverted) enabled as input to AND gate
0 = "B" input (inverted) disabled as input to AND gate

bit 1 **AAEN:** AND Gate "A" Input Enable bit
1 = "A" input enabled as input to AND gate
0 = "A" input disabled as input to AND gate

bit 0 **AANEN:** AND Gate "A" Inverted Input Enable bit
1 = "A" input (inverted) enabled as input to AND gate
0 = "A" input (inverted) disabled as input to AND gate

Note: This register is only available on PIC32MKXXMCXXX devices.

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REGISTER 31-11: PWMCONx: PWM CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FLTIF(1)	CLIF(1)	TRGIF(1)	PWMLIF(1)	PWM-HIF(1)	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—
15:8	HS/HC-0	HS/HC-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>(1)		ITB(2)	—
7:0	R/W-0	R/W-0	R/W-0	HS/HC/R-0	R/W-0	U-0	R/W-0	U-0
	DTC<1:0>		DTCP(4)	PTDIR(6)	MTBS(7)	—	XPRES(3)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTIF:** Fault Interrupt Flag bit(1)
- 1 = Fault interrupt has occurred
- 0 = Fault interrupt has not occurred

bit 30 **CLIF:** Current-Limit Status bit(1)
- 1 = Current limit has occurred
- 0 = Current limit has not occurred

bit 29 **TRGIF:** Trigger Interrupt Status bit(1)
- 1 = Trigger interrupt is pending
- 0 = Trigger interrupt is not pending

bit 28 **PWMLIF:** PWML Interrupt Status bit(1)
- 1 = PWM Timer equal to 0x0 interrupt has occurred
- 0 = PWM Interrupt has not occurred

bit 27 **PWMHIF:** PWMH Interrupt Status bit
- 1 = PWM period match interrupt has occurred
- 0 = PWM period match interrupt has not occurred

bit 26-24 **Unimplemented:** Read as '0'

bit 23 **FLTIEN:** Fault Interrupt Enable bit
- 1 = Fault interrupt is enabled. If FLTIF = 1, an interrupt event will be generated.
- 0 = Fault interrupt is disabled

bit 22 **CLIEN:** Current-Limit Interrupt Enable bit
- 1 = Current-limit interrupt is enabled. If CLIF = 1, an interrupt event will be generated.
- 0 = Current-limit interrupt is disabled

Note 1: If PWM interrupts are enabled, software must clear the PWMCONx interrupt flags here first, followed second by the corresponding IFSx bit in the Interrupt controller. The corresponding PWM IFSx interrupt flag cannot be cleared if any of these local PWMCON interrupt bits are not cleared first. Failure to do so will result in an infinite interrupt loop.

2: This bit should not be changed after the PWM is enabled (PTEN bit (PTCON<15>) = 1).

3: To operate in External Period Reset mode, the ITB bit must be set to '1' and the CLMOD bit in the IOCONx register must be set to '0'.

4: For Dead Time Compensation (DTCP) to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.

5: Negative dead time is only implemented for Edge-Aligned mode.

6: XPRES mode should only be used in Edge-Aligned mode with or without complimentary outputs. It does not support dead time compensation (i.e., duty cycle adjustment), which is selected when DTC<1:0> = 11.

7: The clock source is one of the master time bases even if ITB = 1 is selected.

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REGISTER 31-11: PWMCONx: PWM CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 5 **DTCP:** Dead Time Compensation Polarity bit(5)
- 1 = If the DTCMPx pin = 0, PWMxL is shortened, and PWMxH is lengthened
  If the DTCMPx pin = 1, PWMxH is shortened, and PWMxL is lengthened
- 0 = If the DTCMPx pin = 0, PWMxH is shortened, and PWMxL is lengthened
  If the DTCMPx pin = 1, PWMxL is shortened, and PWMxH is lengthened

bit 4 **PTDIR:** PWM Timer Direction bit(6)
- 1 = PWM timer is decrementing
- 0 = PWM timer is incrementing

bit 3 **MTBS:** Master Time Base Select bit(7)
- 1 = Secondary master time base is the clock source for the MCPWM module
- 0 = Primary master time base is the clock source for the MCPWM module

bit 2 **Unimplemented:** Read as '0'

bit 1 **XPRES:** External PWM Reset Control bit(3)
- 1 = Current-limit source resets primary local time base for this PWM generator if it is in Independent Time Base mode and the PWM module enters the deassertion portion of the duty cycle
- 0 = External pins do not affect PWM time base

Note: If the Current-Limit Reset signal is asserted during the active assertion time of the duty cycle, the time base will not Reset until two PWM clock cycles after the duty cycle transition from assertion to deassertion phase of the duty cycle.

bit 0 **Unimplemented:** Read as '0'

Note 1: If PWM interrupts are enabled, software must clear the PWMCONx interrupt flags here first, followed second by the corresponding IFSx bit in the Interrupt controller. The corresponding PWM IFSx interrupt flag cannot be cleared if any of these local PWMCON interrupt bits are not cleared first. Failure to do so will result in an infinite interrupt loop.

2: This bit should not be changed after the PWM is enabled (PTEN bit (PTCON<15>) = 1).

3: To operate in External Period Reset mode, the ITB bit must be set to '1' and the CLMOD bit in the IOCONx register must be set to '0'.

4: For Dead Time Compensation (DTCP) to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.

5: Negative dead time is only implemented for Edge-Aligned mode.

6: XPRES mode should only be used in Edge-Aligned mode with or without complimentary outputs. It does not support dead time compensation (i.e., duty cycle adjustment), which is selected when DTC<1:0> = 11.

7: The clock source is one of the master time bases even if ITB = 1 is selected.

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REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 22-19 **FLTSRC<3:0>:** Fault Control Signal Source Select bits for PWM Generator 'x'(2,4)
These bits specify the Fault control source.
1111 = FLT15
1110 = Reserved
1101 = Reserved
1100 = Comparator 5
1011 = Comparator 4
1010 = Comparator 3
1001 = Comparator 2
1000 = Comparator 1
0111 = FLT8
0110 = FLT7
0101 = FLT6
0100 = FLT5
0011 = FLT4
0010 = FLT3
0001 = FLT2
0000 = FLT1

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```


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32.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 32-2 for more information.

Note:	Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

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33.2 Registers

TABLE 33-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3FC0	DEVCFG3	31:16	FVBUSIO1	FUSBIDIO1	IOL1WAY	PMDL1WAY	PGL1WAY	—	—	—	FVBUSIO2	FUSBIDIO2	—	PWMLOCK	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
3FC4	DEVCFG2	31:16	UPLLEN	—	BORSEL	FDSEN	DSWDTEN	DSWDT OSC	DSWDTPS<4:0>					DSBOREN	VBAT BOREN	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
3FC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
3FCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	—	—	—	—	—	—	POSC BOOST	POSCGAIN<1:0>		SOSC BOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	—	—	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
3FDC	DEVCP	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
3FEC	DEVSIGN	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 33-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	ADCPRI	—	—	PWMAPIN6	PWMAPIN5	PWMAPIN4	PWMAPIN3	PWMAPIN2	PWMAPIN1	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	—	IOANCPEN	—	—	—	JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00E0	CFGPG	31:16	—	—	—	—	—	—	ADCPG<1:0>		FCPG<1:0>		—	—	CAN4PG<1:0>		CAN3PG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		USB2PG<1:0>		USB1PG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000
0110	CFGCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	ENPGA5	—	ENPGA3	ENPGA2	ENPGA1	0000
		15:0	—	—	—	—	—	—	—	—	EEWS<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the specific device.

3: This register is not available on 64-pin devices.

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35.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

35.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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FIGURE 36-18: PARALLEL MASTER PORT READ TIMING DIAGRAM

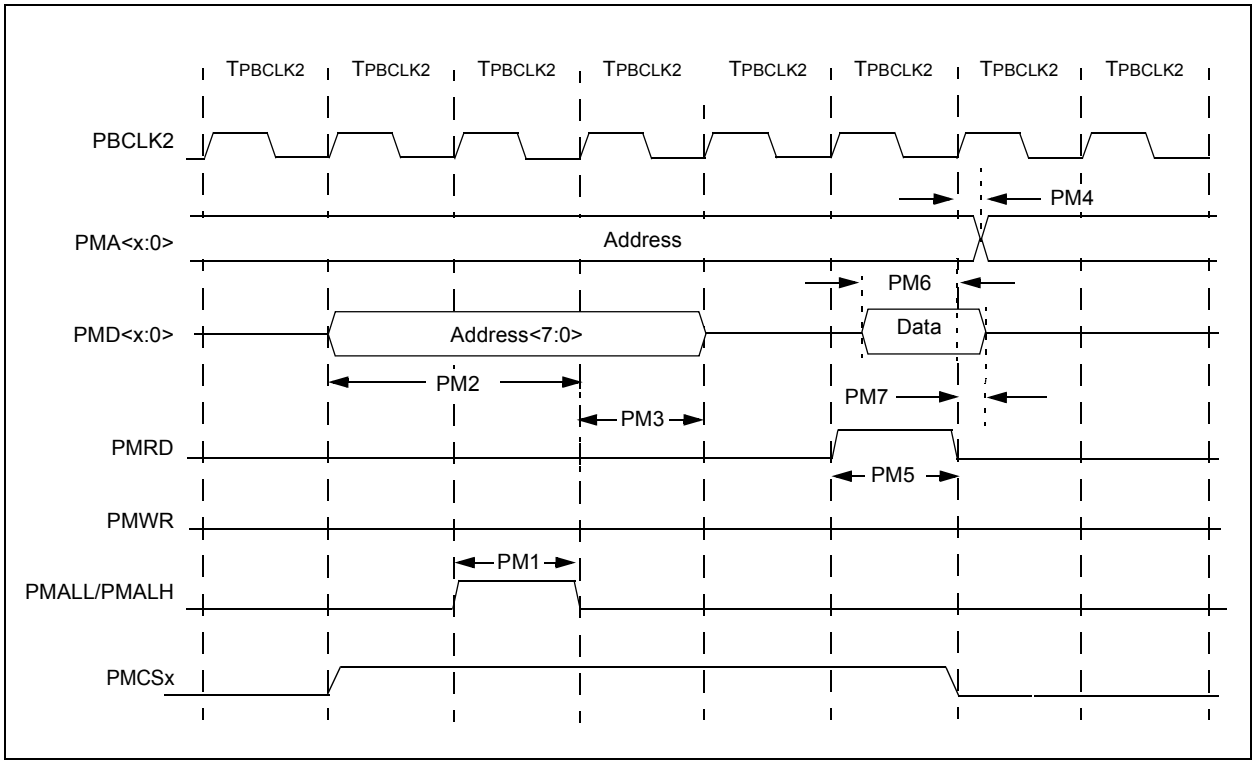

TABLE 36-45: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPBCLK2	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPBCLK2	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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