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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08dv32clh

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	6/2006	Advance Information version for alpha samples customers
2	9/2007	Product Launch. Removed the 64-pin QFN package. Changed from standard to extended mode for MSCAN registers in register summary. Corrected Block diagrams for SCI. Updated the latest Temp Sensor information. Made FTSTMOD reserved. Updated device to use the ADC 12-bit module. Revised the MCG module. Updated the TPM block module to version 3. Added the TPM block module version 2 as an appendix for devices using 3M05C (or earlier) mask sets. Heavily revised the Electricals appendix.
3	6/2008	Sustaining Update. Incorporated PS Issues # 2765, 3177, 3236, 3292, 3301, 3311, 3312, 3326, 3335, 3345, 3382, 2795, 3382 and 3386 PLL Jitter Spec update. Also, added internal reference clock trim adjustment statement to Features page. Updated the TPM module to the latest version. Adjusted values in Table A-13 Control Timing row 2 and in Table A-6 DC Characteristics row 24 so that it references 5.0 V instead of 3.0 V.

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Chapter 14
Serial Communications Interface (S08SCIV4)

Chapter 15
Real-Time Counter (S08RTCV1)

3.6 Stop Modes

One of two stop modes is entered upon execution of a STOP instruction when the STOPE bit in SOPT1 register is set. In both stop modes, all internal clocks are halted. The MCG module can be configured to leave the reference clocks running. See Chapter 8, “Multi-Purpose Clock Generator (S08MCGV1),” for more information.

Table 3-1 shows all of the control bits that affect stop mode selection and the mode selected under various conditions. The selected mode is entered following the execution of a STOP instruction.

Table 3-1. Stop Mode Selection

STOPE	ENBDM [1]	LVDE	LVDSE	PPDC	Stop Mode
0	x	x		x	Stop modes disabled; illegal opcode reset if STOP instruction executed
1	1	x		x	Stop3 with BDM enabled [2]
1	0	Both bits must be 1		x	Stop3 with voltage regulator active
1	0	Either bit a 0		0	Stop3
1	0	Either bit a 0		1	Stop2

1 ENBDM is located in the BDCSCR, which is only accessible through BDC commands, see Section 17.4.1.1, “BDC Status and Control Register (BDCSCR)”.

2 When in Stop3 mode with BDM enabled, The S_{IDD} will be near R_{IDD} levels because internal clocks are enabled.

3.6.1 Stop3 Mode

Stop3 mode is entered by executing a STOP instruction under the conditions as shown in Table 3-1. The states of all of the internal registers and logic, RAM contents, and I/O pin states are maintained.

Exit from stop3 is done by asserting $\overline{\text{RESET}}$ or an asynchronous interrupt pin. The asynchronous interrupt pins are IRQ, PIA0–PIA7, PIB0–PIB7, and PID0–PID7. Exit from stop3 can also be done by the low-voltage detect (LVD) reset, low-voltage warning (LVW) interrupt, ADC conversion complete interrupt, real-time clock (RTC) interrupt, MSCAN wake-up interrupt, or SCI receiver interrupt.

If stop3 is exited by means of the $\overline{\text{RESET}}$ pin, the MCU will be reset and operation will resume after fetching the reset vector. Exit by means of an interrupt will result in the MCU fetching the appropriate interrupt vector.

3.6.1.1 LVD Enabled in Stop3 Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode.

For the ADC to operate the LVD must be left enabled when entering stop3.

4.5.5 Sector Erase Abort

The sector erase abort operation will terminate the active sector erase operation so that other sectors are available for read and program operations without waiting for the sector erase operation to complete.

The sector erase abort command write sequence is as follows:

1. Write to any Flash address to start the command write sequence for the sector erase abort command. The address and data written are ignored.
2. Write the sector erase abort command, 0x47, to the FCMD register.
3. Clear the FCBEF flag in the FSTAT register by writing a 1 to FCBEF to launch the sector erase abort command.

If the sector erase abort command is launched resulting in the early termination of an active sector erase operation, the FACCERR flag will set once the operation completes as indicated by the FCCF flag being set. The FACCERR flag sets to inform the user that the Flash sector may not be fully erased and a new sector erase command must be launched before programming any location in that specific sector.

If the sector erase abort command is launched but the active sector erase operation completes normally, the FACCERR flag will not set upon completion of the operation as indicated by the FCCF flag being set. Therefore, if the FACCERR flag is not set after the sector erase abort command has completed, a sector being erased when the abort command was launched will be fully erased.

A flowchart to execute the sector erase abort operation is shown in Figure 4-4.

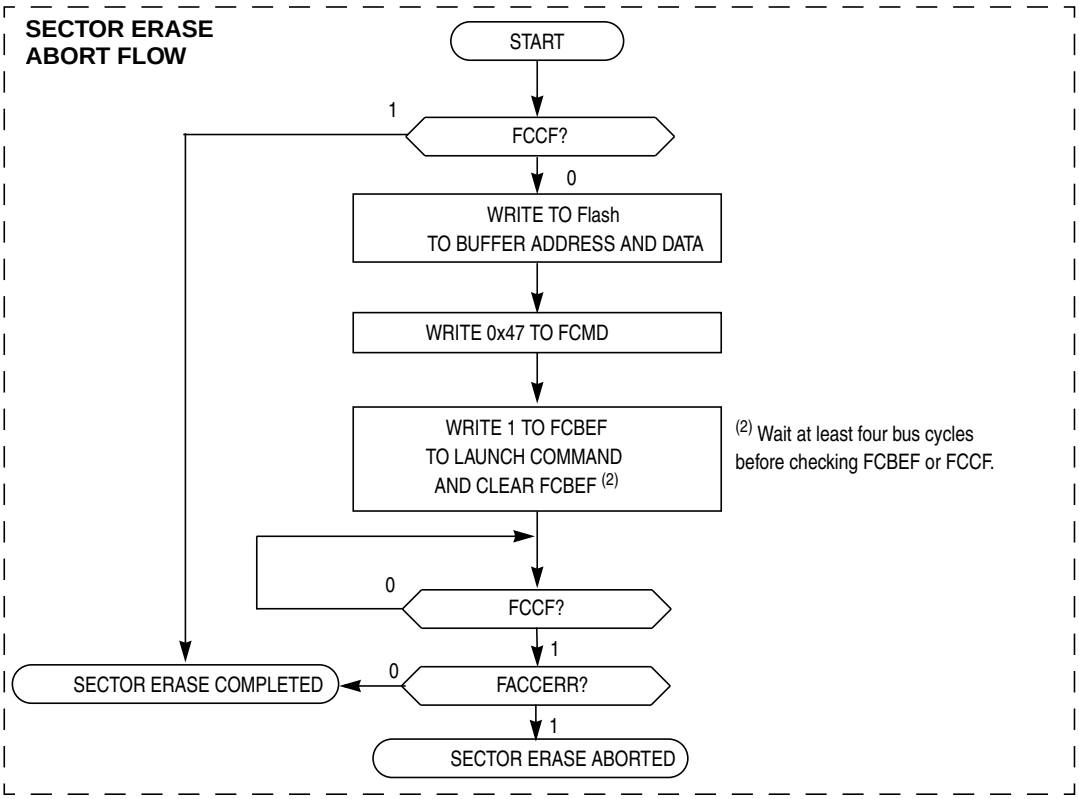

Figure 4-4. Sector Erase Abort Flowchart

4.5.7 Block Protection

The block protection feature prevents the protected region of Flash from program or erase changes. Block protection is controlled through the Flash protection register (FPROT). The FPS bits determine the protected region of Flash. See Section 4.5.10.4, “Flash Protection Register (FPROT and NVPROT).”

After exit from reset, FPROT is loaded with the contents of the NVPROT location, which is in the nonvolatile register block of the Flash memory. Any FPROT write that attempts to decrease the size of the protected region will be ignored. Because NVPROT is within the last sector of Flash, if any amount of memory is protected, NVPROT is itself protected and cannot be unprotected (intentionally or unintentionally) by the application software. FPROT can be written through background debug commands, which provides a way to erase and reprogram protected Flash memory.

One use for block protection is to block protect an area of Flash memory for a bootloader program. this bootloader program can call a routine outside of Flash that can be used to sector erase the rest of the Flash memory and reprogram it. The bootloader is protected even if MCU power is lost during an erase and reprogram operation.

4.5.8 Vector Redirection

While any Flash is block protected, the reset and interrupt vectors will be protected. Vector redirection allows users to modify interrupt vector information without unprotecting bootloader and reset vector space. Vector redirection is enabled by programming the FNORED bit in the NVOPT register located at address 0xFFBF to 0. For redirection to occur, at least some portion of the Flash memory must be block protected by programming the NVPROT register located at address 0xFFBD. All interrupt vectors (memory locations 0xFFC0–0xFFFD) are redirected, though the reset vector (0xFFFE:0xFFFF) is not.

For example, if 1536 bytes of Flash are protected, the protected address region is from 0xFA00 through 0xFFFF. The interrupt vectors (0xFFC0–0xFFFD) are redirected to the locations 0xF9C0–0xF9FD. If vector redirection is enabled and an interrupt occurs, the values in the locations 0xF9E0:0xF9E1 are used for the vector instead of the values in the locations 0xFFE0:0xFFE1. This allows the user to reprogram the unprotected portion of the Flash with new program code including new interrupt vector values while leaving the protected area, which includes the default vector locations, unchanged.

4.5.9 Security

The MC9S08DV60 Series includes circuitry to prevent unauthorized access to the contents of Flash and RAM memory. When security is engaged, Flash and RAM are considered secure resources. Direct-page registers, high-page registers, and the background debug controller are considered unsecured resources. Programs executing within secure memory have normal access to any MCU memory locations and resources. Attempts to access a secure memory location with a program executing from an unsecured memory space or through the background debug interface are blocked (writes are ignored and reads return all 0s).

Security is engaged or disengaged based on the state of two register bits (SEC[1:0]) in the FOPT register. During reset, the contents of the nonvolatile location NVOPT are copied from Flash into the working FOPT register in high-page register space. A user engages security by programming the NVOPT location, which can be performed at the same time the Flash memory is programmed. The 1:0 state disengages

Table 5-1. Vector Summary[1]

Vector No.	Address (High/Low)	Vector Name	Module	Source	Enable	Description
31	0xFFC0/0xFFC1	Vacmp2	ACMP2	ACF	ACIE	Analog comparator 2
30	0xFFC2/0xFFC3	Vacmp1	ACMP1	ACF	ACIE	Analog comparator 1
29	0xFFC4/0xFFC5	Vcantx	MSCAN	TXE[2:0]	TXEIE[2:0]	CAN transmit
28	0xFFC6/0xFFC7	Vcanrx	MSCAN	RXF	RXFIE	CAN receive
27	0xFFC8/0xFFC9	Vcanerr	MSCAN	CSCIF, OVRIF	CSCIE, OVRIE	CAN errors
26	0xFFCA/0xFFCB	Vcanwu	MSCAN	WUPIF	WUPIE	CAN wake-up
25	0xFFCC/0xFFCD	Vrtc	RTC	RTIF	RTIE	Real-time interrupt
24	0xFFCE/0xFFCF	Viic	IIC	IICIS	IICIE	IIC control
23	0xFFD0/0xFFD1	Vadc	ADC	COCO	AIEN	ADC
22	0xFFD2/0xFFD3	Vport	Port A,B,D	PTAIF, PTBIF, PTDIF	PTAIE, PTBIE, PTDIE	Port Pins
21	0xFFD4/0xFFD5	Vsci2tx	SCI2	TDRE, TC	TIE, TCIE	SCI2 transmit
20	0xFFD6/0xFFD7	Vsci2rx	SCI2	IDLE, LBKDIF, RDRF, RXEDGIF	ILIE, LBKDIE, RIE, RXEDGIE	SCI2 receive
19	0xFFD8/0xFFD9	Vsci2err	SCI2	OR, NF FE, PF	ORIE, NFIE, FEIE, PFIE	SCI2 error
18	0xFFDA/0xFFDB	Vsci1tx	SCI1	TDRE, TC	TIE, TCIE	SCI1 transmit
17	0xFFDC/0xFFDD	Vsci1rx	SCI1	IDLE, LBKDIF, RDRF, RXEDGIF	ILIE, LBKDIE, RIE, RXEDGIE	SCI1 receive
16	0xFFDE/0xFFDF	Vsci1err	SCI1	OR, NF, FE, PF	ORIE, NFIE, FEIE, PFIE	SCI1 error
15	0xFFE0/0xFFE1	Vspi	SPI	SPIF, MODF, SPTEF	SPIE, SPIE, SPTIE	SPI
14	0xFFE2/0xFFE3	Vtpm2ovf	TPM2	TOF	TOIE	TPM2 overflow
13	0xFFE4/0xFFE5	Vtpm2ch1	TPM2	CH1F	CH1IE	TPM2 channel 1
12	0xFFE6/0xFFE7	Vtpm2ch0	TPM2	CH0F	CH0IE	TPM2 channel 0
11	0xFFE8/0xFFE9	Vtpm1ovf	TPM1	TOF	TOIE	TPM1 overflow
10	0xFFEA/0xFFEB	Vtpm1ch5	TPM1	CH5F	CH5IE	TPM1 channel 5
9	0xFFEC/0xFFED	Vtpm1ch4	TPM1	CH4F	CH4IE	TPM1 channel 4
8	0xFFEE/0xFFEF	Vtpm1ch3	TPM1	CH3F	CH3IE	TPM1 channel 3
7	0xFFF0/0xFFF1	Vtpm1ch2	TPM1	CH2F	CH2IE	TPM1 channel 2
6	0xFFF2/0xFFF3	Vtpm1ch1	TPM1	CH1F	CH1IE	TPM1 channel 1
5	0xFFF4/0xFFF5	Vtpm1ch0	TPM1	CH0F	CH0IE	TPM1 channel 0
4	0xFFF6/0xFFF7	Vlol	MCG	LOLS	LOLIE	MCG loss of lock
3	0xFFF8/0xFFF9	Vlvd	System control	LVWF	LVWIE	Low-voltage warning
2	0xFFFA/0xFFFB	Virq	IRQ	IRQF	IRQIE	IRQ pin
1	0xFFFC/0xFFFD	Vswi	Core	SWI Instruction	—	Software interrupt
0	0xFFFE/0xFFFF	Vreset	System control	COP, LOC, LVD, $\overline{\text{RESET}}$, ILOP, ILAD, POR, BDFR	COPE CME LVDRE — — — — —	Watchdog timer Loss-of-clock Low-voltage detect External pin Illegal opcode Illegal address Power-on-reset BDM-forced reset

1 Vector priority is shown from lowest (first row) to highest (last row). For example, Vreset is the highest priority vector.

6.5.4.3 Port D Pull Enable Register (PTDPE)

	7	6	5	4	3	2	1	0
R W	PTDPE7	PTDPE6	PTDPE5	PTDPE4	PTDPE3	PTDPE2	PTDPE1	PTDPE0
Reset:	0	0	0	0	0	0	0	0

Figure 6-26. Internal Pull Enable for Port D Register (PTDPE)

Table 6-24. PTDPE Register Field Descriptions

Field	Description
7:0 PTDPE[7:0]	**Internal Pull Enable for Port D Bits** — Each of these control bits determines if the internal pull-up or pull-down device is enabled for the associated PTD pin. For port D pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled. 0 Internal pull-up/pull-down device disabled for port D bit n. 1 Internal pull-up/pull-down device enabled for port D bit n.

NOTE

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured.

6.5.4.4 Port D Slew Rate Enable Register (PTDSE)

	7	6	5	4	3	2	1	0
R W	PTDSE7	PTDSE6	PTDSE5	PTDSE4	PTDSE3	PTDSE2	PTDSE1	PTDSE0
Reset:	0	0	0	0	0	0	0	0

Figure 6-27. Slew Rate Enable for Port D Register (PTDSE)

Table 6-25. PTDSE Register Field Descriptions

Field	Description
7:0 PTDSE[7:0]	**Output Slew Rate Enable for Port D Bits** — Each of these control bits determines if the output slew rate control is enabled for the associated PTD pin. For port D pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port D bit n. 1 Output slew rate control enabled for port D bit n.

Note: Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.

7.3.6.7 SP-Relative, 16-Bit Offset (SP2)

This variation of indexed addressing uses the 16-bit value in the stack pointer (SP) plus a 16-bit offset included in the instruction as the address of the operand needed to complete the instruction.

7.4 Special Operations

The CPU performs a few special operations that are similar to instructions but do not have opcodes like other CPU instructions. In addition, a few instructions such as STOP and WAIT directly affect other MCU circuitry. This section provides additional information about these operations.

7.4.1 Reset Sequence

Reset can be caused by a power-on-reset (POR) event, internal conditions such as the COP (computer operating properly) watchdog, or by assertion of an external active-low reset pin. When a reset event occurs, the CPU immediately stops whatever it is doing (the MCU does not wait for an instruction boundary before responding to a reset event). For a more detailed discussion about how the MCU recognizes resets and determines the source, refer to the Resets, Interrupts, and System Configuration chapter.

The reset event is considered concluded when the sequence to determine whether the reset came from an internal source is done and when the reset pin is no longer asserted. At the conclusion of a reset event, the CPU performs a 6-cycle sequence to fetch the reset vector from 0xFFFE and 0xFFFF and to fill the instruction queue in preparation for execution of the first program instruction.

7.4.2 Interrupt Sequence

When an interrupt is requested, the CPU completes the current instruction before responding to the interrupt. At this point, the program counter is pointing at the start of the next instruction, which is where the CPU should return after servicing the interrupt. The CPU responds to an interrupt by performing the same sequence of operations as for a software interrupt (SWI) instruction, except the address used for the vector fetch is determined by the highest priority interrupt that is pending when the interrupt sequence started.

The CPU sequence for an interrupt is:

1. Store the contents of PCL, PCH, X, A, and CCR on the stack, in that order.
2. Set the I bit in the CCR.
3. Fetch the high-order half of the interrupt vector.
4. Fetch the low-order half of the interrupt vector.
5. Delay for one free bus cycle.
6. Fetch three bytes of program information starting at the address indicated by the interrupt vector to fill the instruction queue in preparation for execution of the first instruction in the interrupt service routine.

After the CCR contents are pushed onto the stack, the I bit in the CCR is set to prevent other interrupts while in the interrupt service routine. Although it is possible to clear the I bit with an instruction in the

Table 7-2. Instruction Set Summary (Sheet 4 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR	
						V 1 1 H	I N Z C

CMP #*opr8i*
CMP *opr8a*
CMP *opr16a*
CMP *oprx16*,X
CMP *oprx8*,X
CMP ,X
CMP *oprx16*,SP
CMP *oprx8*,SP
	Compare Accumulator with Memory
	A – M
	(CCR Updated But Operands Not Changed)
		IMM
		DIR
		EXT
		IX2
		IX1
		IX
		SP2
		SP1
			A1 ii
			B1 dd
			C1 hh ll
			D1 ee ff
			E1 ff
			F1
			9E D1 ee ff
			9E E1 ff
				2
				3
				4
				4
				3
				3
				5
				4
					pp
					rpp
					prpp
					prpp
					rpp
					rfp
					pprpp
					prpp
						↕ 1 1 –	– ↕ ↕ ↕

COM *opr8a* COMA COMX COM *oprx8*,X COM ,X COM *oprx8*,SP	Complement M ← ($\overline{M}$)= $FF – (M) (One's Complement) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	DIR INH INH IX1 IX SP1	33 dd 43 53 63 ff 73 9E 63 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	0 1 1 –	– ↕ ↕ 1
CPHX *opr16a* CPHX #*opr16i* CPHX *opr8a* CPHX *oprx8*,SP	Compare Index Register (H:X) with Memory (H:X) – (M:M + $0001) (CCR Updated But Operands Not Changed)	EXT IMM DIR SP1	3E hh ll 65 jj kk 75 dd 9E F3 ff	6 3 5 6	prrfpp ppp rrfpp prrfpp	↕ 1 1 –	– ↕ ↕ ↕
CPX #*opr8i* CPX *opr8a* CPX *opr16a* CPX *oprx16*,X CPX *oprx8*,X CPX ,X CPX *oprx16*,SP CPX *oprx8*,SP	Compare X (Index Register Low) with Memory X – M (CCR Updated But Operands Not Changed)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A3 ii B3 dd C3 hh ll D3 ee ff E3 ff F3 9E D3 ee ff 9E E3 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	↕ 1 1 –	– ↕ ↕ ↕
DAA	Decimal Adjust Accumulator After ADD or ADC of BCD Values	INH	72	1	p	U 1 1 –	– ↕ ↕ ↕
DBNZ *opr8a*,*rel* DBNZA *rel* DBNZX *rel* DBNZ *oprx8*,X,*rel* DBNZ ,X,*rel* DBNZ *oprx8*,SP,*rel*	Decrement A, X, or M and Branch if Not Zero (if (result) ≠ 0) DBNZX Affects X Not H	DIR INH INH IX1 IX SP1	3B dd rr 4B rr 5B rr 6B ff rr 7B rr 9E 6B ff rr	7 4 4 7 6 8	rfwpppp fppp fppp rfwpppp rfwppp prfwpppp	– 1 1 –	– – – –
DEC *opr8a* DECA DECX DEC *oprx8*,X DEC ,X DEC *oprx8*,SP	Decrement M ← (M) – $01 A ← (A) – $01 X ← (X) – $01 M ← (M) – $01 M ← (M) – $01 M ← (M) – $01	DIR INH INH IX1 IX SP1	3A dd 4A 5A 6A ff 7A 9E 6A ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	↕ 1 1 –	– ↕ ↕ –
DIV	Divide A ← (H:A)÷(X); H ← Remainder	INH	52	6	ffffp	– 1 1 –	– – ↕ ↕
EOR #*opr8i* EOR *opr8a* EOR *opr16a* EOR *oprx16*,X EOR *oprx8*,X EOR ,X EOR *oprx16*,SP EOR *oprx8*,SP	Exclusive OR Memory with Accumulator A ← (A ⊕ M)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A8 ii B8 dd C8 hh ll D8 ee ff E8 ff F8 9E D8 ee ff 9E E8 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0 1 1 –	– ↕ ↕ –

8.5.2.2 Example # 2: Moving from PEE to BLPI Mode: External Crystal = 4 MHz, Bus Frequency =16 kHz

In this example, the MCG will move through the proper operational modes from PEE mode with a 4 MHz crystal configured for an 8 MHz bus frequency (see previous example) to BLPI mode with a 16 kHz bus frequency.First, the code sequence will be described. Then a flowchart will be included which illustrates the sequence.

1. First, PEE must transition to PBE mode:
   a) MCGC1 = 0x90 (%10010000)
      – CLKS (bits 7 and 6) set to %10 in order to switch the system clock source to the external reference clock
   b) Loop until CLKST (bits 3 and 2) in MCGSC are %10, indicating that the external reference clock is selected to feed MCGOUT
2. Then, PBE must transition either directly to FBE mode or first through BLPE mode and then to FBE mode:
   a) BLPE: If a transition through BLPE mode is desired, first set LP (bit 3) in MCGC2 to 1
   b) BLPE/FBE: MCGC1 = 0xB8 (%10111000)
      – RDIV (bits 5-3) set to %111, or divide-by-128 because 4 MHz / 128 = 31.25 kHz which is in the 31.25 kHz to 39.0625 kHz range required by the FLL. In BLPE mode, the configuration of the RDIV does not matter because both the FLL and PLL are disabled. Changing them only sets up the dividers for FLL usage in FBE mode
   c) BLPE/FBE: MCGC3 = 0x04 (%00000100)
      – PLLS (bit 6) clear to 0 to select the FLL. In BLPE mode, changing this bit only prepares the MCG for FLL usage in FBE mode. With PLLS = 0, the VDIV value does not matter.
   d) BLPE: If transitioning through BLPE mode, clear LP (bit 3) in MCGC2 to 0 here to switch to FBE mode
   e) FBE: Loop until PLLST (bit 5) in MCGSC is clear, indicating that the current source for the PLLS clock is the FLL
   f) FBE: Optionally, loop until LOCK (bit 6) in the MCGSC is set, indicating that the FLL has acquired lock. Although the FLL is bypassed in FBE mode, it is still enabled and running.
3. Next, FBE mode transitions into FBI mode:
   a) MCGC1 = 0x44 (%01000100)
      – CLKS (bits7 and 6) in MCGSC1 set to %01 in order to switch the system clock to the internal reference clock
      – IREFS (bit 2) set to 1 to select the internal reference clock as the reference clock source
      – RDIV (bits 5-3) set to %000, or divide-by-1 because the trimmed internal reference should be within the 31.25 kHz to 39.0625 kHz range required by the FLL
   b) Loop until IREFST (bit 4) in MCGSC is 1, indicating the internal reference clock has been selected as the reference clock source
   c) Loop until CLKST (bits 3 and 2) in MCGSC are %01, indicating that the internal reference clock is selected to feed MCGOUT

Table 10-1. ADC Channel Assignment

ADCH	Channel	Input
00000	AD0	PTA0/ADP0/MCLK
00001	AD1	PTA1/ADP1/ACMP1+
00010	AD2	PTA2/ADP2/ACMP1P-
00011	AD3	PTA3/ADP3/ACMP1O
00100	AD4	PTA4/ADP4
00101	AD5	PTA5/ADP5
00110	AD6	PTA6/ADP6
00111	AD7	PTA7/ADP7
01000	AD8	PTB0/ADP8
01001	AD9	PTB1/ADP9
01010	AD10	PTB2/ADP10
01011	AD11	PTB3/ADP11
01100	AD12	PTB4/ADP12
01101	AD13	PTB5/ADP13
01110	AD14	PTB6/ADP14
01111	AD15	PTB7/ADP15
10000–11001	AD16 through AD25	Reserved
11010	AD26	Temperature Sensor[1]
11011	AD27	Internal Bandgap[2]
11100	Reserved	Reserved
11101	V_{REFH}	V_{REFH}
11110	V_{REFL}	V_{REFL}
11111	Module Disabled	None

Notes:
1 For information, see Section 10.1.5, “Temperature Sensor”.

10.1.3 Alternate Clock

The ADC module is capable of performing conversions using the MCU bus clock, the bus clock divided by two, the local asynchronous clock (ADACK) within the module, or the alternate clock, ALTCLK. The alternate clock for the MC9S08DV60 Series MCU devices is the external reference clock (MCGERCLK).

The selected clock source must run at a frequency such that the ADC conversion clock (ADCK) runs at a frequency within its specified range (f_{ADCK}) after being divided down from the ALTCLK input as determined by the ADIV bits.

ALTCLK is active while the MCU is in wait mode provided the conditions described above are met. This allows ALTCLK to be used as the conversion clock source for the ADC while the MCU is in wait mode.

ALTCLK cannot be used as the ADC conversion clock source while the MCU is in either stop2 or stop3.

10.1.4 Hardware Trigger

The ADC hardware trigger, ADHWT, is the output from the real time counter (RTC). The RTC counter can be clocked by either MCGERCLK or a nominal 1 kHz clock source.

The period of the RTC is determined by the input clock frequency, the RTCPS bits, and the RTCMOD register. When the ADC hardware trigger is enabled, a conversion is initiated upon an RTC counter overflow.

The RTC can be configured to cause a hardware trigger in MCU run, wait, and stop3.

11.3.4 IIC Status Register (IICS)

	7	6	5	4	3	2	1	0
R	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-6. IIC Status Register (IICS)

Table 11-6. IICS Field Descriptions

Field	Description
7 TCF	**Transfer Complete Flag.** This bit is set on the completion of a byte transfer. This bit is only valid during or immediately following a transfer to the IIC module or from the IIC module.The TCF bit is cleared by reading the IICD register in receive mode or writing to the IICD in transmit mode. 0 Transfer in progress 1 Transfer complete
6 IAAS	**Addressed as a Slave.** The IAAS bit is set when the calling address matches the programmed slave address or when the GCAEN bit is set and a general call is received. Writing the IICC register clears this bit. 0 Not addressed 1 Addressed as a slave
5 BUSY	**Bus Busy.** The BUSY bit indicates the status of the bus regardless of slave or master mode. The BUSY bit is set when a start signal is detected and cleared when a stop signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	**Arbitration Lost.** This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software by writing a 1 to it. 0 Standard bus operation 1 Loss of arbitration
2 SRW	**Slave Read/Write.** When addressed as a slave, the SRW bit indicates the value of the R/W command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	**IIC Interrupt Flag.** The IICIF bit is set when an interrupt is pending. This bit must be cleared by software, by writing a 1 to it in the interrupt routine. One of the following events can set the IICIF bit: • One byte transfer completes • Match of slave address to calling address • Arbitration lost 0 No interrupt pending 1 Interrupt pending
0 RXAK	**Receive Acknowledge**. When the RXAK bit is low, it indicates an acknowledge signal has been received after the completion of one byte of data transmission on the bus. If the RXAK bit is high it means that no acknowledge signal is detected. 0 Acknowledge received 1 No acknowledge received

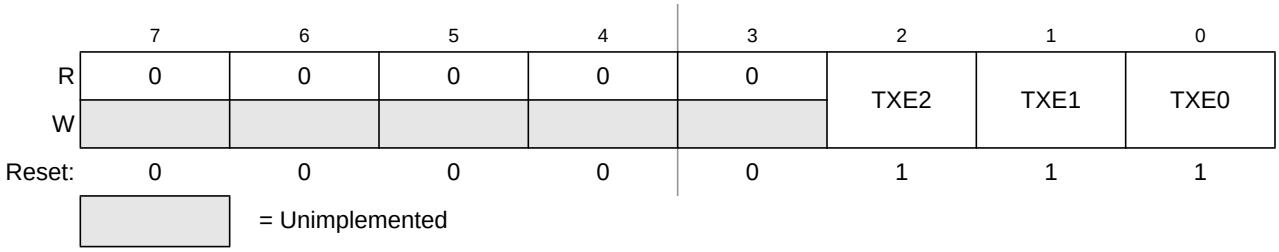

Figure 12-10. MSCAN Transmitter Flag Register (CANTFLG)

NOTE

The CANTFLG register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Read: Anytime
Write: Anytime for TXEx flags when not in initialization mode; write of 1 clears flag, write of 0 is ignored

Table 12-11. CANTFLG Register Field Descriptions

Field	Description
2:0 TXE[2:0]	**Transmitter Buffer Empty** — This flag indicates that the associated transmit message buffer is empty, and thus not scheduled for transmission. The CPU must clear the flag after a message is set up in the transmit buffer and is due for transmission. The MSCAN sets the flag after the message is sent successfully. The flag is also set by the MSCAN when the transmission request is successfully aborted due to a pending abort request (see Section 12.3.8, "MSCAN Transmitter Message Abort Request Register (CANTARQ)"). If not masked, a transmit interrupt is pending while this flag is set. Clearing a TXEx flag also clears the corresponding ABTAKx (see Section 12.3.9, "MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)"). When a TXEx flag is set, the corresponding ABTRQx bit is cleared (see Section 12.3.8, "MSCAN Transmitter Message Abort Request Register (CANTARQ)"). When listen-mode is active (see Section 12.3.2, "MSCAN Control Register 1 (CANCTL1)") the TXEx flags cannot be cleared and no transmission is started. Read and write accesses to the transmit buffer are blocked, if the corresponding TXEx bit is cleared (TXEx = 0) and the buffer is scheduled for transmission. 0 The associated message buffer is full (loaded with a message due for transmission) 1 The associated message buffer is empty (not scheduled)

12.3.7 MSCAN Transmitter Interrupt Enable Register (CANTIER)

This register contains the interrupt enable bits for the transmit buffer empty interrupt flags.

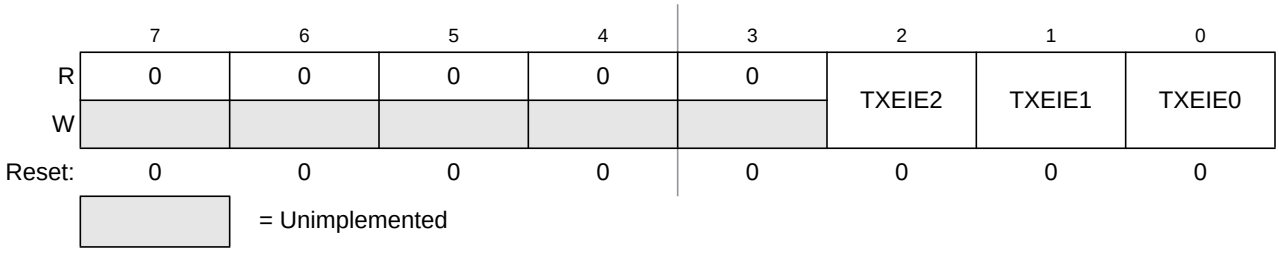

Figure 12-11. MSCAN Transmitter Interrupt Enable Register (CANTIER)

Table 12-33. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

12.4.5 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message transmit buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.
- The transmission buffer with the lowest local priority field wins the prioritization.

In cases of more than one buffer having the same lowest priority, the message buffer with the lower index number wins.

	7	6	5	4	3	2	1	0
R W	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
Reset:	0	0	0	0	0	0	0	0

Figure 12-35. Transmit Buffer Priority Register (TBPR)

Read: Anytime when TXEx flag is set (see Section 12.3.6, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.10, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Anytime when TXEx flag is set (see Section 12.3.6, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.10, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

12.4.6 Time Stamp Register (TSRH–TSRL)

If the TIME bit is enabled, the MSCAN will write a time stamp to the respective registers in the active transmit or receive buffer as soon as a message has been acknowledged on the CAN bus (see

12.6.2 Bus-Off Recovery

The bus-off recovery is user configurable. The bus-off state can either be exited automatically or on user request.

For reasons of backwards compatibility, the MSCAN defaults to automatic recovery after reset. In this case, the MSCAN will become error active again after counting 128 occurrences of 11 consecutive recessive bits on the CAN bus (See the Bosch CAN specification for details).

If the MSCAN is configured for user request (BORM set in Section 12.3.2, "MSCAN Control Register 1 (CANCTL1)"), the recovery from bus-off starts after both independent events have become true:

- 128 occurrences of 11 consecutive recessive bits on the CAN bus have been monitored
- BOHOLD in Section 12.3.12, "MSCAN Miscellaneous Register (CANMISC) has been cleared by the user

These two events may occur in any order.

16.6.2.1.2 Center-Aligned PWM Case

When CPWMS=1, TOF gets set when the timer counter changes direction from up-counting to down-counting at the end of the terminal count (the value in the modulo register). In this case the TOF corresponds to the end of a PWM period.

16.6.2.2 Channel Event Interrupt Description

The meaning of channel interrupts depends on the channel's current mode (input-capture, output-compare, edge-aligned PWM, or center-aligned PWM).

16.6.2.2.1 Input Capture Events

When a channel is configured as an input capture channel, the ELSnB:ELSnA control bits select no edge (off), rising edges, falling edges or any edge as the edge which triggers an input capture event. When the selected edge is detected, the interrupt flag is set. The flag is cleared by the two-step sequence described in Section 16.6.2, "Description of Interrupt Operation."

16.6.2.2.2 Output Compare Events

When a channel is configured as an output compare channel, the interrupt flag is set each time the main timer counter matches the 16-bit value in the channel value register. The flag is cleared by the two-step sequence described Section 16.6.2, "Description of Interrupt Operation."

16.6.2.2.3 PWM End-of-Duty-Cycle Events

For channels configured for PWM operation there are two possibilities. When the channel is configured for edge-aligned PWM, the channel flag gets set when the timer counter matches the channel value register which marks the end of the active duty cycle period. When the channel is configured for center-aligned PWM, the timer count matches the channel value register twice during each PWM cycle. In this CPWM case, the channel flag is set at the start and at the end of the active duty cycle period which are the times when the timer counter matches the channel value register. The flag is cleared by the two-step sequence described Section 16.6.2, "Description of Interrupt Operation."

16.7 The Differences from TPM v2 to TPM v3

1. Write to TPMxCNTH:L registers (Section 16.3.2, "TPM-Counter Registers (TPMxCNTH:TPMxCNTL)) [SE110-TPM case 7]

   Any write to TPMxCNTH or TPMxCNTL registers in TPM v3 clears the TPM counter (TPMxCNTH:L) and the prescaler counter. Instead, in the TPM v2 only the TPM counter is cleared in this case.
2. Read of TPMxCNTH:L registers (Section 16.3.2, "TPM-Counter Registers (TPMxCNTH:TPMxCNTL))
   - In TPM v3, any read of TPMxCNTH:L registers during BDM mode returns the value of the TPM counter that is frozen. In TPM v2, if only one byte of the TPMxCNTH:L registers was read before the BDM mode became active, then any read of TPMxCNTH:L registers during

A.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table A-6. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	V_{DD}		2.7	—	5.5	V
2	P	Output high voltage — All I/O pins, low-drive strength	V_{OH}	5 V, I_{Load} = –2 mA	V_{DD} – 1.5	—	—	V
	C			3 V, I_{Load} = –0.6 mA	V_{DD} – 1.5	—	—	
	C			5 V, I_{Load} = –0.4 mA	V_{DD} – 0.8	—	—	
	C			3 V, I_{Load} = –0.24 mA	V_{DD} – 0.8	—	—	
	P	Output high voltage — All I/O pins, high-drive strength		5 V, I_{Load} = –10 mA	V_{DD} – 1.5	—	—	
	C			3 V, I_{Load} = –3 mA	V_{DD} – 1.5	—	—	
	C			5 V, I_{Load} = –2 mA	V_{DD} – 0.8	—	—	
	C			3 V, I_{Load} = –0.4 mA	V_{DD} – 0.8	—	—	
3	C	Output high current — Max total I_{OH} for all ports	I_{OHT}	5 V	0	—	-100	mA
				3 V	0	—	-60	
4	P	Output low voltage — All I/O pins, low-drive strength	V_{OL}	5 V, I_{Load} = 2 mA	—	—	1.5	V
	C			3 V, I_{Load} = 0.6 mA	—	—	1.5	
	C			5 V, I_{Load} = 0.4 mA	—	—	0.8	
	C			3 V, I_{Load} = 0.24 mA	—	—	0.8	
	P	Output low voltage — All I/O pins, high-drive strength		5 V, I_{Load} = 10 mA	—	—	1.5	
	C			3 V, I_{Load} = 3 mA	—	—	1.5	
	C			5 V, I_{Load} = 2 mA	—	—	0.8	
	C			3 V, I_{Load} = 0.4 mA	—	—	0.8	
5	C	Output low current — Max total I_{OL} for all ports	I_{OLT}	5 V	0	—	100	mA
				3 V	0	—	60	
6	C	Input high voltage; all digital inputs	V_{IH}	5V	0.65 x V_{DD}	—	—	V
7	C	Input low voltage; all digital inputs	V_{IL}	5V	—	—	0.35 x V_{DD}	
8	C	Input hysteresis	V_{hys}		0.06 x V_{DD}			mV
9	P	Input leakage current (Per pin) all input only pins	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current (per pin) all input/output	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
11	P	Pullup resistors (or Pulldown[2] resistors when enabled)	R_{PU}, R_{PD}	5 V	20	45	65	kΩ
	C			3 V	20	45	65	
12	T	Input Capacitance, all pins	C_{In}		—	—	8	pF
13	D	RAM retention voltage	V_{RAM}		—	0.6	1.0	V

Table A-7. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
6	C	RTC adder to stop2 or stop3[5], 25°C		5	300	—	nA
				3	300	—	nA
7	C	LVD adder to stop3 (LVDE = LVDSE = 1)		5	110	—	µA
				3	90	—	µA
8	C	Adder to stop3 for oscillator enabled[6] (IRCLKEN = 1 and IREFSTEN = 1 or ERCLKEN = 1 and EREFSTEN = 1)		5	5	—	µA
				3	5	—	µA

1 Typicals are measured at 25°C, unless otherwise noted.

2 Maximum values in this column apply for the full operating temperature range of the device unless otherwise noted.

3 All modules except ADC active, MCG configured for FBE, and does not include any dc loads on port pins

4 Stop currents are tested in production for 25°C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

5 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

6 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

A.8 Analog Comparator (ACMP) Electricals

Table A-8. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	D	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}		20	40	mV
5	D	Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	--	--	1.0	µA
7	D	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs

A.9 ADC Characteristics

Table A-9. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V	
	Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	ΔV_{DDAD}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	ΔV_{SSAD}	-100	0	+100	mV	

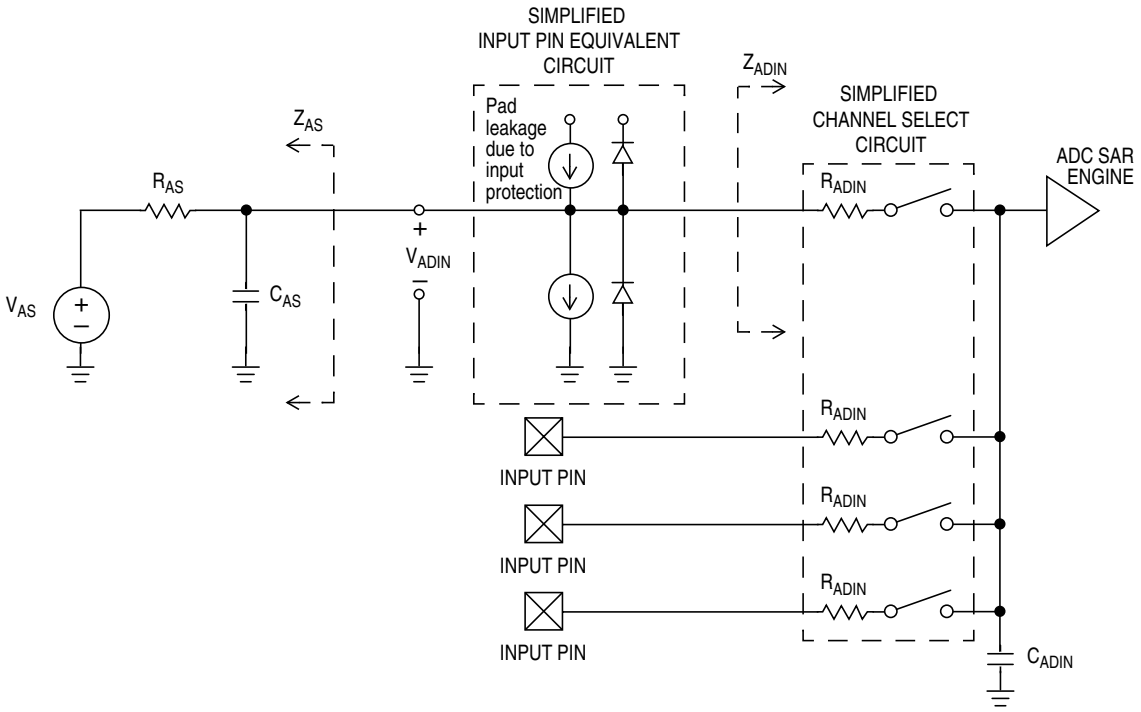

Figure A-1. ADC Input Impedance Equivalency Diagram

Table A-10. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current	ADLPC=1 ADLSMP=1 ADCO=1	T	I_{DD} + I_{DDAD}	—	133	—	µA	ADC current only
Supply Current	ADLPC=1 ADLSMP=0 ADCO=1	T	I_{DD} + I_{DDAD}	—	218	—	µA	ADC current only
Supply Current	ADLPC=0 ADLSMP=1 ADCO=1	T	I_{DD} + I_{DDAD}	—	327	—	µA	ADC current only
Supply Current	ADLPC=0 ADLSMP=0 ADCO=1	D	I_{DD} + I_{DDAD}	—	0.582	1	mA	ADC current only
Supply Current	Stop, Reset, Module Off		I_{DD} + I_{DDAD}	—	0.011	1	µA	ADC current only
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
	Low Power (ADLPC=1)			1.25	2	3.3		

A.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

A.12.1 Control Timing

Table A-13. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D/P	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	T	Internal low-power oscillator period	t_{LPO}	—	1500	—	µs
3	D	External reset pulse width[2]	t_{extrst}	1.5 x t_{cyc}		—	ns
4	D	Reset low drive[3]	t_{rstdrv}	34 x t_{cyc}		—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	25		—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	25		—	ns
7	D	IRQ/PIAx/ PIBx/PIDx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 t_{cyc}	—	—	ns
8	T	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 40 75		ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 11 35		ns

1 Typical data was characterized at 5.0 V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 When any reset is initiated, internal circuitry drives the $\overline{\text{RESET}}$ pin low for about 34 cycles of t_{cyc}. After POR reset, the bus clock frequency changes to the untrimmed DCO frequency (freset = (f_{dco_ut})/4) because TRIM is reset to 0x80 and FTRIM is reset to 0; and there is an extra divide-by-two because BDIV is reset to 0:1. After other resets, trim stays at the pre-reset value.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

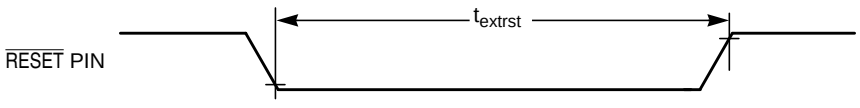

Figure A-2. Reset Timing