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Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | S08 |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | CANbus, I ² C, LINbus, SCI, SPI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 10x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08dv32f2mlcr |

Table 4-1. Reset and Interrupt Vectors

| Address (High/Low) | Vector | Vector Name |
|-----------------------|------------------------|-------------|
| 0xFFCE:0xFFCF | IIC | Viic |
| 0xFFD0:0xFFD1 | ADC Conversion | Vadc |
| 0xFFD2:0xFFD3 | Port A, Port B, Port D | Vport |
| 0xFFD4:0xFFD5 | SCI2 Transmit | Vsci2tx |
| 0xFFD6:0xFFD7 | SCI2 Receive | Vsci2rx |
| 0xFFD8:0xFFD9 | SCI2 Error | Vsci2err |
| 0xFFDA:0xFFDB | SCI1 Transmit | Vsci1tx |
| 0xFFDC:0xFFDD | SCI1 Receive | Vsci1rx |
| 0xFFDE:0xFFDF | SCI1 Error | Vsci1err |
| 0xFFE0:0xFFE1 | SPI | Vspi |
| 0xFFE2:0xFFE3 | TPM2 Overflow | Vtpm2ovf |
| 0xFFE4:0xFFE5 | TPM2 Channel 1 | Vtpm2ch1 |
| 0xFFE6:0xFFE7 | TPM2 Channel 0 | Vtpm2ch0 |
| 0xFFE8:0xFFE9 | TPM1 Overflow | Vtpm1ovf |
| 0xFFEA:0xFFEB | TPM1 Channel 5 | Vtpm1ch5 |
| 0xFFEC:0xFFED | TPM1 Channel 4 | Vtpm1ch4 |
| 0xFFEE:0xFFEF | TPM1 Channel 3 | Vtpm1ch3 |
| 0xFFFF0:0xFFFF1 | TPM1 Channel 2 | Vtpm1ch2 |
| 0xFFFF2:0xFFFF3 | TPM1 Channel 1 | Vtpm1ch1 |
| 0xFFFF4:0xFFFF5 | TPM1 Channel 0 | Vtpm1ch0 |
| 0xFFFF6:0xFFFF7 | MCG Loss of lock | Vlol |
| 0xFFFF8:0xFFFF9 | Low-Voltage Detect | Vlvd |
| 0xFFFFA:0xFFFFB | IRQ | Virq |
| 0xFFFFC:0xFFFFD | SWI | Vswi |
| 0xFFFFE:0xFFFFF | Reset | Vreset |

5.6 Low-Voltage Detect (LVD) System

The MC9S08DV60 Series includes a system to protect against low-voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The system is comprised of a power-on reset (POR) circuit and a LVD circuit with trip voltages for warning and detection. The LVD circuit is enabled when LVDE in SPMSC1 is set to 1. The LVD is disabled upon entering any of the stop modes unless LVDSE is set in SPMSC1. If LVDSE and LVDE are both set, then the MCU cannot enter stop2 (it will enter stop3 instead), and the current consumption in stop3 with the LVD enabled will be higher.

5.6.1 Power-On Reset Operation

When power is initially applied to the MCU, or when the supply voltage drops below the power-on reset rearm voltage level, V_{POR} , the POR circuit will cause a reset condition. As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above the low-voltage detection low threshold, V_{LVDL} . Both the POR bit and the LVD bit in SRS are set following a POR.

5.6.2 Low-Voltage Detection (LVD) Reset Operation

The LVD can be configured to generate a reset upon detection of a low-voltage condition by setting LVDRE to 1. The low-voltage detection threshold is determined by the LVDV bit. After an LVD reset has occurred, the LVD system will hold the MCU in reset until the supply voltage has risen above the low-voltage detection threshold. The LVD bit in the SRS register is set following either an LVD reset or POR.

5.6.3 Low-Voltage Warning (LVW) Interrupt Operation

The LVD system has a low-voltage warning flag to indicate to the user that the supply voltage is approaching the low-voltage condition. When a low-voltage warning condition is detected and is configured for interrupt operation (LVWIE set to 1), LVWIF in SPMSC1 will be set and an LVW interrupt request will occur.

5.7 MCLK Output

The PTA0 pin is shared with the MCLK clock output. If the MCSEL bits are all zeroes, the MCLK clock is disabled. Setting any of the MCSEL bits causes the PTA0 pin to output a divided version of the internal MCU bus clock regardless of the state of the port data direction control bit for the pin. The divide ratio is determined by the MCSEL bits. The slew rate and drive strength for the pin are controlled by PTASE0 and PTADS0, respectively. The maximum clock output frequency is limited if slew rate control is enabled, see the electrical specifications for the maximum frequency under different conditions.

In general, whenever a pin is shared with both an alternate digital function and an analog function, the analog function has priority such that if both the digital and analog functions are enabled, the analog function controls the pin.

It is a good programming practice to write to the port data register before changing the direction of a port pin to become an output. This ensures that the pin will not be driven momentarily with an old data value that happened to be in the port data register.

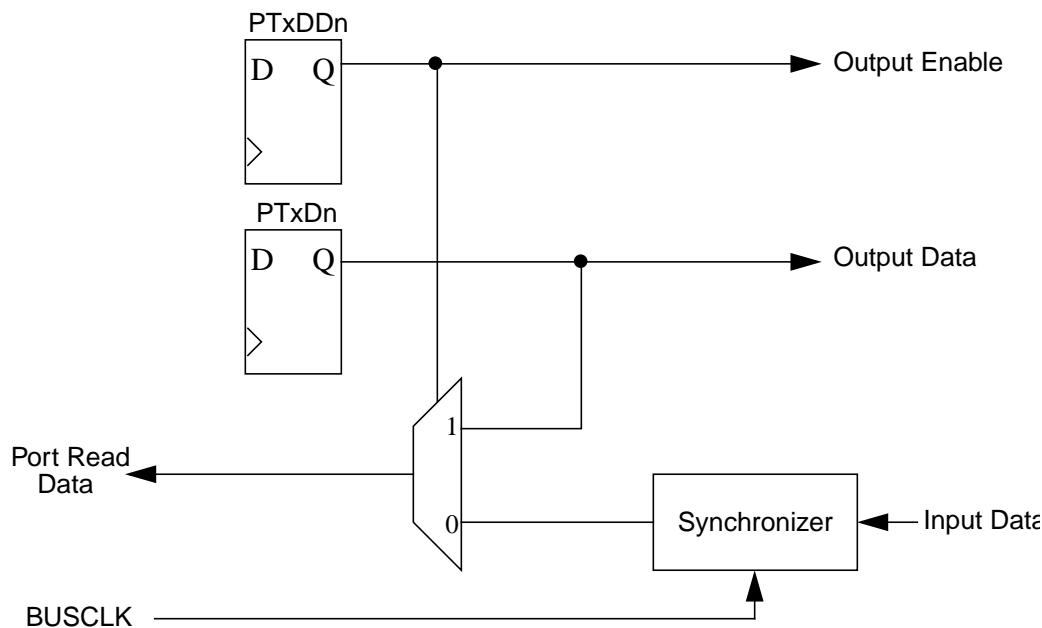


Figure 6-1. Parallel I/O Block Diagram

6.2 Pull-up, Slew Rate, and Drive Strength

Associated with the parallel I/O ports is a set of registers located in the high page register space that operate independently of the parallel I/O registers. These registers are used to control pull-ups, slew rate, and drive strength for the pins.

An internal pull-up device can be enabled for each port pin by setting the corresponding bit in the pull-up enable register (PTxPEN). The pull-up device is disabled if the pin is configured as an output by the parallel I/O control logic or any shared peripheral function regardless of the state of the corresponding pull-up enable register bit. The pull-up device is also disabled if the pin is controlled by an analog function.

Slew rate control can be enabled for each port pin by setting the corresponding bit in the slew rate control register (PTxSEn). When enabled, slew control limits the rate at which an output can transition in order to reduce EMC emissions. Slew rate control has no effect on pins that are configured as inputs.

NOTE

Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.

6.5.5.5 Port E Drive Strength Selection Register (PTEDS)

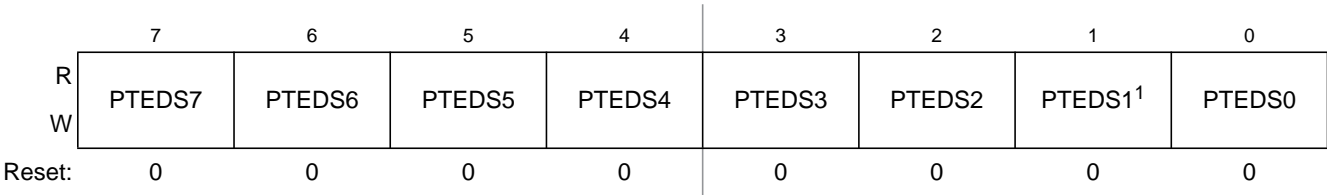


Figure 6-36. Drive Strength Selection for Port E Register (PTEDS)

¹ PTEDS1 has no effect on the input-only PTE1 pin.

Table 6-34. PTEDS Register Field Descriptions

| Field | Description |
|-------------------|--|
| 7:0 PTEDS[7:0] | Output Drive Strength Selection for Port E Bits — Each of these control bits selects between low and high output drive for the associated PTE pin. For port E pins that are configured as inputs, these bits have no effect. 0 Low output drive strength selected for port E bit n. 1 High output drive strength selected for port E bit n. |

6.5.6 Port F Registers

Port F is controlled by the registers listed below.

6.5.6.1 Port F Data Register (PTFD)

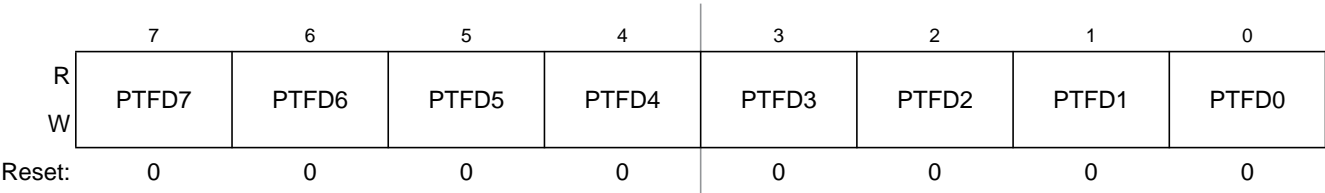


Figure 6-37. Port F Data Register (PTFD)

Table 6-35. PTFD Register Field Descriptions

| Field | Description |
|------------------|---|
| 7:0 PTFD[7:0] | Port F Data Register Bits — For port F pins that are inputs, reads return the logic level on the pin. For port F pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port F pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTFD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups disabled. |

6.5.6.2 Port F Data Direction Register (PTFDD)

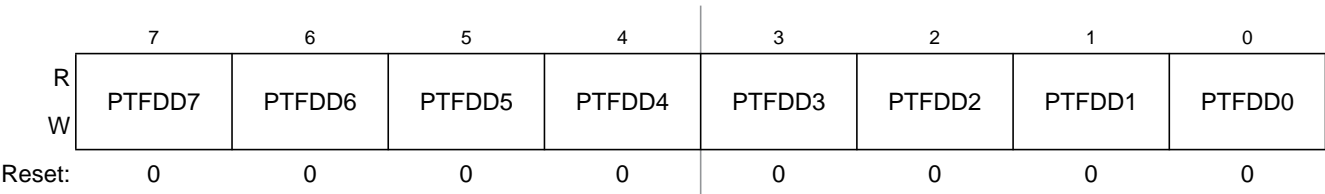


Figure 6-38. Port F Data Direction Register (PTFDD)

Table 6-36. PTFDD Register Field Descriptions

| Field | Description |
|-------------------|--|
| 7:0 PTFDD[7:0] | Data Direction for Port F Bits — These read/write bits control the direction of port F pins and what is read for PTFD reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port F bit n and PTFD reads return the contents of PTFDn. |

Chapter 7

Central Processor Unit (S08CPUV3)

7.1 Introduction

This section provides summary information about the registers, addressing modes, and instruction set of the CPU of the HCS08 Family. For a more detailed discussion, refer to the *HCS08 Family Reference Manual, volume 1*, Freescale Semiconductor document order number HCS08RMV1/D.

The HCS08 CPU is fully source- and object-code-compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes were added to improve C compiler efficiency and to support a new background debug system which replaces the monitor mode of earlier M68HC08 microcontrollers (MCU).

7.1.1 Features

Features of the HCS08 CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 Families
- All registers and memory are mapped to a single 64-Kbyte address space
- 16-bit stack pointer (any size stack anywhere in 64-Kbyte address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:
 - Inherent — Operands in internal registers
 - Relative — 8-bit signed offset to branch destination
 - Immediate — Operand in next object code byte(s)
 - Direct — Operand in memory at 0x0000–0x00FF
 - Extended — Operand anywhere in 64-Kbyte address space
 - Indexed relative to H:X — Five submodes including auto increment
 - Indexed relative to SP — Improves C efficiency dramatically
- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- STOP and WAIT instructions to invoke low-power operating modes

Table 7-2. Instruction Set Summary (Sheet 2 of 9)

| Source Form | Operation | Address Mode | Object Code | Cycles | Cyc-by-Cyc Details | Affect on CCR | |
|--|---|---|--|--------------------------------------|--|---------------|---------|
| | | | | | | V 1 1 H | I N Z C |
| BCC <i>rel</i> | Branch if Carry Bit Clear (if C = 0) | REL | 24 rr | 3 | ppp | - 1 1 - | - - - - |
| BCLR <i>n,opr8a</i> | Clear Bit n in Memory (Mn ← 0) | DIR (b0) | 11 dd | 5 | r fwpp | - 1 1 - | - - - - |
| | | DIR (b1) | 13 dd | 5 | r fwpp | | |
| | | DIR (b2) | 15 dd | 5 | r fwpp | | |
| | | DIR (b3) | 17 dd | 5 | r fwpp | | |
| | | DIR (b4) | 19 dd | 5 | r fwpp | | |
| | | DIR (b5) | 1B dd | 5 | r fwpp | | |
| | | DIR (b6) | 1D dd | 5 | r fwpp | | |
| | | DIR (b7) | 1F dd | 5 | r fwpp | | |
| | | | | | | | |
| BCS <i>rel</i> | Branch if Carry Bit Set (if C = 1) (Same as BLO) | REL | 25 rr | 3 | ppp | - 1 1 - | - - - - |
| BEQ <i>rel</i> | Branch if Equal (if Z = 1) | REL | 27 rr | 3 | ppp | - 1 1 - | - - - - |
| BGE <i>rel</i> | Branch if Greater Than or Equal To (if N ⊕ V = 0) (Signed) | REL | 90 rr | 3 | ppp | - 1 1 - | - - - - |
| BGND | Enter active background if ENBDM=1 Waits for and processes BDM commands until GO, TRACE1, or TAGGO | INH | 82 | 5+ | f p . . . ppp | - 1 1 - | - - - - |
| BGT <i>rel</i> | Branch if Greater Than (if Z (N ⊕ V) = 0) (Signed) | REL | 92 rr | 3 | ppp | - 1 1 - | - - - - |
| BHCC <i>rel</i> | Branch if Half Carry Bit Clear (if H = 0) | REL | 28 rr | 3 | ppp | - 1 1 - | - - - - |
| BHCS <i>rel</i> | Branch if Half Carry Bit Set (if H = 1) | REL | 29 rr | 3 | ppp | - 1 1 - | - - - - |
| BHI <i>rel</i> | Branch if Higher (if C Z = 0) | REL | 22 rr | 3 | ppp | - 1 1 - | - - - - |
| BHS <i>rel</i> | Branch if Higher or Same (if C = 0) (Same as BCC) | REL | 24 rr | 3 | ppp | - 1 1 - | - - - - |
| BIH <i>rel</i> | Branch if IRQ Pin High (if IRQ pin = 1) | REL | 2F rr | 3 | ppp | - 1 1 - | - - - - |
| BIL <i>rel</i> | Branch if IRQ Pin Low (if IRQ pin = 0) | REL | 2E rr | 3 | ppp | - 1 1 - | - - - - |
| BIT # <i>opr8i</i> BIT <i>opr8a</i> BIT <i>opr16a</i> BIT <i>opr16,X</i> BIT <i>opr8,X</i> BIT <i>,X</i> BIT <i>opr16,SP</i> BIT <i>opr8,SP</i> | Bit Test (A) & (M) (CCR Updated but Operands Not Changed) | IMM DIR EXT IX2 IX1 IX SP2 SP1 | A5 ii B5 dd C5 hh ll D5 ee ff E5 ff F5 9E D5 ee ff 9E E5 ff | 2 3 4 4 3 3 5 4 | pp rpp prpp prpp rpp rfp pprpp prpp | 0 1 1 - | - ↑ ↓ - |
| BLE <i>rel</i> | Branch if Less Than or Equal To (if Z (N ⊕ V) = 1) (Signed) | REL | 93 rr | 3 | ppp | - 1 1 - | - - - - |
| BLO <i>rel</i> | Branch if Lower (if C = 1) (Same as BCS) | REL | 25 rr | 3 | ppp | - 1 1 - | - - - - |
| BLS <i>rel</i> | Branch if Lower or Same (if C Z = 1) | REL | 23 rr | 3 | ppp | - 1 1 - | - - - - |
| BLT <i>rel</i> | Branch if Less Than (if N ⊕ V = 1) (Signed) | REL | 91 rr | 3 | ppp | - 1 1 - | - - - - |
| BMC <i>rel</i> | Branch if Interrupt Mask Clear (if I = 0) | REL | 2C rr | 3 | ppp | - 1 1 - | - - - - |
| BMI <i>rel</i> | Branch if Minus (if N = 1) | REL | 2B rr | 3 | ppp | - 1 1 - | - - - - |
| BMS <i>rel</i> | Branch if Interrupt Mask Set (if I = 1) | REL | 2D rr | 3 | ppp | - 1 1 - | - - - - |
| BNE <i>rel</i> | Branch if Not Equal (if Z = 0) | REL | 26 rr | 3 | ppp | - 1 1 - | - - - - |

When a conversion is aborted, the contents of the data registers, ADCRH and ADCRL, are not altered. However, they continue to be the values transferred after the completion of the last successful conversion. If the conversion was aborted by a reset, ADCRH and ADCRL return to their reset states.

10.4.4.4 Power Control

The ADC module remains in its idle state until a conversion is initiated. If ADACK is selected as the conversion clock source, the ADACK clock generator is also enabled.

Power consumption when active can be reduced by setting ADLPC. This results in a lower maximum value for f_{ADCK} (see the electrical specifications).

10.4.4.5 Sample Time and Total Conversion Time

The total conversion time depends on the sample time (as determined by ADLSMP), the MCU bus frequency, the conversion mode (8-bit, 10-bit or 12-bit), and the frequency of the conversion clock (f_{ADCK}). After the module becomes active, sampling of the input begins. ADLSMP selects between short (3.5 ADCK cycles) and long (23.5 ADCK cycles) sample times. When sampling is complete, the converter is isolated from the input channel and a successive approximation algorithm is performed to determine the digital value of the analog signal. The result of the conversion is transferred to ADCRH and ADCRL upon completion of the conversion algorithm.

If the bus frequency is less than the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADLSMP=0). If the bus frequency is less than 1/11th of the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADLSMP=1).

The maximum total conversion time for different conditions is summarized in [Table 10-13](#).

Table 10-13. Total Conversion Time vs. Control Conditions

| Conversion Type | ADICLK | ADLSMP | Max Total Conversion Time |
|--|--------|--------|--|
| Single or first continuous 8-bit | 0x, 10 | 0 | 20 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 10-bit or 12-bit | 0x, 10 | 0 | 23 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 8-bit | 0x, 10 | 1 | 40 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 10-bit or 12-bit | 0x, 10 | 1 | 43 ADCK cycles + 5 bus clock cycles |
| Single or first continuous 8-bit | 11 | 0 | 5 μ s + 20 ADCK + 5 bus clock cycles |
| Single or first continuous 10-bit or 12-bit | 11 | 0 | 5 μ s + 23 ADCK + 5 bus clock cycles |
| Single or first continuous 8-bit | 11 | 1 | 5 μ s + 40 ADCK + 5 bus clock cycles |
| Single or first continuous 10-bit or 12-bit | 11 | 1 | 5 μ s + 43 ADCK + 5 bus clock cycles |
| Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}$ | xx | 0 | 17 ADCK cycles |
| Subsequent continuous 10-bit or 12-bit; $f_{BUS} \geq f_{ADCK}$ | xx | 0 | 20 ADCK cycles |
| Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}/11$ | xx | 1 | 37 ADCK cycles |

11.4.1.3 Data Transfer

Before successful slave addressing is achieved, the data transfer can proceed byte-by-byte in a direction specified by the R/\overline{W} bit sent by the calling master.

All transfers that come after an address cycle are referred to as data transfers, even if they carry sub-address information for the slave device

Each data byte is 8 bits long. Data may be changed only while SCL is low and must be held stable while SCL is high as shown in [Figure 11-9](#). There is one clock pulse on SCL for each data bit, the msb being transferred first. Each data byte is followed by a 9th (acknowledge) bit, which is signalled from the receiving device. An acknowledge is signalled by pulling the SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit time, the SDA line must be left high by the slave. The master interprets the failed acknowledge as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets this as an end of data transfer and releases the SDA line.

In either case, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a stop signal.
- Commences a new calling by generating a repeated start signal.

11.4.1.4 Stop Signal

The master can terminate the communication by generating a stop signal to free the bus. However, the master may generate a start signal followed by a calling command without generating a stop signal first. This is called repeated start. A stop signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see [Figure 11-9](#)).

The master can generate a stop even if the slave has generated an acknowledge at which point the slave must release the bus.

11.4.1.5 Repeated Start Signal

As shown in [Figure 11-9](#), a repeated start signal is a start signal generated without first generating a stop signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

11.4.1.6 Arbitration Procedure

The IIC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case,

Table 12-5. Baud Rate Prescaler

| BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 | Prescaler value (P) |
|------|------|------|------|------|------|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 4 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 64 |

12.3.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

| | | | | | | | | |
|--------|------|--------|--------|--------|--------|--------|--------|--------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | |
| W | SAMP | TSEG22 | TSEG21 | TSEG20 | TSEG13 | TSEG12 | TSEG11 | TSEG10 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure 12-7. MSCAN Bus Timing Register 1 (CANBTR1)

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-6. CANBTR1 Register Field Descriptions

| Field | Description |
|-------------------|---|
| 7 SAMP | Sampling — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit ¹ . If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0). |
| 6:4 TSEG2[2:0] | Time Segment 2 — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 12-43). Time segment 2 (TSEG2) values are programmable as shown in Table 12-7 . |
| 3:0 TSEG1[3:0] | Time Segment 1 — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 12-43). Time segment 1 (TSEG1) values are programmable as shown in Table 12-8 . |

¹ In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

12.5.7.1 Description of Interrupt Operation

The MSCAN supports four interrupt vectors (see [Table 12-37](#)), any of which can be individually masked (for details see sections from [Section 12.3.5](#), “MSCAN Receiver Interrupt Enable Register (CANRIER),” to [Section 12.3.7](#), “MSCAN Transmitter Interrupt Enable Register (CANTIER)”).

NOTE

The dedicated interrupt vector addresses are defined in the [Resets and Interrupts](#) chapter.

Table 12-37. Interrupt Vectors

| Interrupt Source | CCR Mask | Local Enable |
|---|----------|------------------------|
| Wake-Up Interrupt (WUPIF) | 1 bit | CANRIER (WUPIE) |
| Error Interrupts Interrupt (CSCIF, OVRIF) | 1 bit | CANRIER (CSCIE, OVRIE) |
| Receive Interrupt (RXF) | 1 bit | CANRIER (RXFIE) |
| Transmit Interrupts (TXE[2:0]) | 1 bit | CANTIER (TXEIE[2:0]) |

12.5.7.2 Transmit Interrupt

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXEx flag of the empty message buffer is set.

12.5.7.3 Receive Interrupt

A message is successfully received and shifted into the foreground buffer (RxFG) of the receiver FIFO. This interrupt is generated immediately after receiving the EOF symbol. The RXF flag is set. If there are multiple messages in the receiver FIFO, the RXF flag is set as soon as the next message is shifted to the foreground buffer.

12.5.7.4 Wake-Up Interrupt

A wake-up interrupt is generated if activity on the CAN bus occurs during MSCAN internal sleep mode. WUPE (see [Section 12.3.1](#), “MSCAN Control Register 0 (CANCTL0)”) must be enabled.

12.5.7.5 Error Interrupt

An error interrupt is generated if an overrun of the receiver FIFO, error, warning, or bus-off condition occurs. [Section 12.3.4.1](#), “MSCAN Receiver Flag Register (CANRFLG)” indicates one of the following conditions:

- **Overrun** — An overrun condition of the receiver FIFO as described in [Section 12.5.2.3](#), “[Receive Structures](#),” occurred.
- **CAN Status Change** — The actual value of the transmit and receive error counters control the CAN bus state of the MSCAN. As soon as the error counters skip into a critical range (Tx/Rx-warning, Tx/Rx-error, bus-off) the MSCAN flags an error condition. The status change, which caused the error condition, is indicated by the TSTAT and RSTAT flags (see

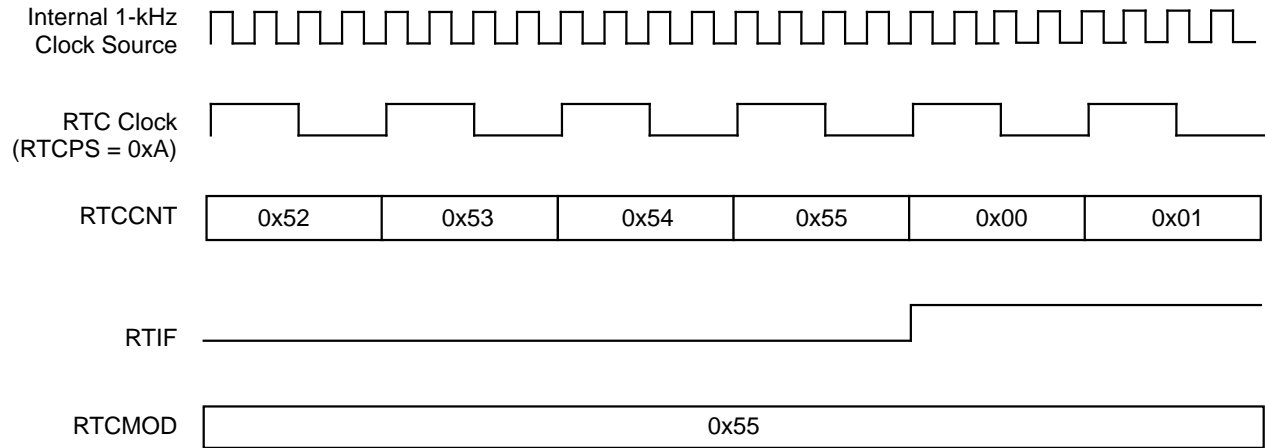


Figure 15-6. RTC Counter Overflow Example

In the example of Figure 15-6, the selected clock source is the 1-kHz internal oscillator clock source. The prescaler (RTCPs) is set to 0xA or divide-by-4. The modulo value in the RTCMOD register is set to 0x55. When the counter, RTCCNT, reaches the modulo value of 0x55, the counter overflows to 0x00 and continues counting. The real-time interrupt flag, RTIF, sets when the counter value changes from 0x55 to 0x00. A real-time interrupt is generated when RTIF is set, if RTIE is set.

15.5 Initialization/Application Information

This section provides example code to give some basic direction to a user on how to initialize and configure the RTC module. The example software is implemented in C language.

The example below shows how to implement time of day with the RTC using the 1-kHz clock source to achieve the lowest possible power consumption. Because the 1-kHz clock source is not as accurate as a crystal, software can be added for any adjustments. For accuracy without adjustments at the expense of additional power consumption, the external clock (ERCLK) or the internal clock (IRCLK) can be selected with appropriate prescaler and modulo values.

```

/* Initialize the elapsed time counters */
Seconds = 0;
Minutes = 0;
Hours = 0;
Days=0;

/* Configure RTC to interrupt every 1 second from 1-kHz clock source */
RTCMOD.byte = 0x00;
RTCSC.byte = 0x1F;

/*****
Function Name : RTC_ISR
Notes : Interrupt service routine for RTC module.
*****/

```

16.1.1 Features

The TPM includes these distinctive features:

- One to eight channels:
 - Each channel may be input capture, output compare, or edge-aligned PWM
 - Rising-Edge, falling-edge, or any-edge input capture trigger
 - Set, clear, or toggle output compare action
 - Selectable polarity on PWM outputs
- Module may be configured for buffered, center-aligned pulse-width-modulation (CPWM) on all channels
- Timer clock source selectable as prescaled bus clock, fixed system clock, or an external clock pin
 - Prescale taps for divide-by 1, 2, 4, 8, 16, 32, 64, or 128
 - Fixed system clock source are synchronized to the bus clock by an on-chip synchronization circuit
 - External clock pin may be shared with any timer channel pin or a separated input pin
- 16-bit free-running or modulo up/down count operation
- Timer system enable
- One interrupt per channel plus terminal count interrupt

16.1.2 Modes of Operation

In general, TPM channels may be independently configured to operate in input capture, output compare, or edge-aligned PWM modes. A control bit allows the whole TPM (all channels) to switch to center-aligned PWM mode. When center-aligned PWM mode is selected, input capture, output compare, and edge-aligned PWM functions are not available on any channels of this TPM module.

When the microcontroller is in active BDM background or BDM foreground mode, the TPM temporarily suspends all counting until the microcontroller returns to normal user operating mode. During stop mode, all system clocks, including the main oscillator, are stopped; therefore, the TPM is effectively disabled until clocks resume. During wait mode, the TPM continues to operate normally. Provided the TPM does not need to produce a real time reference or provide the interrupt source(s) needed to wake the MCU from wait mode, the user can save power by disabling TPM functions before entering wait mode.

- Input capture mode

When a selected edge event occurs on the associated MCU pin, the current value of the 16-bit timer counter is captured into the channel value register and an interrupt flag bit is set. Rising edges, falling edges, any edge, or no edge (disable channel) may be selected as the active edge which triggers the input capture.
- Output compare mode

When the value in the timer counter register matches the channel value register, an interrupt flag bit is set, and a selected output action is forced on the associated MCU pin. The output compare action may be selected to force the pin to zero, force the pin to one, toggle the pin, or ignore the pin (used for software timing functions).

When a channel is configured for edge-aligned PWM (CPWMS=0, MSnB=1 and ELSnB:ELSnA not = 0:0), the data direction is overridden, the TPMxCHn pin is forced to be an output controlled by the TPM, and ELSnA controls the polarity of the PWM output signal on the pin. When ELSnB:ELSnA=1:0, the TPMxCHn pin is forced high at the start of each new period (TPMxCNT=0x0000), and the pin is forced low when the channel value register matches the timer counter. When ELSnA=1, the TPMxCHn pin is forced low at the start of each new period (TPMxCNT=0x0000), and the pin is forced high when the channel value register matches the timer counter.

TPMxMODH:TPMxMODL = 0x0008
 TPMxCnVH:TPMxCnVL = 0x0005

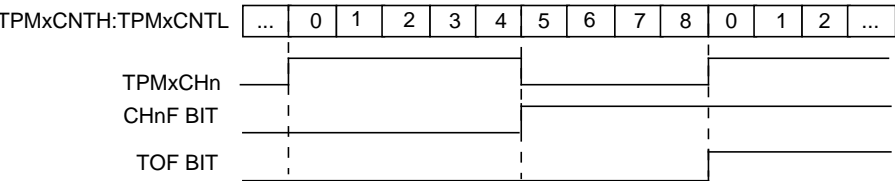


Figure 16-3. High-True Pulse of an Edge-Aligned PWM

TPMxMODH:TPMxMODL = 0x0008
 TPMxCnVH:TPMxCnVL = 0x0005

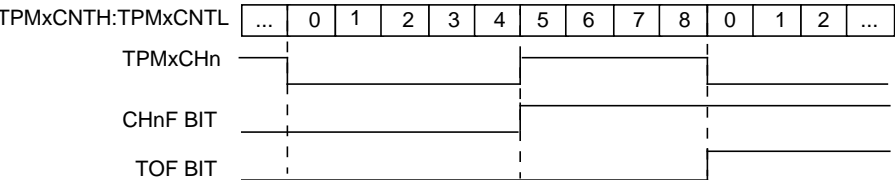


Figure 16-4. Low-True Pulse of an Edge-Aligned PWM

16.4.1.3 Counting Modes

The main timer counter has two counting modes. When center-aligned PWM is selected (CPWMS=1), the counter operates in up/down counting mode. Otherwise, the counter operates as a simple up counter. As an up counter, the timer counter counts from 0x0000 through its terminal count and then continues with 0x0000. The terminal count is 0xFFFF or a modulus value in TPMxMODH:TPMxMODL.

When center-aligned PWM operation is specified, the counter counts up from 0x0000 through its terminal count and then down to 0x0000 where it changes back to up counting. Both 0x0000 and the terminal count value are normal length counts (one timer clock period long). In this mode, the timer overflow flag (TOF) becomes set at the end of the terminal-count period (as the count changes to the next lower count value).

16.4.1.4 Manual Counter Reset

The main timer counter can be manually reset at any time by writing any value to either half of TPMxCNTH or TPMxCNTL. Resetting the counter in this manner also resets the coherency mechanism in case only half of the counter was read before resetting the count.

16.4.2 Channel Mode Selection

Provided CPWMS=0, the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and edge-aligned PWM.

16.4.2.1 Input Capture Mode

With the input-capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input-capture channel, the TPM latches the contents of the TPM counter into the channel-value registers (TPMxCnVH:TPMxCnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

In input capture mode, the TPMxCnVH and TPMxCnVL registers are read only.

When either half of the 16-bit capture register is read, the other half is latched into a buffer to support coherent 16-bit accesses in big-endian or little-endian order. The coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

An input capture event sets a flag bit (CHnF) which may optionally generate a CPU interrupt request.

While in BDM, the input capture function works as configured by the user. When an external event occurs, the TPM latches the contents of the TPM counter (which is frozen because of the BDM mode) into the channel value registers and sets the flag bit.

16.4.2.2 Output Compare Mode

With the output-compare function, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter reaches the value in the channel-value registers of an output-compare channel, the TPM can set, clear, or toggle the channel pin.

17.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode, if BDC enabled
- COP watchdog disabled while in active background mode

Features of the ICE system include:

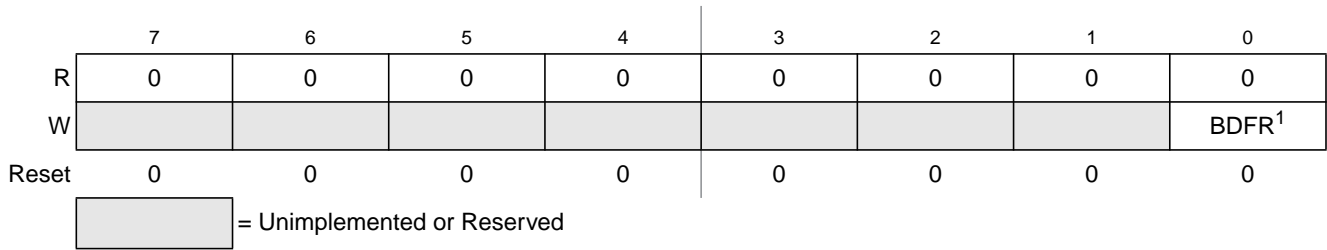
- Two trigger comparators: Two address + read/write (R/W) or one full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
 - Change-of-flow addresses or
 - Event-only data
- Two types of breakpoints:
 - Tag breakpoints for instruction opcodes
 - Force breakpoints for any address access
- Nine trigger modes:
 - Basic: A-only, A OR B
 - Sequence: A then B
 - Full: A AND B data, A AND NOT B data
 - Event (store data): Event-only B, A then event-only B
 - Range: Inside range ($A \leq \text{address} \leq B$), outside range ($\text{address} < A$ or $\text{address} > B$)

17.2 Background Debug Controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

- Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be read or written, and allow the user to trace one user instruction at a time, or GO to the user program from active background mode.



¹ BDFR is writable only through serial background mode debug commands, not from user programs.

Figure 17-6. System Background Debug Force Reset Register (SBDFR)

Table 17-3. SBDFR Register Field Description

| Field | Description |
|-----------|---|
| 0 BDFR | Background Debug Force Reset — A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program. |

17.4.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

17.4.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

Freescall-provided equate or header file is used to translate these names into the appropriate absolute addresses.

B.2.1 Timer Status and Control Register (TPMxSC)

TPMxSC contains the overflow status flag and control bits that are used to configure the interrupt enable, TPM configuration, clock source, and prescale divisor. These controls relate to all channels within this timer module.

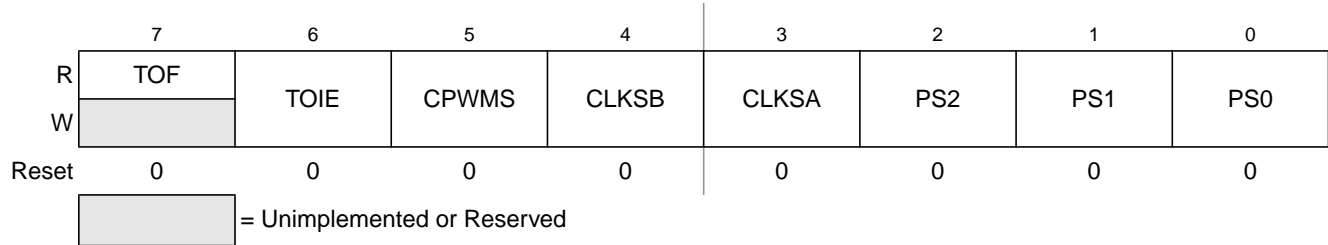


Figure B-2. Timer Status and Control Register (TPMxSC)

Table B-1. TPMxSC Register Field Descriptions

| Field | Description |
|------------------|--|
| 7 TOF | Timer Overflow Flag — This flag is set when the TPM counter changes to 0x0000 after reaching the modulo value programmed in the TPM counter modulo registers. When the TPM is configured for CPWM, TOF is set after the counter has reached the value in the modulo register, at the transition to the next lower count value. Clear TOF by reading the TPM status and control register when TOF is set and then writing a 0 to TOF. If another TPM overflow occurs before the clearing sequence is complete, the sequence is reset so TOF would remain set after the clear sequence was completed for the earlier TOF. Reset clears TOF. Writing a 1 to TOF has no effect. 0 TPM counter has not reached modulo value or overflow 1 TPM counter has overflowed |
| 6 TOIE | Timer Overflow Interrupt Enable — This read/write bit enables TPM overflow interrupts. If TOIE is set, an interrupt is generated when TOF equals 1. Reset clears TOIE. 0 TOF interrupts inhibited (use software polling) 1 TOF interrupts enabled |
| 5 CPWMS | Center-Aligned PWM Select — This read/write bit selects CPWM operating mode. Reset clears this bit so the TPM operates in up-counting mode for input capture, output compare, and edge-aligned PWM functions. Setting CPWMS reconfigures the TPM to operate in up-/down-counting mode for CPWM functions. Reset clears CPWMS. 0 All TPMx channels operate as input capture, output compare, or edge-aligned PWM mode as selected by the MSnB:MSnA control bits in each channel's status and control register 1 All TPMx channels operate in center-aligned PWM mode |
| 4:3 CLKS[B:A] | Clock Source Select — As shown in Table B-2 , this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The external source and the XCLK are synchronized to the bus clock by an on-chip synchronization circuit. |
| 2:0 PS[2:0] | Prescale Divisor Select — This 3-bit field selects one of eight divisors for the TPM clock input as shown in Table B-3 . This prescaler is located after any clock source synchronization or clock source selection, so it affects whatever clock source is selected to drive the TPM system. |

Table B-2. TPM Clock Source Selection

| CLKSB:CLKSA | TPM Clock Source to Prescaler Input |
|-------------|--|
| 0:0 | No clock selected (TPMx disabled) |
| 0:1 | Bus rate clock (BUSCLK) |
| 1:0 | Fixed system clock (XCLK) |
| 1:1 | External source (TPMxCLK) ^{1,2} |

¹ The maximum frequency that is allowed as an external clock is one-fourth of the bus frequency.

² If the external clock input is shared with channel n and is selected as the TPM clock source, the corresponding ELSnB:ELSnA control bits should be set to 0:0 so channel n does not try to use the same pin for a conflicting function.

Table B-3. Prescale Divisor Selection

| PS2:PS1:PS0 | TPM Clock Source Divided-By |
|-------------|-----------------------------|
| 0:0:0 | 1 |
| 0:0:1 | 2 |
| 0:1:0 | 4 |
| 0:1:1 | 8 |
| 1:0:0 | 16 |
| 1:0:1 | 32 |
| 1:1:0 | 64 |
| 1:1:1 | 128 |

B.2.2 Timer Counter Registers (TPMxCNTH:TPMxCNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPMxCNTH or TPMxCNTL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This allows coherent 16-bit reads in either order. The coherency mechanism is automatically restarted by an MCU reset, a write of any value to TPMxCNTH or TPMxCNTL, or any write to the timer status/control register (TPMxSC).

Reset clears the TPM counter registers.

| | | | | | | | | |
|-------|--|----|----|----|----|----|---|-------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| W | Any write to TPMxCNTH clears the 16-bit counter. | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure B-3. Timer Counter Register High (TPMxCNTH)

| | | | | | |
|---|--|--------------------|----------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | | PRINT VERSION NOT TO SCALE | |
| TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | | | DOCUMENT NO: 98ASH70029A | | REV: D |
| | | | CASE NUMBER: 873A-03 | | 19 MAY 2005 |
| | | | STANDARD: JEDEC MS-026 BBA | | |