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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08dv60f2mlf

Section Number	Title	Page
10.2	External Signal Description	176
10.2.1	Analog Power (V_{DDAD})	177
10.2.2	Analog Ground (V_{SSAD})	177
10.2.3	Voltage Reference High (V_{REFH})	177
10.2.4	Voltage Reference Low (V_{REFL})	177
10.2.5	Analog Channel Inputs (ADx)	177
10.3	Register Definition	177
10.3.1	Status and Control Register 1 (ADCSC1)	177
10.3.2	Status and Control Register 2 (ADCSC2)	179
10.3.3	Data Result High Register (ADCRH)	179
10.3.4	Data Result Low Register (ADCRL)	180
10.3.5	Compare Value High Register (ADCCVH)	180
10.3.6	Compare Value Low Register (ADCCVL)	181
10.3.7	Configuration Register (ADCCFG)	181
10.3.8	Pin Control 1 Register (APCTL1)	182
10.3.9	Pin Control 2 Register (APCTL2)	183
10.3.10	Pin Control 3 Register (APCTL3)	184
10.4	Functional Description	185
10.4.1	Clock Select and Divide Control	186
10.4.2	Input Select and Pin Control	186
10.4.3	Hardware Trigger	186
10.4.4	Conversion Control	186
10.4.5	Automatic Compare Function	189
10.4.6	MCU Wait Mode Operation	189
10.4.7	MCU Stop3 Mode Operation	190
10.4.8	MCU Stop2 Mode Operation	190
10.5	Initialization Information	191
10.5.1	ADC Module Initialization Example	191
10.6	Application Information	193
10.6.1	External Pins and Routing	193
10.6.2	Sources of Error	194

Chapter 11 Inter-Integrated Circuit (S08IICV2)

11.1	Introduction	197
11.1.1	Features	199
11.1.2	Modes of Operation	199
11.1.3	Block Diagram	200
11.2	External Signal Description	200
11.2.1	SCL — Serial Clock Line	200
11.2.2	SDA — Serial Data Line	200
11.3	Register Definition	200

Section Number	Title	Page
17.4	Register Definition	359
17.4.1	BDC Registers and Control Bits	359
17.4.2	System Background Debug Force Reset Register (SBD FR)	361
17.4.3	DBG Registers and Control Bits	362

Appendix A Electrical Characteristics

A.1	Introduction	367
A.2	Parameter Classification	367
A.3	Absolute Maximum Ratings	367
A.4	Thermal Characteristics	368
A.5	ESD Protection and Latch-Up Immunity	370
A.6	DC Characteristics	371
A.7	Supply Current Characteristics	373
A.8	Analog Comparator (ACMP) Electricals	374
A.9	ADC Characteristics	374
A.10	External Oscillator (XOSC) Characteristics	378
A.11	MCG Specifications	379
A.12	AC Characteristics	381
A.12.1	Control Timing	381
A.12.2	Timer/PWM	382
A.12.3	MSCAN	383
A.12.4	SPI	384
A.13	Flash	387
A.14	EMC Performance	387
A.14.1	Radiated Emissions	388

Appendix B Timer Pulse-Width Modulator (TPMV2)

B.0.1	Features	389
B.0.2	Block Diagram	389
B.1	External Signal Description	391
B.1.1	External TPM Clock Sources	391
B.1.2	TPMxCHn — TPMx Channel n I/O Pins	391
B.2	Register Definition	391
B.2.1	Timer Status and Control Register (TPMxSC)	392
B.2.2	Timer Counter Registers (TPMxCNTH:TPMxCNTL)	393
B.2.3	Timer Counter Modulo Registers (TPMxMODH:TPMxMODL)	394
B.2.4	Timer Channel n Status and Control Register (TPMxCnSC)	395
B.2.5	Timer Channel Value Registers (TPMxCnVH:TPMxCnVL)	396
B.3	Functional Description	397
B.3.1	Counter	397

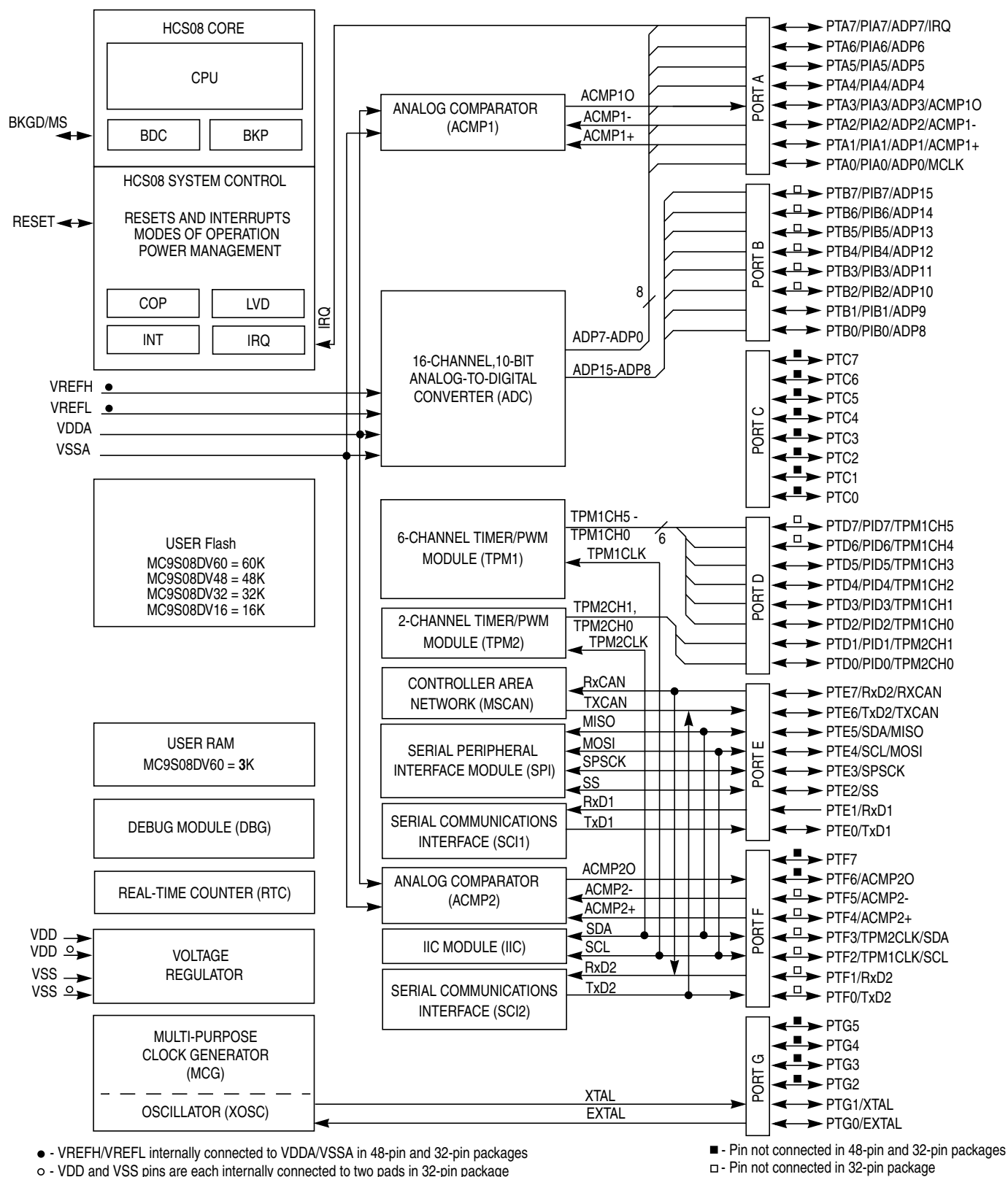


Figure 1-1. MC9S08DV60 Block Diagram

Background commands are of two types:

- Non-intrusive commands, defined as commands that can be issued while the user program is running. Non-intrusive commands can be issued through the BKGD/MS pin while the MCU is in run mode; non-intrusive commands can also be executed when the MCU is in the active background mode. Non-intrusive commands include:
 - Memory access commands
 - Memory-access-with-status commands
 - BDC register access commands
 - The BACKGROUND command
- Active background commands, which can only be executed while the MCU is in active background mode. Active background commands include commands to:
 - Read or write CPU registers
 - Trace one user program instruction at a time
 - Leave active background mode to return to the user application program (GO)

The active background mode is used to program a bootloader or user application program into the Flash program memory before the MCU is operated in run mode for the first time. When the MC9S08DV60 Series is shipped from the Freescale Semiconductor factory, the Flash program memory is erased by default unless specifically noted so there is no program that could be executed in run mode until the Flash memory is initially programmed. The active background mode can also be used to erase and reprogram the Flash memory after it has been previously programmed.

For additional information about the active background mode, refer to the [Development Support](#) chapter.

3.5 Wait Mode

Wait mode is entered by executing a WAIT instruction. Upon execution of the WAIT instruction, the CPU enters a low-power state in which it is not clocked. The I bit in CCR is cleared when the CPU enters the wait mode, enabling interrupts. When an interrupt request occurs, the CPU exits the wait mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

While the MCU is in wait mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available when the MCU is in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from wait mode and enter active background mode.

Table 4-2. Direct-Page Register Summary (Sheet 2 of 3)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x0028	TPM1C1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
0x0029	TPM1C1VH	Bit 15	14	13	12	11	10	9	Bit 8
0x002A	TPM1C1VL	Bit 7	6	5	4	3	2	1	Bit 0
0x002B	TPM1C2SC	CH2F	CH2IE	MS2B	MS2A	ELS2B	ELS2A	0	0
0x002C	TPM1C2VH	Bit 15	14	13	12	11	10	9	Bit 8
0x002D	TPM1C2VL	Bit 7	6	5	4	3	2	1	Bit 0
0x002E	TPM1C3SC	CH3F	CH3IE	MS3B	MS3A	ELS3B	ELS3A	0	0
0x002F	TPM1C3VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0030	TPM1C3VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0031	TPM1C4SC	CH4F	CH4IE	MS4B	MS4A	ELS4B	ELS4A	0	0
0x0032	TPM1C4VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0033	TPM1C4VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0034	TPM1C5SC	CH5F	CH5IE	MS5B	MS5A	ELS5B	ELS5A	0	0
0x0035	TPM1C5VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0036	TPM1C5VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0037	Reserved	—	—	—	—	—	—	—	—
0x0038	SCI1BDH	LBKDIE	RXEDGIE	0	SBR12	SBR11	SBR10	SBR9	SBR8
0x0039	SCI1BDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x003A	SCI1C1	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x003B	SCI1C2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x003C	SCI1S1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x003D	SCI1S2	LBKDIF	RXEDGIF	0	RXINV	RWUID	BRK13	LBKDE	RAF
0x003E	SCI1C3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
0x003F	SCI1D	Bit 7	6	5	4	3	2	1	Bit 0
0x0040	SCI2BDH	LBKDIE	RXEDGIE	0	SBR12	SBR11	SBR10	SBR9	SBR8
0x0041	SCI2BDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x0042	SCI2C1	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x0043	SCI2C2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x0044	SCI2S1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x0045	SCI2S2	LBKDIF	RXEDGIF	0	RXINV	RWUID	BRK13	LBKDE	RAF
0x0046	SCI2C3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
0x0047	SCI2D	Bit 7	6	5	4	3	2	1	Bit 0
0x0048	MCGC1	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
0x0049	MCGC2	BDIV		RANGE	HGO	LP	EREFS	ERCLKEN	EREFTEN
0x004A	MCGTRM	TRIM							
0x004B	MCGSC	LOLS	LOCK	PLLST	IREFST	CLKST		OSCINIT	FTRIM
0x004C	MCGC3	LOLIE	PLLS	CME	0	VDIV			
0x004D– 0x004F	Reserved	—	—	—	—	—	—	—	—

5.8.1 Interrupt Pin Request Status and Control Register (IRQSC)

This direct page register includes status and control bits which are used to configure the IRQ function, report status, and acknowledge IRQ events.

	7	6	5	4	3	2	1	0
R	0	IRQPDD	IRQEDG	IRQPE	IRQF	0	IRQIE	IRQMOD
W						IRQACK		
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-2. Interrupt Request Status and Control Register (IRQSC)

Table 5-2. IRQSC Register Field Descriptions

Field	Description
6 IRQPDD	Interrupt Request (IRQ) Pull Device Disable — This read/write control bit is used to disable the internal pull-up/pull-down device when the IRQ pin is enabled (IRQPE = 1) allowing for an external device to be used. 0 IRQ pull device enabled if IRQPE = 1. 1 IRQ pull device disabled if IRQPE = 1.
5 IRQEDG	Interrupt Request (IRQ) Edge Select — This read/write control bit is used to select the polarity of edges or levels on the IRQ pin that cause IRQF to be set. The IRQMOD control bit determines whether the IRQ pin is sensitive to both edges and levels or only edges. When the IRQ pin is enabled as the IRQ input and is configured to detect rising edges, it has a pull-down. When the IRQ pin is enabled as the IRQ input and is configured to detect falling edges, it has a pull-up. 0 IRQ is falling edge or falling edge/low-level sensitive. 1 IRQ is rising edge or rising edge/high-level sensitive.
4 IRQPE	IRQ Pin Enable — This read/write control bit enables the IRQ pin function. When this bit is set the IRQ pin can be used as an interrupt request. 0 IRQ pin function is disabled. 1 IRQ pin function is enabled.
3 IRQF	IRQ Flag — This read-only status bit indicates when an interrupt request event has occurred. 0 No IRQ request. 1 IRQ event detected.
2 IRQACK	IRQ Acknowledge — This write-only bit is used to acknowledge interrupt request events (write 1 to clear IRQF). Writing 0 has no meaning or effect. Reads always return 0. If edge-and-level detection is selected (IRQMOD = 1), IRQF cannot be cleared while the IRQ pin remains at its asserted level.
1 IRQIE	IRQ Interrupt Enable — This read/write control bit determines whether IRQ events generate an interrupt request. 0 Interrupt request when IRQF set is disabled (use polling). 1 Interrupt requested whenever IRQF = 1.
0 IRQMOD	IRQ Detection Mode — This read/write control bit selects either edge-only detection or edge-and-level detection. The IRQEDG control bit determines the polarity of edges and levels that are detected as interrupt request events. See Section 5.5.2.2, “Edge and Level Sensitivity” for more details. 0 IRQ event on falling edges or rising edges only. 1 IRQ event on falling edges and low levels or on rising edges and high levels.

6.5.4 Port D Registers

Port D is controlled by the registers listed below.

6.5.4.1 Port D Data Register (PTDD)

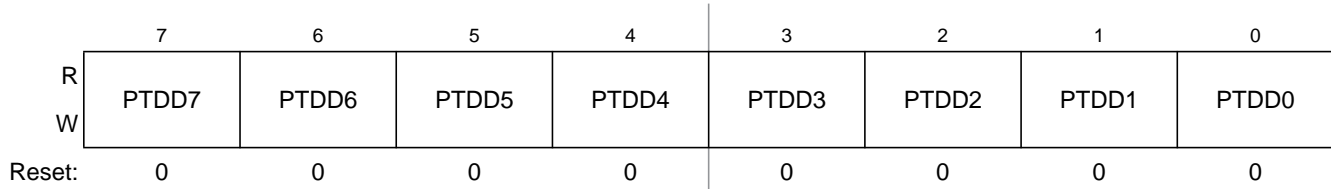


Figure 6-24. Port D Data Register (PTDD)

Table 6-22. PTDD Register Field Descriptions

Field	Description
7:0 PTDD[7:0]	Port D Data Register Bits — For port D pins that are inputs, reads return the logic level on the pin. For port D pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port D pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTDD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups/pull-downs disabled.

6.5.4.2 Port D Data Direction Register (PTDDD)

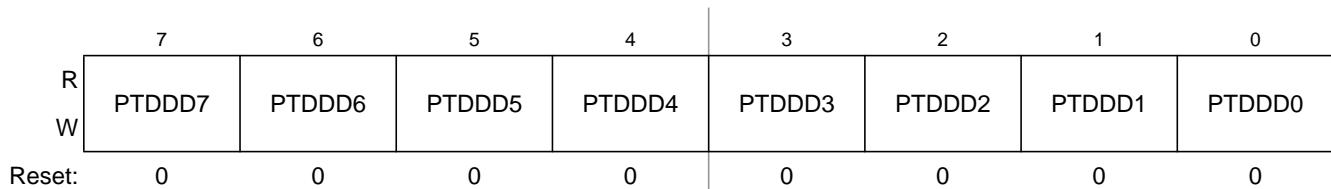


Figure 6-25. Port D Data Direction Register (PTDDD)

Table 6-23. PTDDD Register Field Descriptions

Field	Description
7:0 PTDDD[7:0]	Data Direction for Port D Bits — These read/write bits control the direction of port D pins and what is read for PTDD reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port D bit n and PTDD reads return the contents of PTDDn.

8.1.1 Features

Key features of the MCG module are:

- Frequency-locked loop (FLL)
 - 0.2% resolution using internal 32-kHz reference
 - 2% deviation over voltage and temperature using internal 32-kHz reference
 - Internal or external reference can be used to control the FLL
- Phase-locked loop (PLL)
 - Voltage-controlled oscillator (VCO)
 - Modulo VCO frequency divider
 - Phase/Frequency detector
 - Integrated loop filter
 - Lock detector with interrupt capability
- Internal reference clock
 - Nine trim bits for accuracy
 - Can be selected as the clock source for the MCU
- External reference clock
 - Control for external oscillator
 - Clock monitor with reset capability
 - Can be selected as the clock source for the MCU
- Reference divider is provided
- Clock source selected can be divided down by 1, 2, 4, or 8
- BDC clock (MCGLCLK) is provided as a constant divide by 2 of the DCO output whether in an FLL or PLL mode.

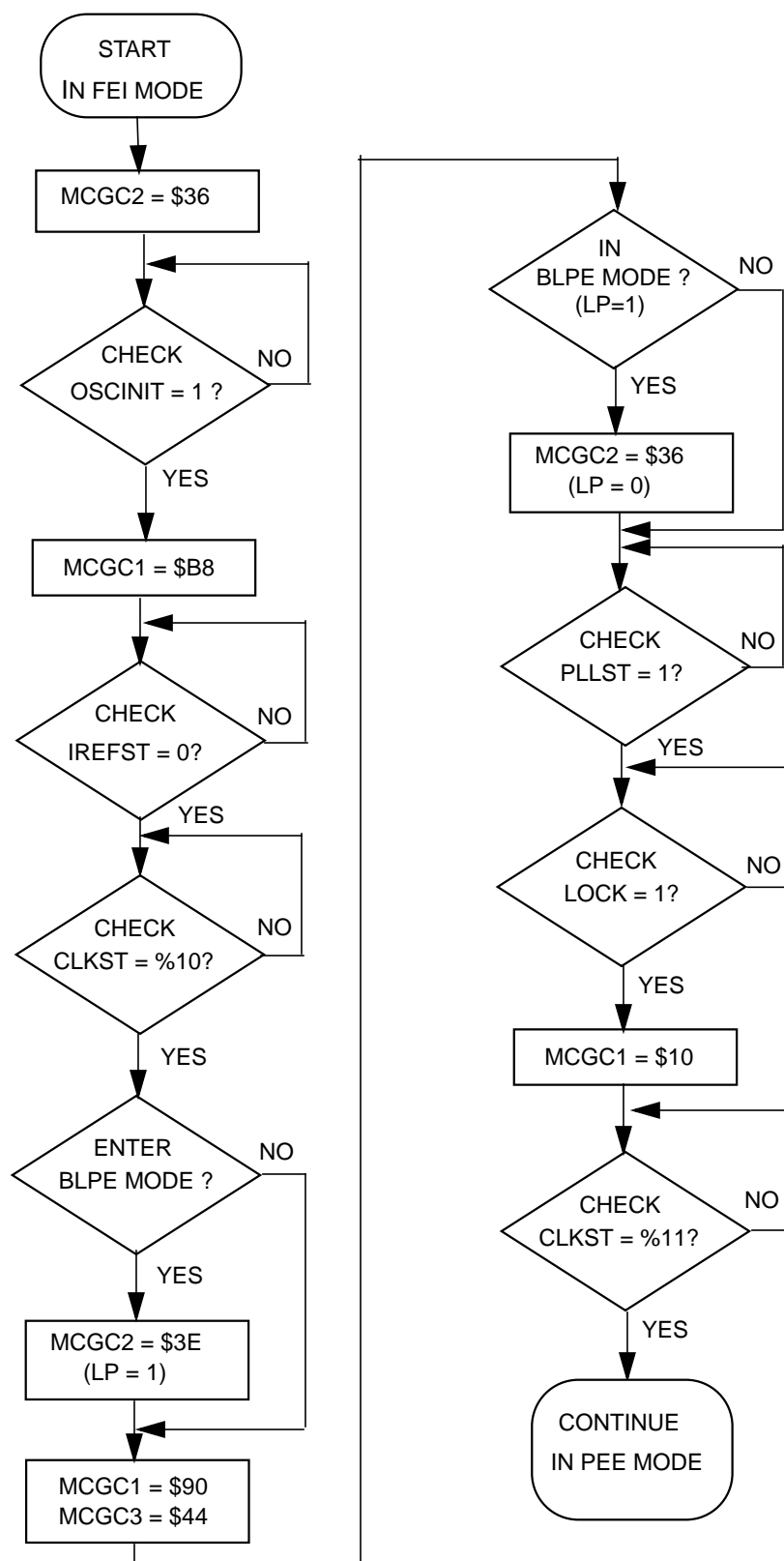


Figure 8-9. Flowchart of FEI to PEE Mode Transition using a 4 MHz crystal

9.1.2 Features

The ACMP has the following features:

- Full rail to rail supply operation.
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output.
- Option to compare to fixed internal bandgap reference voltage.
- Option to allow comparator output to be visible on a pin, ACMPxO.

9.1.3 Modes of Operation

This section defines the ACMP operation in wait, stop, and background debug modes.

9.1.3.1 ACMP in Wait Mode

The ACMP continues to run in wait mode if enabled before executing the appropriate instruction. Therefore, the ACMP can be used to bring the MCU out of wait mode if the ACMP interrupt is enabled (ACIE is set). For lowest possible current consumption, the ACMP should be disabled by software if not required as an interrupt source during wait mode.

9.1.3.2 ACMP in Stop Modes

The ACMP is disabled in all stop modes, regardless of the settings before executing the stop instruction. Therefore, the ACMP cannot be used as a wake up source from stop modes.

During stop2 mode, the ACMP module is fully powered down. Upon wake-up from stop2 mode, the ACMP module is in the reset state.

During stop3 mode, clocks to the ACMP module are halted. No registers are affected. In addition, the ACMP comparator circuit enters a low-power state. No compare operation occurs while in stop3.

If stop3 is exited with a reset, the ACMP is put into its reset state. If stop3 is exited with an interrupt, the ACMP continues from the state it was in when stop3 was entered.

9.1.3.3 ACMP in Active Background Mode

When the microcontroller is in active background mode, the ACMP continues to operate normally.

Chapter 11

Inter-Integrated Circuit (S08IICV2)

11.1 Introduction

The inter-integrated circuit (IIC) provides a method of communication between a number of devices. The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

All MC9S08DV60 Series MCUs feature the IIC, as shown in the following block diagram.

NOTE

Drive strength must be disabled (DSE=0) for the IIC pins when using the IIC module for correct operation.

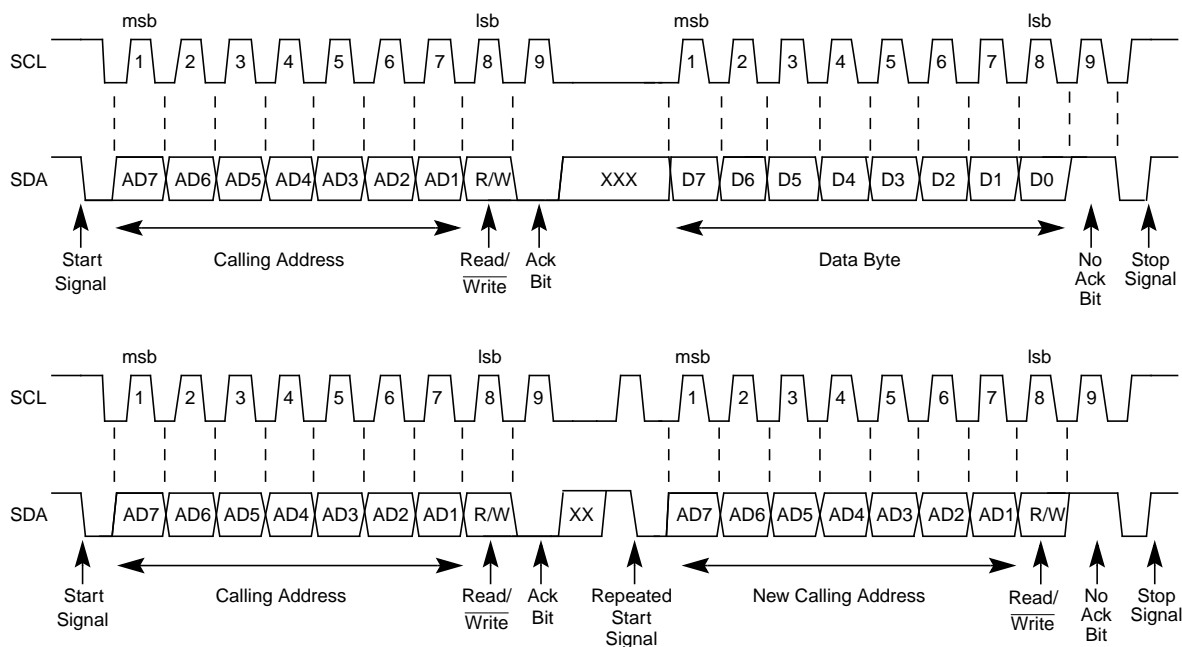


Figure 11-9. IIC Bus Transmission Signals

11.4.1.1 Start Signal

When the bus is free, no master device is engaging the bus (SCL and SDA lines are at logical high), a master may initiate communication by sending a start signal. As shown in Figure 11-9, a start signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and brings all slaves out of their idle states.

11.4.1.2 Slave Address Transmission

The first byte of data transferred immediately after the start signal is the slave address transmitted by the master. This is a seven-bit calling address followed by a R/\overline{W} bit. The R/\overline{W} bit tells the slave the desired direction of data transfer.

- 1 = Read transfer, the slave transmits data to the master.
- 0 = Write transfer, the master transmits data to the slave.

Only the slave with a calling address that matches the one transmitted by the master responds by sending back an acknowledge bit. This is done by pulling the SDA low at the ninth clock (see Figure 11-9).

No two slaves in the system may have the same address. If the IIC module is the master, it must not transmit an address equal to its own slave address. The IIC cannot be master and slave at the same time. However, if arbitration is lost during an address cycle, the IIC reverts to slave mode and operates correctly even if it is being addressed by another master.

12.1.3 Block Diagram

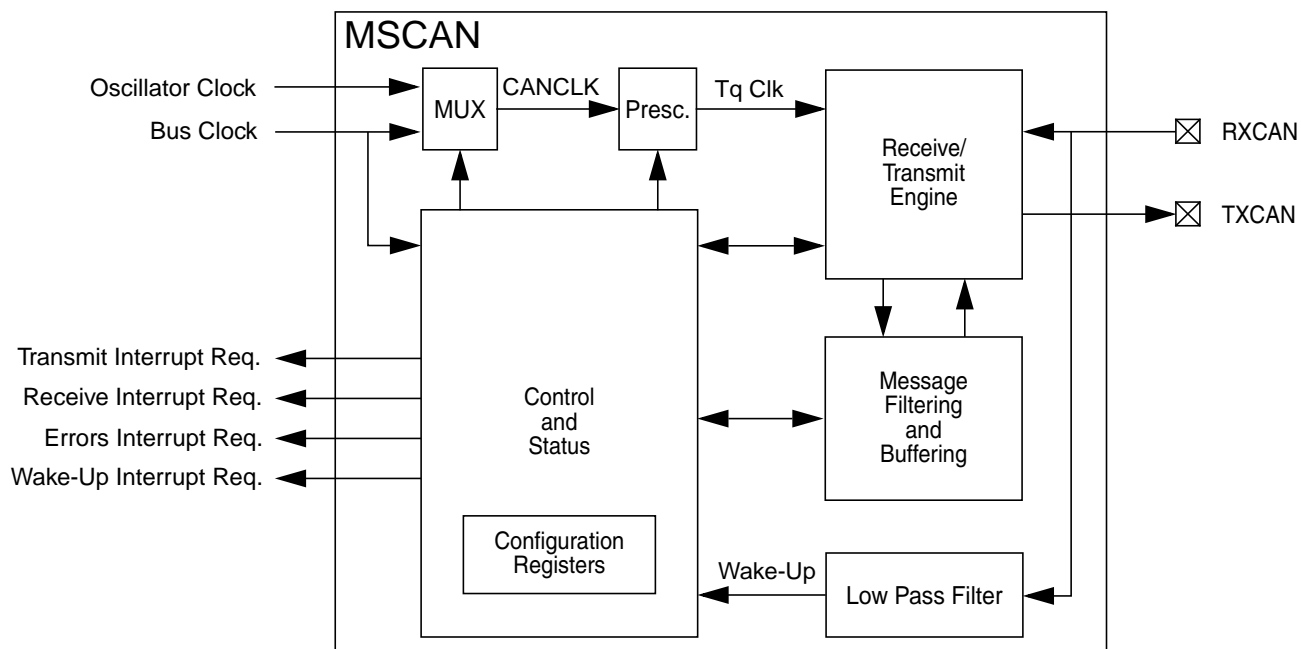


Figure 12-2. MSCAN Block Diagram

12.2 External Signal Description

The MSCAN uses two external pins:

12.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

12.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

- 0 = Dominant state
- 1 = Recessive state

12.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 12-3. Each CAN node is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective nodes.

12.3.9 MSCAN Transmitter Message Abort Acknowledge Register (CANTAACK)

The CANTAACK register indicates the successful abort of messages queued for transmission, if requested by the appropriate bits in the CANTARQ register.

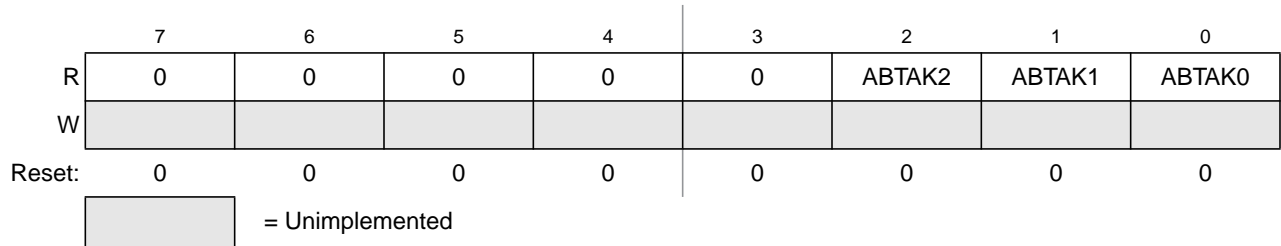


Figure 12-13. MSCAN Transmitter Message Abort Acknowledge Register (CANTAACK)

NOTE

The CANTAACK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Read: Anytime

Write: Unimplemented for ABTAKx flags

Table 12-14. CANTAACK Register Field Descriptions

Field	Description
2:0 ABTAK[2:0]	Abort Acknowledge — This flag acknowledges that a message was aborted due to a pending transmission abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

12.3.10 MSCAN Transmit Buffer Selection Register (CANTBSEL)

The CANTBSEL selections of the actual transmit message buffer, which is accessible in the CANTXFG register space.

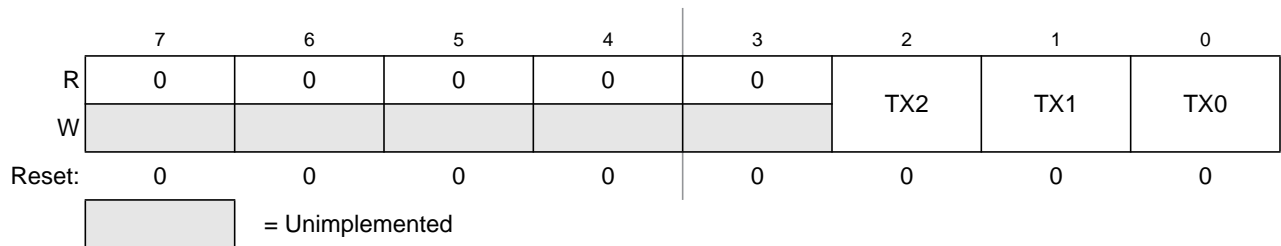


Figure 12-14. MSCAN Transmit Buffer Selection Register (CANTBSEL)

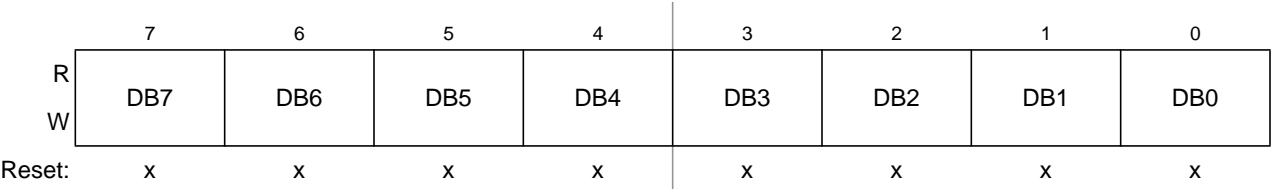


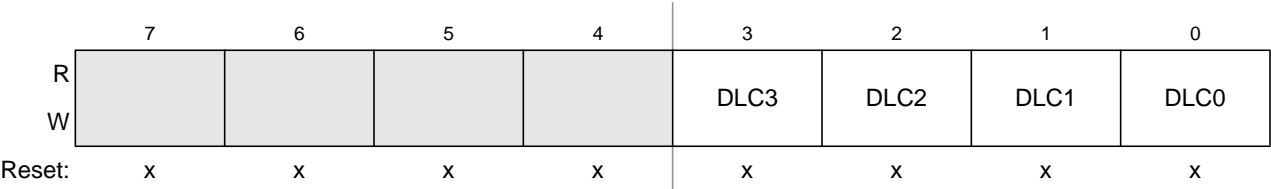
Figure 12-33. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 12-31. DSR0–DSR7 Register Field Descriptions

Field	Description
7:0 DB[7:0]	Data bits 7:0

12.4.4 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.




 = Unused; always read “x”

Figure 12-34. Data Length Register (DLR) — Extended Identifier Mapping

Table 12-32. DLR Register Field Descriptions

Field	Description
3:0 DLC[3:0]	Data Length Code Bits — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 12-33 shows the effect of setting the DLC bits.

in LSBFE. Both variations of SPSCCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The \overline{SS} OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master \overline{SS} output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCCK cycle after the end of the eighth bit time of the transfer. The \overline{SS} IN waveform applies to the slave select input of a slave.

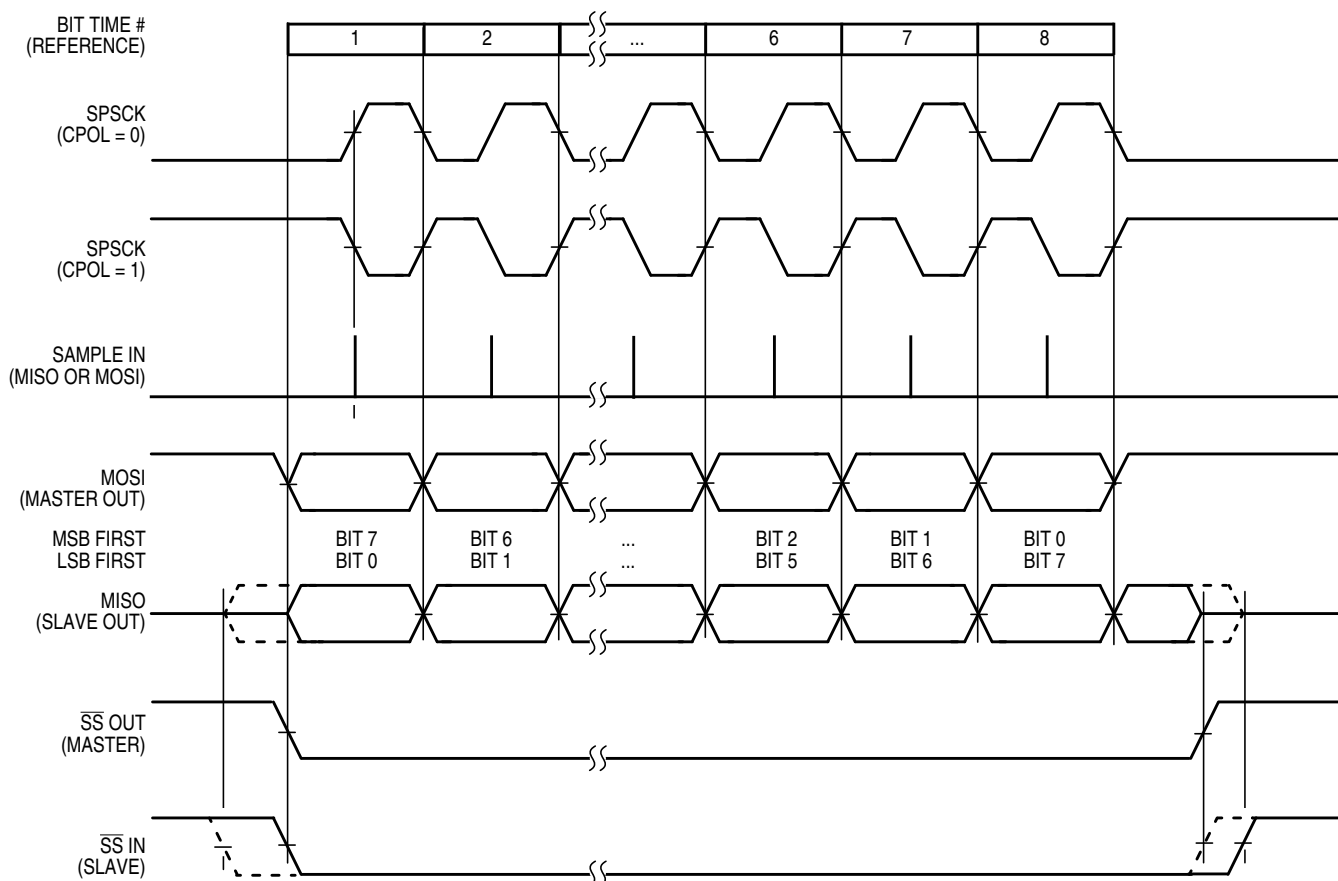


Figure 13-11. SPI Clock Formats (CPHA = 0)

When CPHA = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when \overline{SS} goes to active low. The first SPSCCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 0, the slave's \overline{SS} input must go to its inactive high level between transfers.

14.1.4 Block Diagram

Figure 14-2 shows the transmitter portion of the SCI.

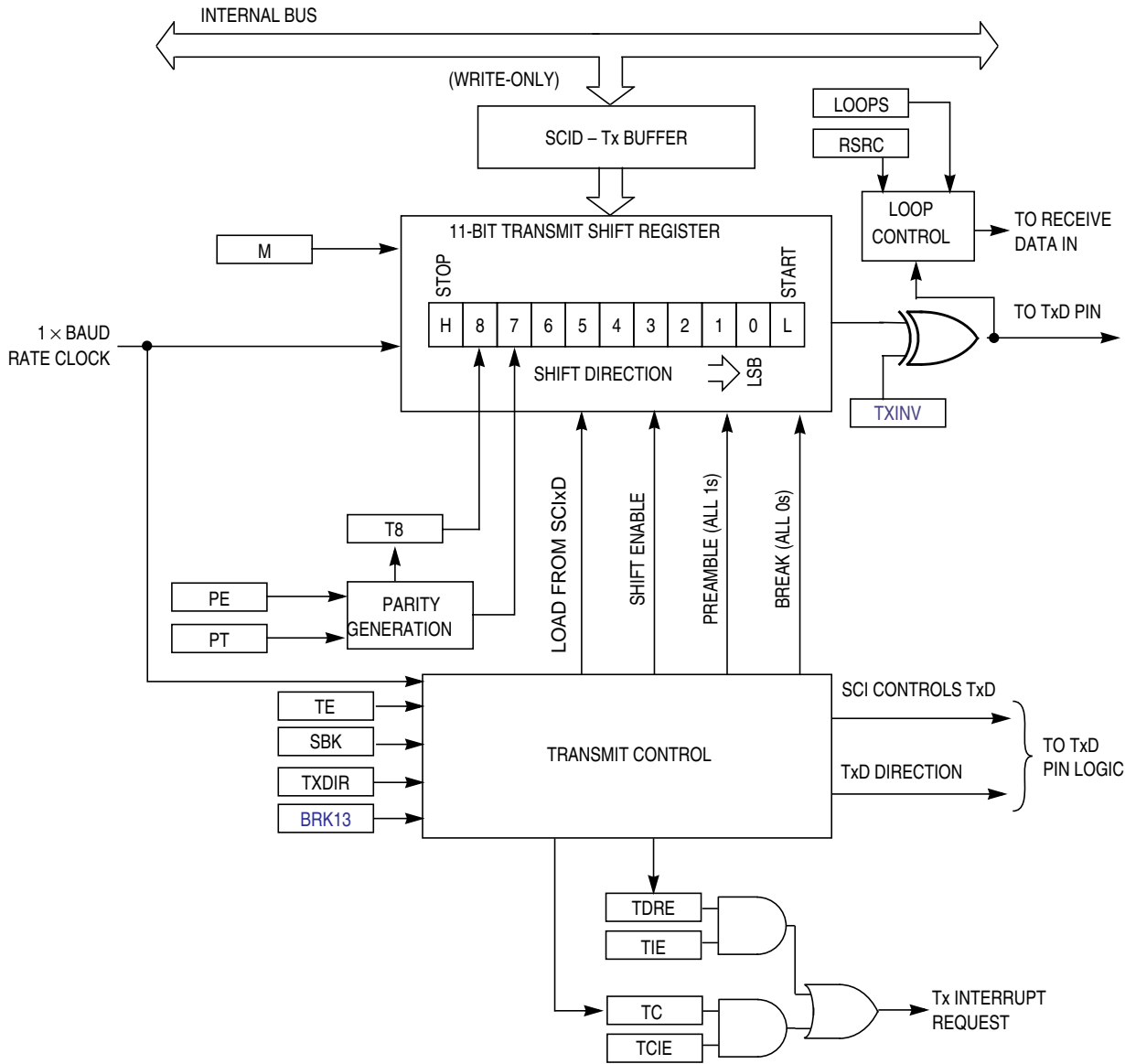


Figure 14-2. SCI Transmitter Block Diagram

15.1.4 Block Diagram

The block diagram for the RTC module is shown in Figure 15-2.

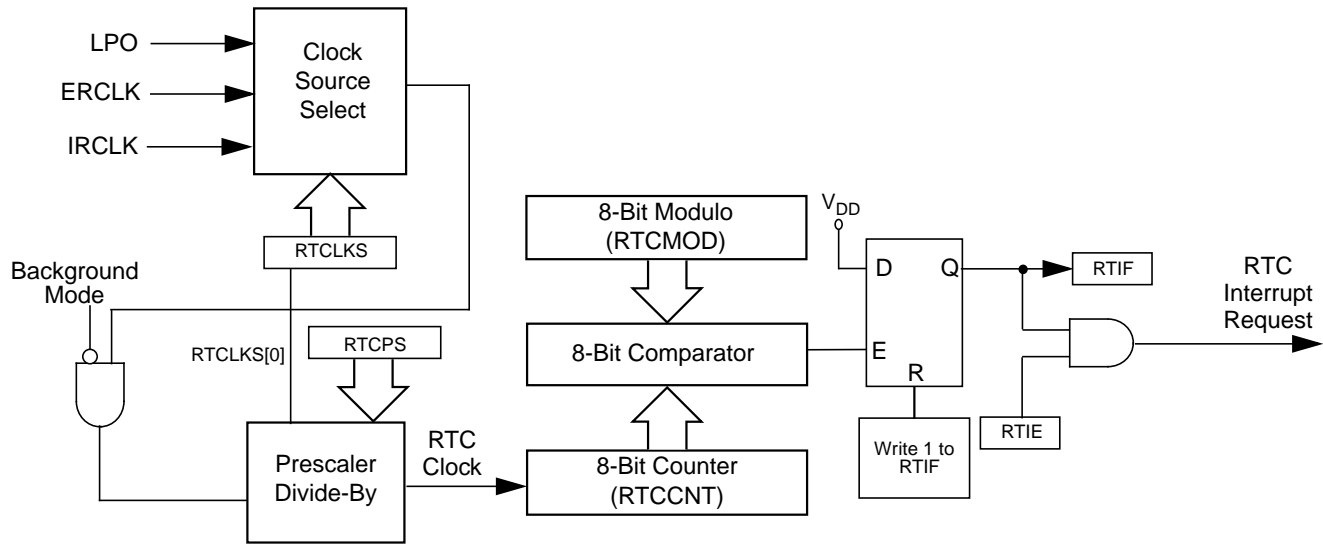


Figure 15-2. Real-Time Counter (RTC) Block Diagram

15.2 External Signal Description

The RTC does not include any off-chip signals.

15.3 Register Definition

The RTC includes a status and control register, an 8-bit counter register, and an 8-bit modulo register.

Refer to the direct-page register summary in the memory section of this document for the absolute address assignments for all RTC registers. This section refers to registers and control bits only by their names and relative address offsets.

Table 15-1 is a summary of RTC registers.

Table 15-1. RTC Register Summary

Name		7	6	5	4	3	2	1	0
RTCSC	R	RTIF	RTCLKS		RTIE	RTCPS			
	W								
RTCCNT	R	RTCCNT							
	W								
RTCMOD	R	RTCMOD							
	W								

Chapter 17

Development Support

17.1 Introduction

Development support systems in the HCS08 include the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip Flash and other nonvolatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the target MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

17.1.1 Forcing Active Background

The method for forcing active background mode depends on the specific HCS08 derivative. For the MC9S08DV60, you can force active background after a power-on reset by holding the BKGD pin low as the device exits the reset condition. You can also force active background by driving BKGD low immediately after a serial background command that writes a one to the BDFR bit in the SBDIFR register. If no debug pod is connected to the BKGD pin, the MCU will always reset into normal operating mode.

A.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table A-6. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit	
1	—	Operating Voltage	V _{DD}		2.7	—	5.5	V	
2	P	All I/O pins, low-drive strength	V _{OH}	5 V, I _{Load} = −2 mA	V _{DD} − 1.5	—	—	V	
	C			3 V, I _{Load} = −0.6 mA	V _{DD} − 1.5	—	—		
	C			Output high voltage	5 V, I _{Load} = −0.4 mA	V _{DD} − 0.8	—		—
	C			3 V, I _{Load} = −0.24 mA	V _{DD} − 0.8	—	—		
	P	All I/O pins, high-drive strength		5 V, I _{Load} = −10 mA	V _{DD} − 1.5	—	—		
	C			3 V, I _{Load} = −3 mA	V _{DD} − 1.5	—	—		
	C			5 V, I _{Load} = −2 mA	V _{DD} − 0.8	—	—		
	C			3 V, I _{Load} = −0.4 mA	V _{DD} − 0.8	—	—		
3	C	Output high current Max total I _{OH} for all ports	I _{OHT}	5 V	0	—	-100	mA	
				3 V	0	—	-60		
4	P	All I/O pins, low-drive strength	V _{OL}	5 V, I _{Load} = 2 mA	—	—	1.5	V	
	C			3 V, I _{Load} = 0.6 mA	—	—	1.5		
	C			Output low voltage	5 V, I _{Load} = 0.4 mA	—	—		0.8
	C			3 V, I _{Load} = 0.24 mA	—	—	0.8		
	P	All I/O pins, high-drive strength		5 V, I _{Load} = 10 mA	—	—	1.5		
	C			3 V, I _{Load} = 3 mA	—	—	1.5		
	C			5 V, I _{Load} = 2 mA	—	—	0.8		
	C			3 V, I _{Load} = 0.4 mA	—	—	0.8		
5	C	Output low current Max total I _{OL} for all ports	I _{OLT}	5 V	0	—	100	mA	
				3 V	0	—	60		
6	C	Input high voltage; all digital inputs	V _{IH}	5V	0.65 x V _{DD}	—	—	V	
7	C	Input low voltage; all digital inputs	V _{IL}	5V	—	—	0.35 x V _{DD}		
8	C	Input hysteresis	V _{hys}		0.06 x V _{DD}			mV	
9	P	Input leakage current (Per pin) all input only pins	I _{In}	V _{In} = V _{DD} or V _{SS}	—	0.1	1	μA	
10	P	Hi-Z (off-state) leakage current (per pin) all input/output	I _{OZ}	V _{In} = V _{DD} or V _{SS}	—	0.1	1	μA	
11	P	Pullup resistors (or Pulldown ² resistors when enabled)	R _{PU} , R _{PD}	5 V	20	45	65	kΩ	
	C			3 V	20	45	65		
12	T	Input Capacitance, all pins	C _{In}		—	—	8	pF	
13	D	RAM retention voltage	V _{RAM}		—	0.6	1.0	V	