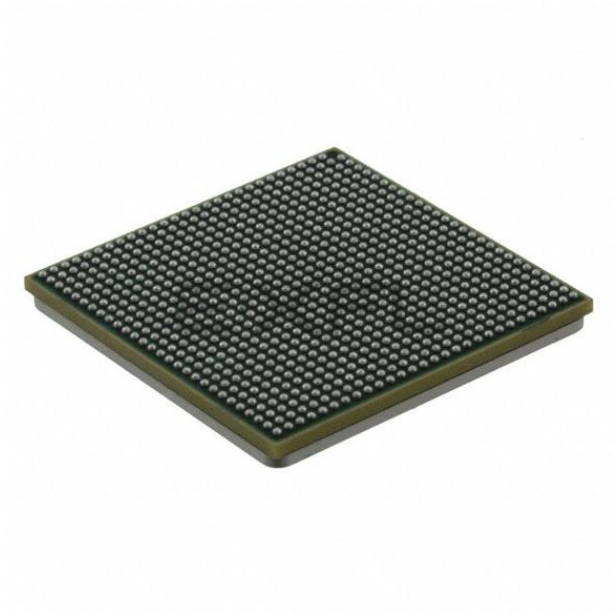

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535avjatha

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Programmable Interrupt Controller					
$\overline{\text{MCP}}$	Machine check processor	Y14	I	OV_{DD}	—
$\overline{\text{UDE}}$	Unconditional debug event	AB14	I	OV_{DD}	—
IRQ[0:8]	External interrupts	AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ[3]}}$	External interrupt/DMA request	AE13	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK[3]}}$	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE[3]}}$	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	Interrupt output	AC17	O	OV_{DD}	2,4
Ethernet Management Interface					
EC_MDC	Management data clock	Y10	O	OV_{DD}	5,9,22
EC_MDIO	Management data In/Out	Y11	I/O	OV_{DD}	—
Gigabit Reference Clock					
EC_GTX_CLK125	Reference clock	AA6	I	LV_{DD}	31
Three-Speed Ethernet Controller (Gigabit Ethernet 1)					
TSEC1_TXD[7:0]	Transmit data	AA8,AA5,Y8,Y5,W3, W5,W4,W6	O	LV_{DD}	5,9,22
TSEC1_TX_EN	Transmit Enable	W1	O	LV_{DD}	23
TSEC1_TX_ER	Transmit Error	AB5	O	LV_{DD}	5,9
TSEC1_TX_CLK	Transmit clock In	AB4	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit clock Out	W2	O	LV_{DD}	—
TSEC1_CRS	Carrier sense	AA9	I/O	LV_{DD}	17
TSEC1_COL	Collision detect	AB6	I	LV_{DD}	—
TSEC1_RXD[7:0]	Receive data	AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2	I	LV_{DD}	—
TSEC1_RX_DV	Receive data valid	AA1	I	LV_{DD}	—
TSEC1_RX_ER	Receive data error	Y9	I	LV_{DD}	—
TSEC1_RX_CLK	Receive clock	AA3	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)					
TSEC3_TXD[7:0]	Transmit data	T12,V8,U8,V9,T8,T7, T5,T6	O	TV_{DD}	5,9,22
TSEC3_TX_EN	Transmit Enable	V5	O	TV_{DD}	23
TSEC3_TX_ER	Transmit Error	U9	O	TV_{DD}	5,9

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST\_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	—	XV_{DD}	—
S2VDD	SerDes 2 core logic supply	R6,N7,M9	—	$S2V_{DD}$	—
X2VDD	SerDes 2 transceiver supply	R11,N12,L11	—	$X2V_{DD}$	—
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13	—	V_{DD_CORE}	—
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	—	V_{DD_PLAT}	—
AVDD_CORE	CPU PLL supply	AH16	—	AV_{DD_CORE}	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV_{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV_{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV_{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV_{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	—	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V_{DD_CORE}	13
SENSEVDD_PLAT	—	W17	—	V_{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13	—	—	—
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND	SerDes 1 Transceiver core logic GND (xcorevss)	M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28	—	—	—
X2GND	SerDes 2 Transceiver pad GND (xpadvss)	R12,M10,N11,L12	—	—	—
S2GND	SerDes 2 Transceiver core logic GND (xcorevss)	P8,P9,N6,M8	—	—	—
AGND_SRDS	SerDes 1 PLL GND	V27	—	—	—
AGND_SRDS2	SerDes 2 PLL GND	T2	—	—	—
SENSEVSS	GND Sensing	V16	—	—	13
Analog Signals					
MVREF	SSTL2 reference voltage	A28	Reference voltage for DDR	GVDD/2	—
SD1_IMP_CAL_RX	Rx impedance calibration	M26	—	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	Tx impedance calibration	AE28	—	100Ω (±1%) to GND	—
SD1_PLL_TPA	PLL test point analog	V26	—	AVDD_SRDS analog	18
SD2_IMP_CAL_RX	Rx impedance calibration	R7	—	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	Tx impedance calibration	L6	—	100Ω (±1%) to GND	—
SD2_PLL_TPA	PLL test point analog	T3	—	AVDD_SRDS2 analog	18
Reserved	—	R4	—	—	—
Reserved	—	R5	—	—	—
No Connect Pins					
NC	—	C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9	—	—	—

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	3
DDR3 signal	20 40 (half strength mode)	GV_{DD} = 1.5 V	2
TSEC signals	42	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I^2C	150	OV_{DD} = 3.3 V	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI1\_GNT1}}$ signal at reset.
3. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min)

2.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper chip operation. These requirements are as follows for power up:

1. V_{DD_PLAT}, V_{DD_CORE} (if POWER_EN is not used to control V_{DD_CORE}), AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD},$S2V_{DD}$, TV_{DD}, XV_{DD} and $X2V_{DD}$
2. [Wait for POWER_EN to assert], then V_{DD_CORE} (if POWER_EN is used to control V_{DD_CORE})
3. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD platform supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the chip.

During the Deep Sleep state, the VDD core supply is removed. But all other power supplies remain applied. Therefore, there is no requirement to apply the VDD core supply before any other power rails when the silicon waking from Deep Sleep.

Table 17. DDR3 SDRAM Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606MHz and 667MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
667 MHz	—	–240	240	—	3
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} =+/-(T/4 - abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR2 and DDR3 frequency is 667MHz.

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

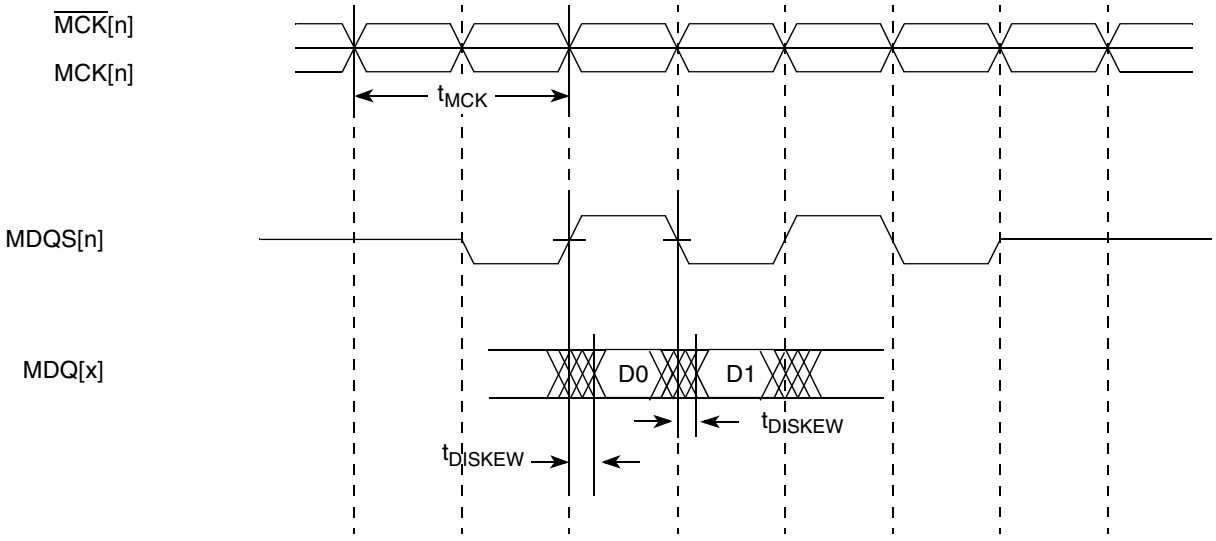

Figure 8. DDR SDRAM Input Timing Diagram

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
<= 667 MHz		$0.9 \times t_{MCK}$			7
MDQS epilogue end	t_{DDKHME}			ns	6
<= 667 MHz		$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$		7

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR2 and DDR3 frequency is 667 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

2.9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps) — FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 2.10, "Ethernet Management Interface Electrical Characteristics."

The electrical characteristics for SGMII is specified in Section 2.9.3, "SGMII Interface Electrical Characteristics." The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

2.9.1.1 GMII, MII, TBI, RGMII, RMII and RTBI DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in the following tables. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	1.90	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	3

Notes:

1 LV_{DD} supports eTSECs 1.

2 TV_{DD} supports eTSECs 3.

3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

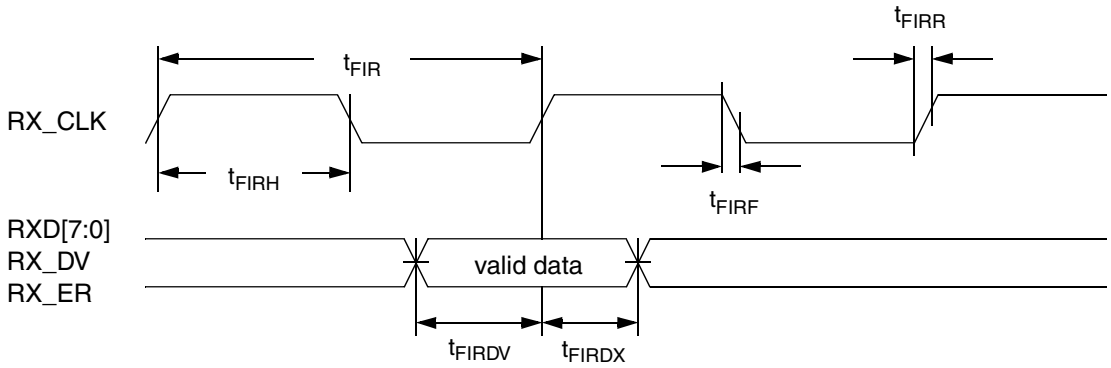

Figure 15. FIFO Receive AC Timing Diagram

2.9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

2.9.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 28. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTK}	—	8.0	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}[3]	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}	—	—	1.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{GTKHDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the GMII transmit AC timing diagram.

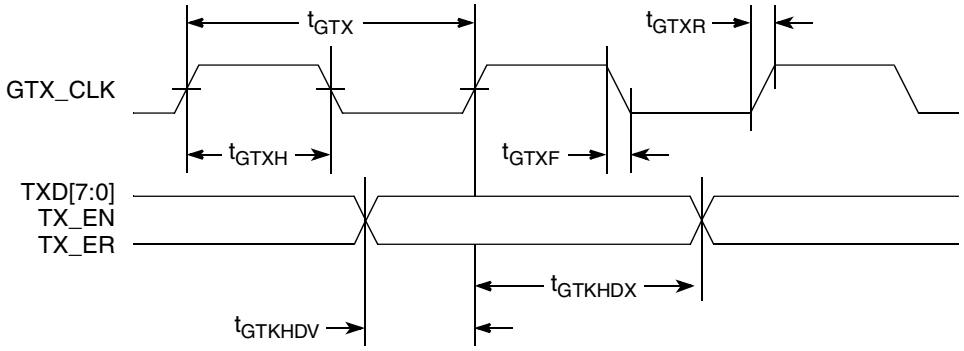

Figure 16. GMII Transmit AC Timing Diagram

2.9.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

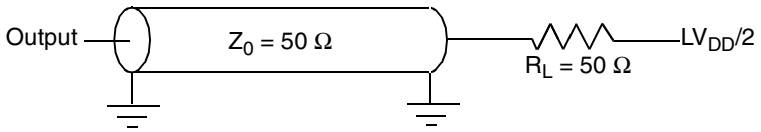

Figure 17. eTSEC AC Test Load

This figure shows the MII transmit AC timing diagram.

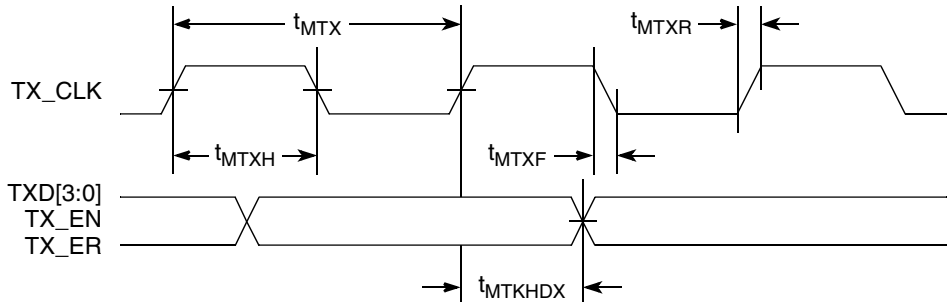

Figure 19. MII Transmit AC Timing Diagram

2.9.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 31. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

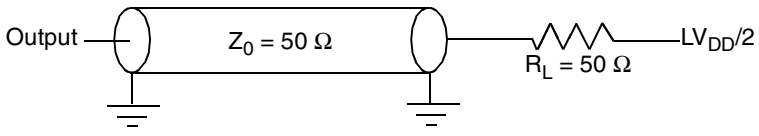

Figure 20. eTSEC AC Test Load

Table 36. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

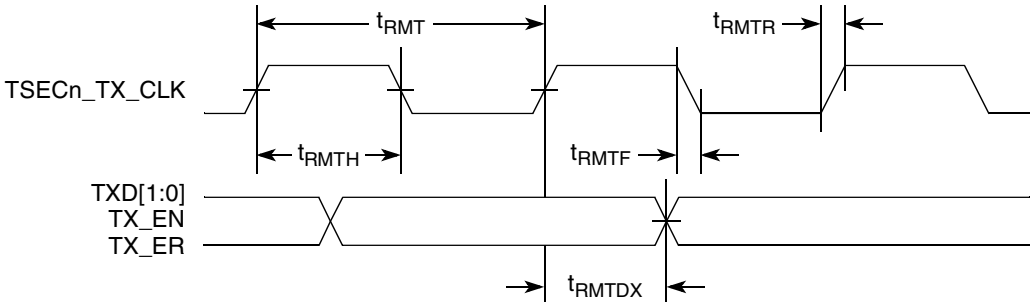

Figure 26. RMII Transmit AC Timing Diagram

2.9.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_RX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_RX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns

2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

Table 44. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.40	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDC frequency	f_{MDC}	0.74	2.5	8.3	MHz	2
EC_MDC period	t_{MDC}	120	400	1350	ns	—
EC_MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
EC_MDC to EC_MDIO delay	t_{MDKHDX}	(16 * t_{plb_clk})-3	—	(16 * t_{plb_clk})+3	ns	3,5,6
EC_MDIO to EC_MDC setup time	t_{MDDVKH}	5	—	—	ns	—

This figure provides the eSDHC clock input timing diagram.

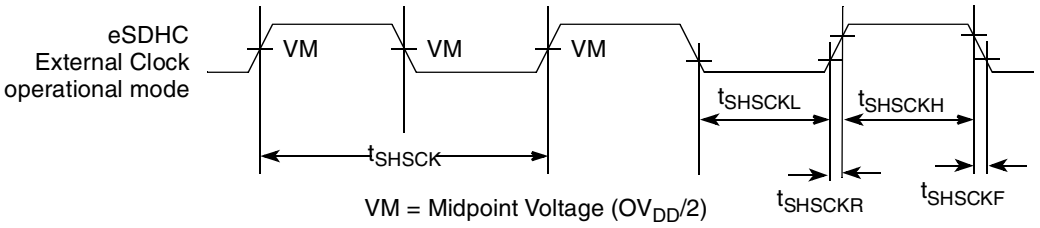

Figure 43. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

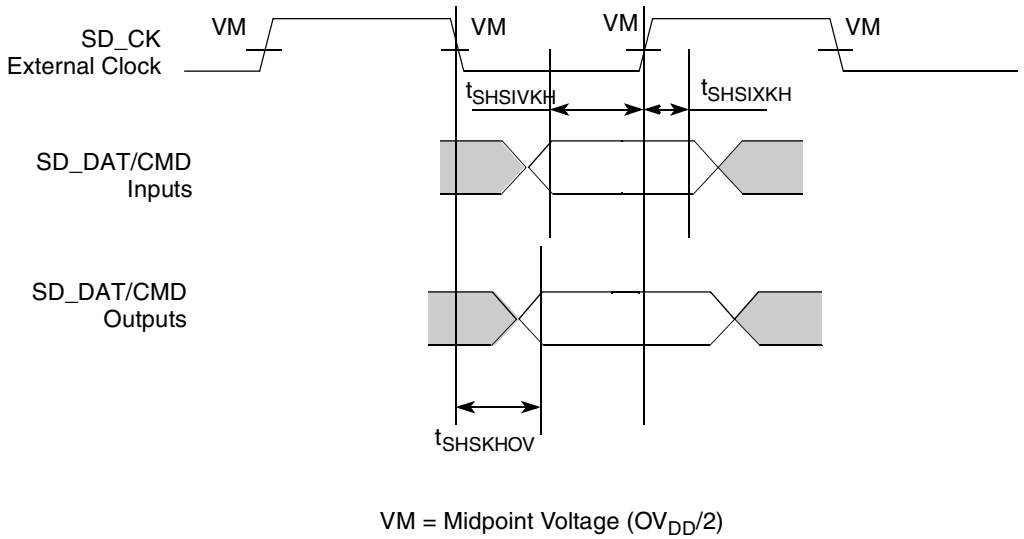

Figure 44. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.14 Programmable Interrupt Controller (PIC)

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

2.15 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

2.15.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Table 57. JTAG DC Electrical Characteristics

Parameter	Symbol [1]	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V

2.16.2 Differential Transmitter (TX) Output Characteristics

This table provides the differential transmitter (TX) output characteristics for the SATA interface.

Table 60. Differential Transmitter (TX) Output Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Channel Speed 1.5G 3.0G	t_{CH_SPEED}	—	 1.5 3.0	—	Gbps	—
Unit Interval 1.5G 3.0G	T_{UI}	666.4333 333.2167	666.4333 333.3333	670.2333 335.1167	ps	—
DC Coupled Common Mode Voltage	V_{dc_cm}	200	250	450	mV	3
TX Diff Output Voltage 1.5G 3.0G	V_{SATA_TXDIFF}	400 400	500 —	600 700	mV	—
TX rise/fall time 1.5G 3.0G	$t_{SATA\_20\text{-}80TX}$	100 67	— —	273 136	ps	—
TX differential skew	t_{SATA_TXSKEW}	—	—	20	ps	—
TX Differential pair impedance 1.5G	$Z_{SATA\_TXDIFFIM}$	 85	 —	 115	ohm	—
TX Single ended impedance 1.5G	Z_{SATA_TXSEIM}	 40	 —	 —	ohm	—
TX AC common mode voltage (peak to peak) 1.5G 3.0G	$V_{SATA\_TXCMMOD}$	 — —	 — —	 — 50	mV	—
OOB Differential Delta	$V_{SATA\_OOBvdoff}$	—	—	25	mV	1
OOB Common mode Delta	V_{SATA_OOBcm}	—	—	50	mV	1
TX Rise/Fall Imbalance	$T_{SATA\_TXR/Fbal}$	—	—	20	%	—
TX Amplitude Imbalance	$T_{SATA\_TXampbal}$	—	—	10	%	—
TX Differential Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXDD11}	 — — — — — —	 — — — — — —	 14 8 6 6 3 1	 dB	 1, 2

Table 60. Differential Transmitter (TX) Output Characteristics (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
TX Common Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXCC11}	 — — — — — —	 — — — — — —	 5 5 2 2 1 1	 dB	 1, 2
TX Impedance Balance 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXDC11}	 — — — — — —	 — — — — — —	 30 20 10 10 4 4	 dB	 1, 2
Deterministic jitter 1.5G 3.0G	U_{SATA_TXDJ}	—	—	 0.18 0.14	 UI	—
Total Jitter 1.5G 3.0G	U_{SATA_TXTJ}	—	—	 0.42 0.32	 UI	—

Notes:
1. Only applies when operating in 3.0Gb data rate mode.
2. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
3. Only applies to Gen1i mode.

Table 64. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 63).

Parameter	Symbol [1]	Min	Max	Unit	Notes
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the chip acts as the I²C bus master while transmitting, the chip drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. For details of the I²C frequency calculation, refer to *Determining the I²C Frequency Divider Ratio for SCL* (AN2919). Note that the I²C Source Clock Frequency is half of the CCB clock frequency for the chip.
3. The maximum t_{I2DVKH} has only to be met if the chip does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

This figure provides the AC test load for the I²C.

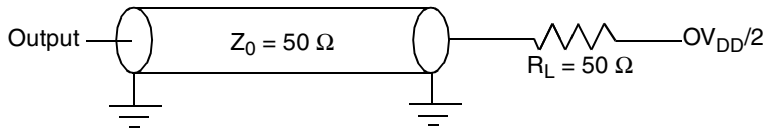

Figure 51. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

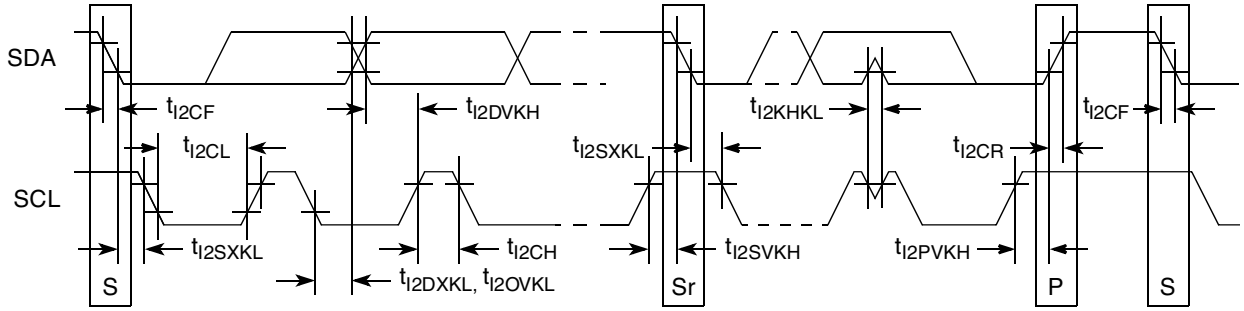

Figure 52. I²C Bus AC Timing Diagram

2.21.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 72. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = \|V_{RXD+} - V_{RXD-}\|/2 + V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and –300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

4.1 Part Numbers Fully Addressed by this Document

This table shows the part numbering nomenclature.

Table 82. Part Numbering Nomenclature

MPC	*nnnn*	*E*	*C*	*VT*	*AA*	*X*	*R*
Product Code	**Part Identifier**	**Security Engine**	**Tiers and Temperature Range**	**Package [1]**	**Processor Frequency [2]**	**DDR Frequency [3]**	**Revision Level**
MPC	8536 8535	E = included	• A = Commercial tier standard temperature range (0° to 90°C) • B or Blank = industrial tier standard temperature range (0° to 105°C) • C = Industrial tier extended temperature range (–40° to 105°C)	• VT = FC-PBGA • (Pb-free) • PX = plastic standard	• AK = 600 MHz • AN = 800 MHz • AQ = 1000 MHz • AT = 1250 MHz • AU = 1333 MHz • AV = 1500 MHz	• G = 400 MHz • H = 500 MHz • J = 533 MHz • L = 667 MHz	• Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0190, 0x803F0191) • A = Ver. 1.2 (SVR = 0x803F0192)
		Blank = not included					• Blank = Ver. 1.0 or 1.1 (SVR = 0x80370190, 0x80370191) • A = Ver. 1.2 (SVR = 0x80370192)

Notes:

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.

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