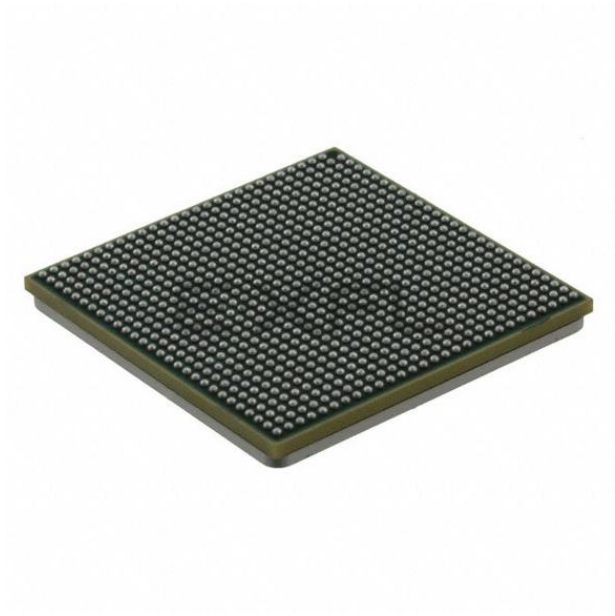

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535avtakg

Table of Contents

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DMA_DREQ[0:1] /GPIO[14:15]	DMA Request	AB10,AD11	I	OV_{DD}	—
DMA_DDONE[0:1] /GPIO[12:13]	DMA Done	AA11,AB11	O	OV_{DD}	—
DMA_DREQ[2]/LCS[5]	Chips selects / DMA Request	H16	I/O	BV_{DD}	1,29
DMA_DACK[2]/LCS[6]	Chips selects / DMA Ack	J16	O	BV_{DD}	1,29
DMA_DDONE[2]/LCS[7]	Chips selects / DMA Done	L18	O	BV_{DD}	1,29
DMA_DREQ[3]/IRQ[9]	External interrupt/DMA request	AE13	I	OV_{DD}	1
DMA_DACK[3]/IRQ[10]	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
DMA_DDONE[3]/IRQ[11]	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
USB Port 1					
USB1_D[7:0]	USB1 Data bits	AF1,AE2,AE1,AD2, AC2,AC1,AB2,AB1	I/O	OV_{DD}	—
USB1_NXT	USB1 Next data	AF2	I	OV_{DD}	—
USB1_DIR	USB1 Data Direction	AH1	I	OV_{DD}	—
USB1_STP	USB1 Stop	AG1	O	OV_{DD}	5,9
USB1_PWRFAULT	USB1 bus power fault.	AH2	I	OV_{DD}	—
USB1_PCTL0/GPIO[6]	USB1 Port control 0	AC3	O	OV_{DD}	—
USB1_PCTL1/GPIO[7]	USB1 Port control 1	AC4	O	OV_{DD}	—
USB1_CLK	USB1 bus clock	AD1	I	OV_{DD}	—
USB Port 2					
USB2_D[7:0]	USB2 Data bits	AE6,AC6,AF5,AE5, AF4,AE4,AE3,AD3	I/O	OV_{DD}	—
USB2_NXT	USB2 Next data	AC7	I	OV_{DD}	—
USB2_DIR	USB2 Data Direction	AF7	I	OV_{DD}	—
USB2_STP	USB2 Stop	AD7	O	OV_{DD}	5,9
USB2_PWRFAULT	USB2 bus power fault.	AC8	I	OV_{DD}	—
USB2_PCTL0/GPIO[8]	USB2 Port control 0	AG9	O	OV_{DD}	—
USB2_PCTL1/GPIO[9]	USB2 Port control 1	AC9	O	OV_{DD}	—
USB2_CLK	USB2 bus clock	AD5	I	OV_{DD}	—
—					
Reserved	—	AH8	—	—	—
Reserved	—	AH7,AG6,AH6,AG5, AG4,AH4,AG3,AH3, AG7, AG8, AH9,AH5	—	—	27

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	—	XV_{DD}	—
S2VDD	SerDes 2 core logic supply	R6,N7,M9	—	$S2V_{DD}$	—
X2VDD	SerDes 2 transceiver supply	R11,N12,L11	—	$X2V_{DD}$	—
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13	—	V_{DD_CORE}	—
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	—	V_{DD_PLAT}	—
AVDD_CORE	CPU PLL supply	AH16	—	AV_{DD_CORE}	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV_{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV_{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV_{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV_{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	—	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V_{DD_CORE}	13
SENSEVDD_PLAT	—	W17	—	V_{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13	—	—	—
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	—	—	—

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	–0.3 to 1.21	V	—
Platform supply voltage		V_{DD_PLAT}	–0.3 to 1.1	V	—
PLL core supply voltage		AV_{DD_CORE}	–0.3 to 1.21	V	—
PLL other supply voltage		AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers		SV_{DD}, $S2V_{DD}$	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}, $X2V_{DD}$	–0.3 to 1.1	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface		–0.3 to 1.65		
Three-speed Ethernet I/O		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	2
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	2
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	^0C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.
2. The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

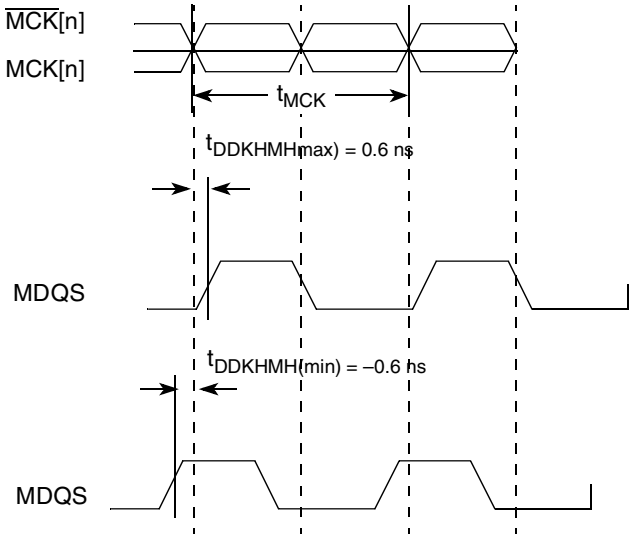


Figure 9. Timing Diagram for tDDKHMH

This figure shows the DDR SDRAM output timing diagram.

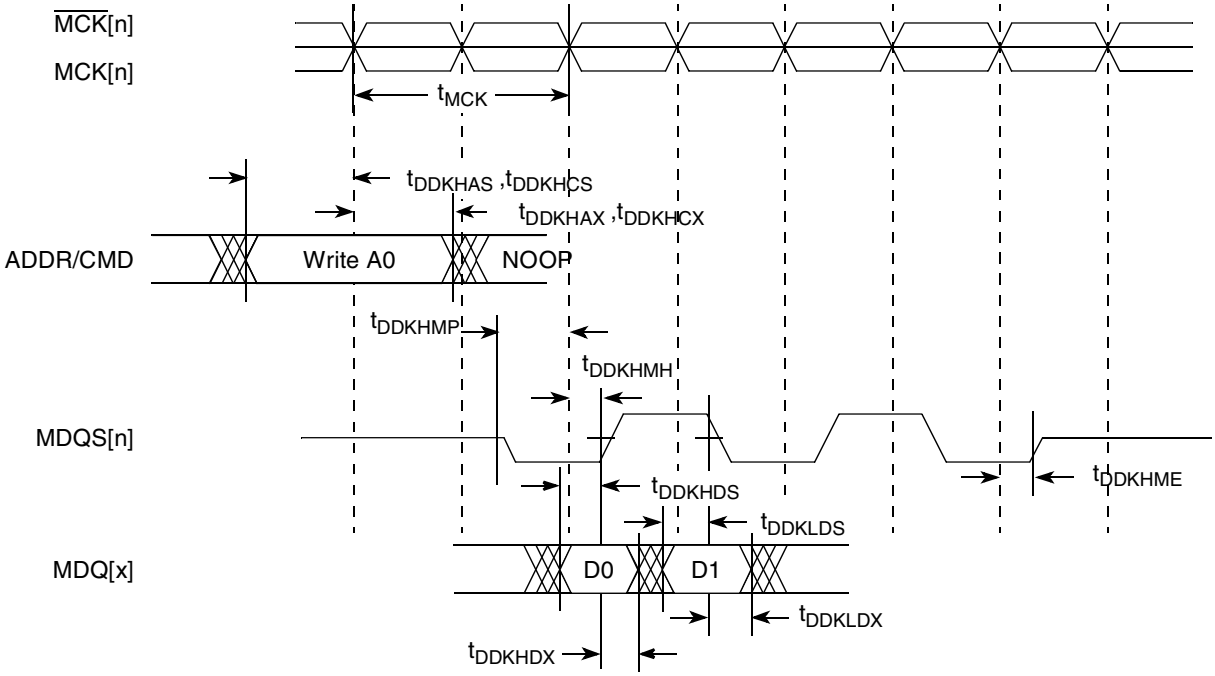


Figure 10. DDR SDRAM Output Timing Diagram

This figure shows the GMII transmit AC timing diagram.

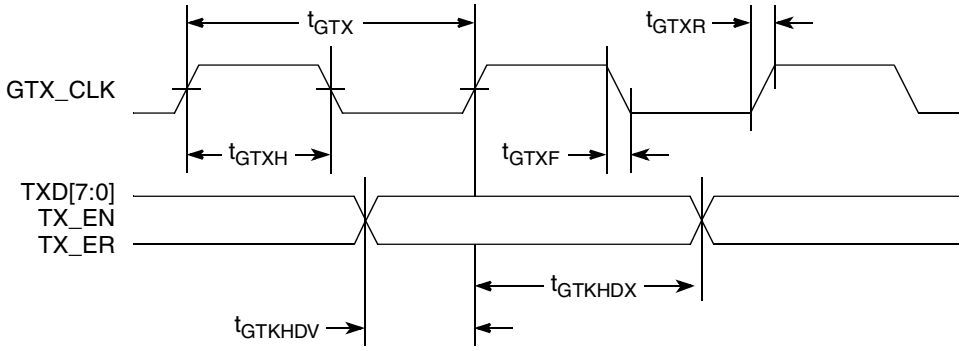


Figure 16. GMII Transmit AC Timing Diagram

2.9.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

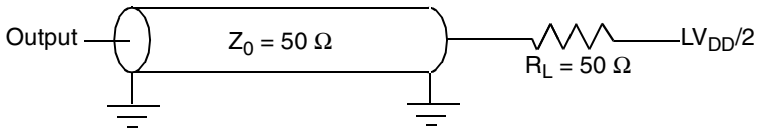


Figure 17. eTSEC AC Test Load

Table 36. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

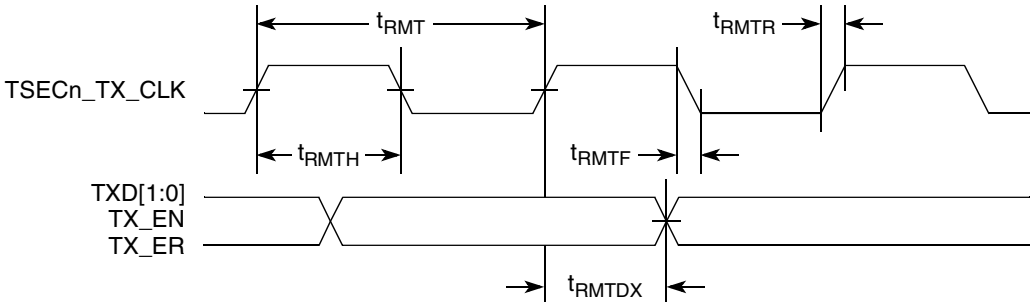


Figure 26. RMII Transmit AC Timing Diagram

2.9.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_RX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_RX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns

Table 37. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Fall time TSECn_RX_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSECn_RX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to TSECn_RX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

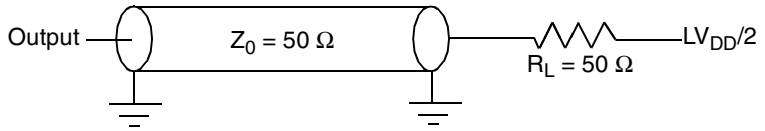


Figure 27. eTSEC AC Test Load

This figure shows the RMII receive AC timing diagram.

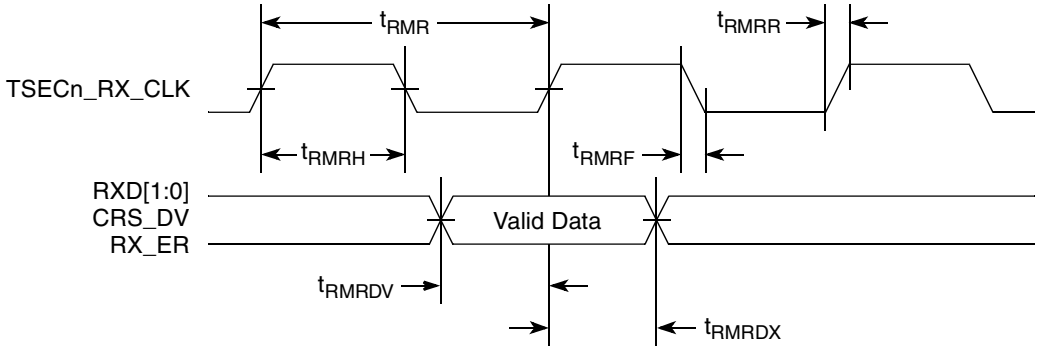


Figure 28. RMII Receive AC Timing Diagram

2.9.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes 2 interface of the chip as shown in Figure 29, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to S2GND (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 68.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 3.6, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

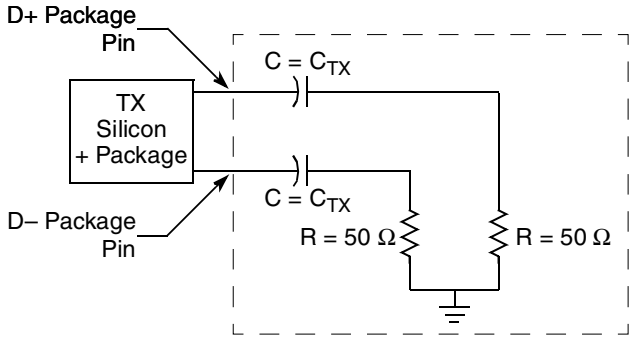


Figure 32. SGMII AC Test/Measurement Load

2.9.4 eTSEC IEEE 1588 AC Specifications

This figure shows the data and command output timing diagram.

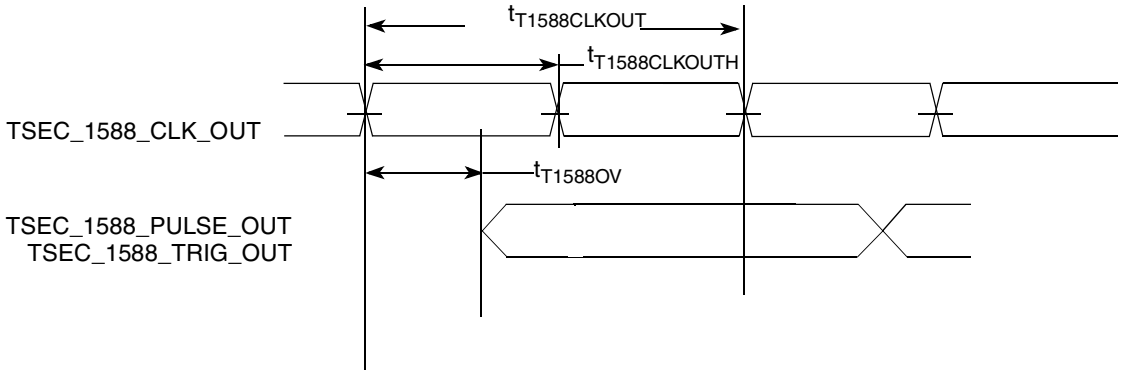


Figure 33. eTSEC IEEE 1588 Output AC timing

[1] The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

This figure provides the data and command input timing diagram.

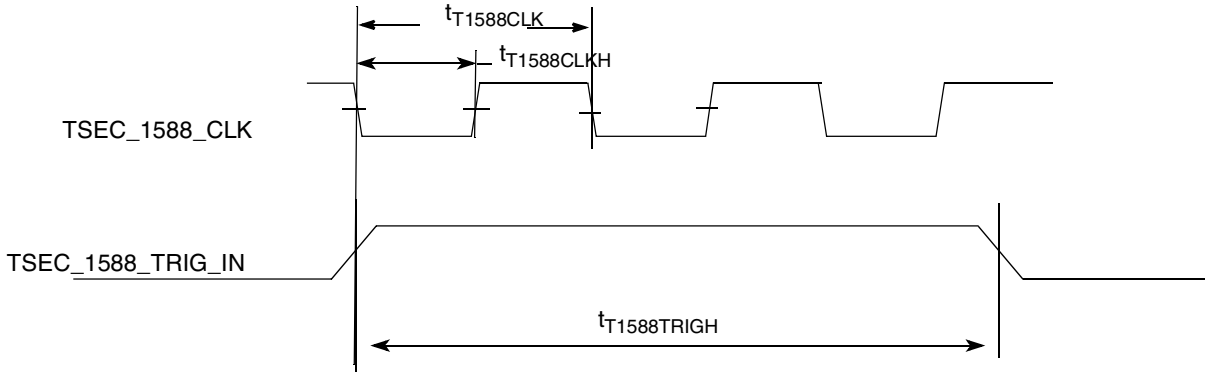


Figure 34. eTSEC IEEE 1588 Input AC timing

The IEEE 1588 AC timing specifications are in the following table.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	T_{TX_CLK}*7	ns	1
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2*$t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. When TMR_CTRL[CKSEL]=00, the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in the Table above. The maximum value of $t_{T1588CLK}$ is defined in terms of T_{TX_CLK}, which is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running.
   When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.
   See the *MPC8536E PowerQUICC III Integrated Communications Processor Reference Manual* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

2.10 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals EC_MDIO (management data input/output) and EC_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in Section 2.9, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management”

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDIO to EC_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
EC_MDC rise time	t_{MDCR}	—	—	10	ns	—
EC_MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. t_{CLKplb_clk} is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time t_{MDKHDX}. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

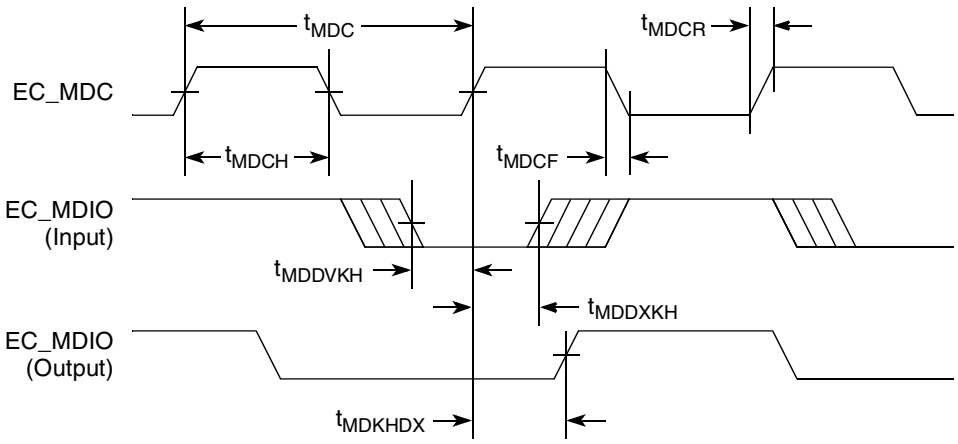


Figure 35. MII Management Interface Timing Diagram

2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

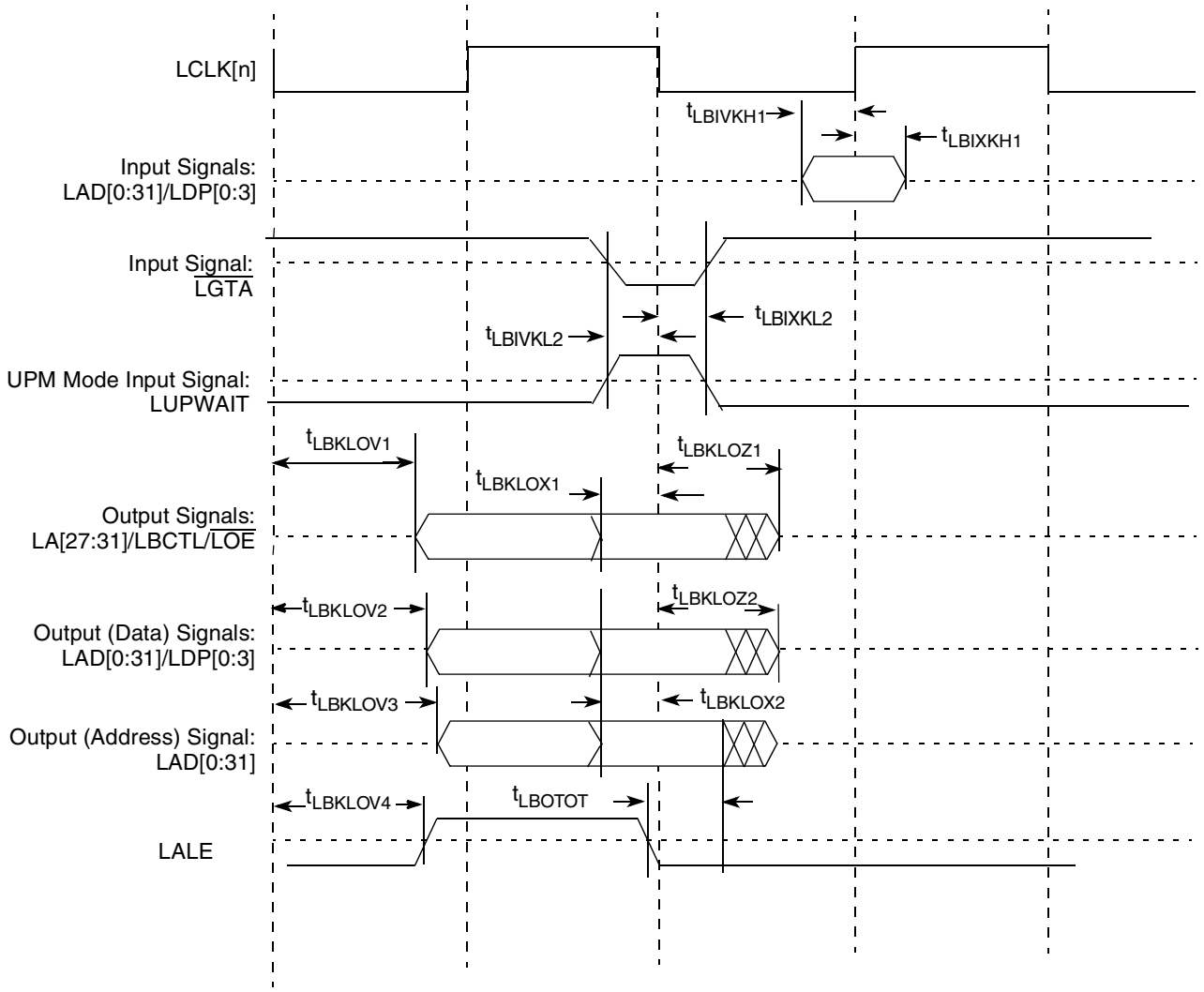


Figure 40. Local Bus Signals (PLL Bypass Mode)

This table describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 54. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	5.1	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	4.2	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	-1.4	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-2.0	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.4	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	0.5	ns	4

Table 54. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	0.5	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	0.5	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.5	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	—	2.2	ns	4,8
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	—	2.2	ns	4,8
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.1	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.1	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. These timing parameters for PLL bypass mode are defined in the opposite direction of the PLL enabled output hold timing parameters.

Table 55. eSDHC interface DC Electrical Characteristics (continued)

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output low voltage	V_{OL}	I_{OL} = 100uA @OVDDmin	—	0.125 * OVDD	V	—
Output high voltage	V_{OH}	I_{OH} = -100 uA	OV_{DD} - 0.2	—	—	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	—	2

Notes:

1. The min V_{IL} and V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.13.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in the following figure.

Table 56. eSDHC AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full speed/high speed mode MMC Full speed/high speed mode	f_{SHSCK}	 0	 25/50 20/52	MHz	2, 5
SD_CLK clock frequency - identification mode	f_{SIDCK}	0 100	400	KHz	3, 5
SD_CLK clock low time - High speed/Full speed mode	t_{SHSCKL}	7/10	—	ns	5
SD_CLK clock high time - High speed/Full speed mode	t_{SHSCKH}	7/10	—	ns	5
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	5
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	4,5,6
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	5,6
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	5,6

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52MHz for a MMC card.
3. 0 Hz means to stop the clock. The given minimum frequency range is for cases were a continuous clock is required.
4. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns.
5. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF
6. The parameter values apply to both full speed and high speed modes.

2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

Table 59. Reference Clock Input Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD2_REF_CLK/_B reference clock cycle time	t_{CLK_REF}	100	—	150	MHz	1
SD2_REF_CLK/_B frequency tolerance	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/_B rise/fall time (80%-20%)	$t_{CLK\_RISE}/t_{CLK\_FALL}$	—	—	1	ns	—
SD_REF_CLK/_B duty cycle (@50% X2VDD)	t_{CLK_DUTY}	45	50	55	%	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter (peak-to-peak)	t_{CLK_PJ}	–50	—	+50	ps	2,3

Note:

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

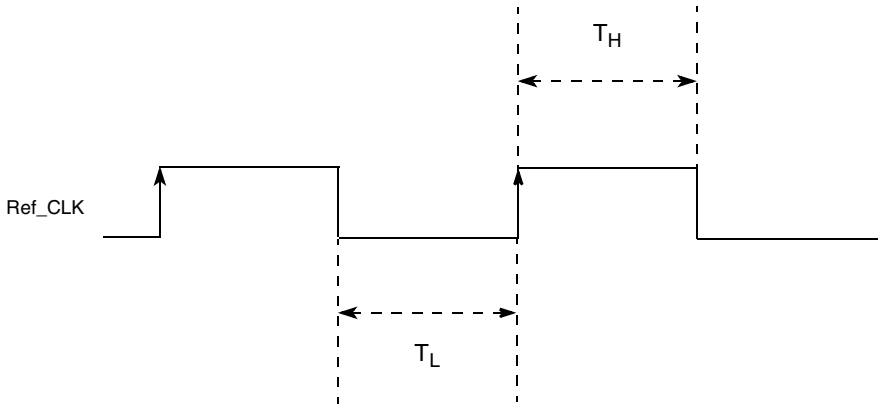


Figure 49. Reference Clock Timing Waveform

2.19 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

2.19.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 67. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.19.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. This table provides the PCI AC timing specifications at 66 MHz.

Table 68. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 5
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7

2.23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in the following table:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 75. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	Reserved	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

2.23.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in this table.

Table 76. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

2.23.4 DDR/DDRCLK PLL Ratio

The DDR memory controller complex can be synchronous with, or asynchronous to, the CCB, depending on configuration.

The following table describes the clock ratio between the DDR memory controller complex and the DDR/DDRCLK PLL reference clock, DDRCLK, which is not the memory bus clock.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for the DDR controller to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 77 reflects the DDR data rate to DDRCLK ratio, since the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

2.23.6 Frequency Options

2.23.6.1 SYSCLK to Platform Frequency Options

This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 78. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)						
3						333	400
4				333	400	444	
5			333	415	500		
6			400	500			
8		333					
10	333	417					
12	400	500					

2.24 Thermal

This section describes the thermal specifications of the chip.

2.24.1 Thermal Characteristics

This table provides the package thermal characteristics.

Table 79. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	18	°C/W	1, 2

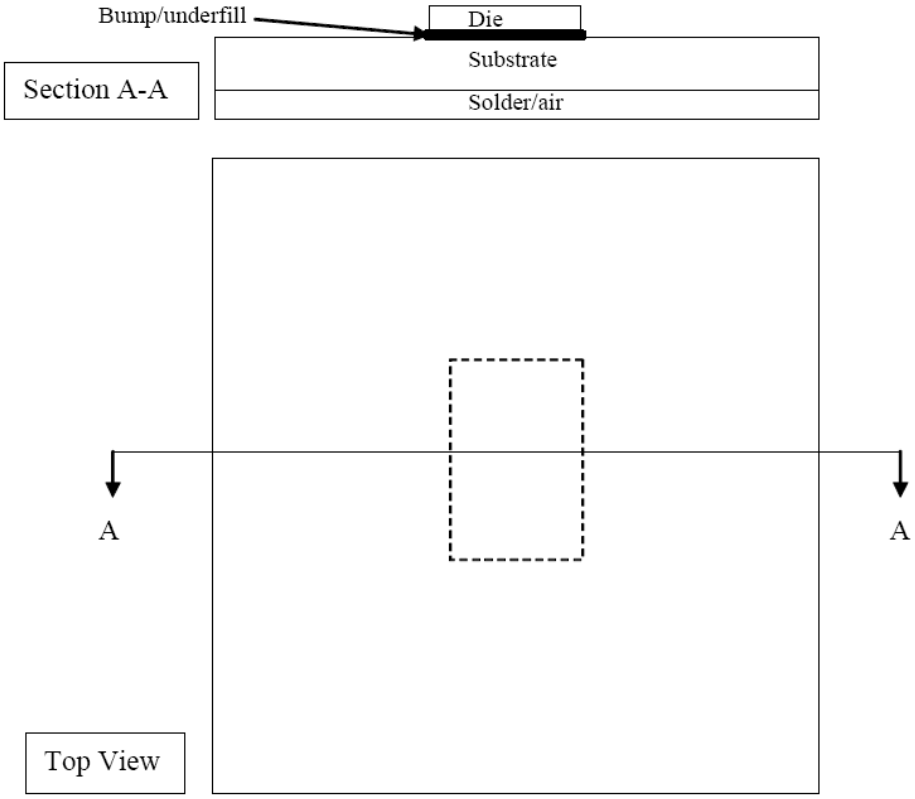
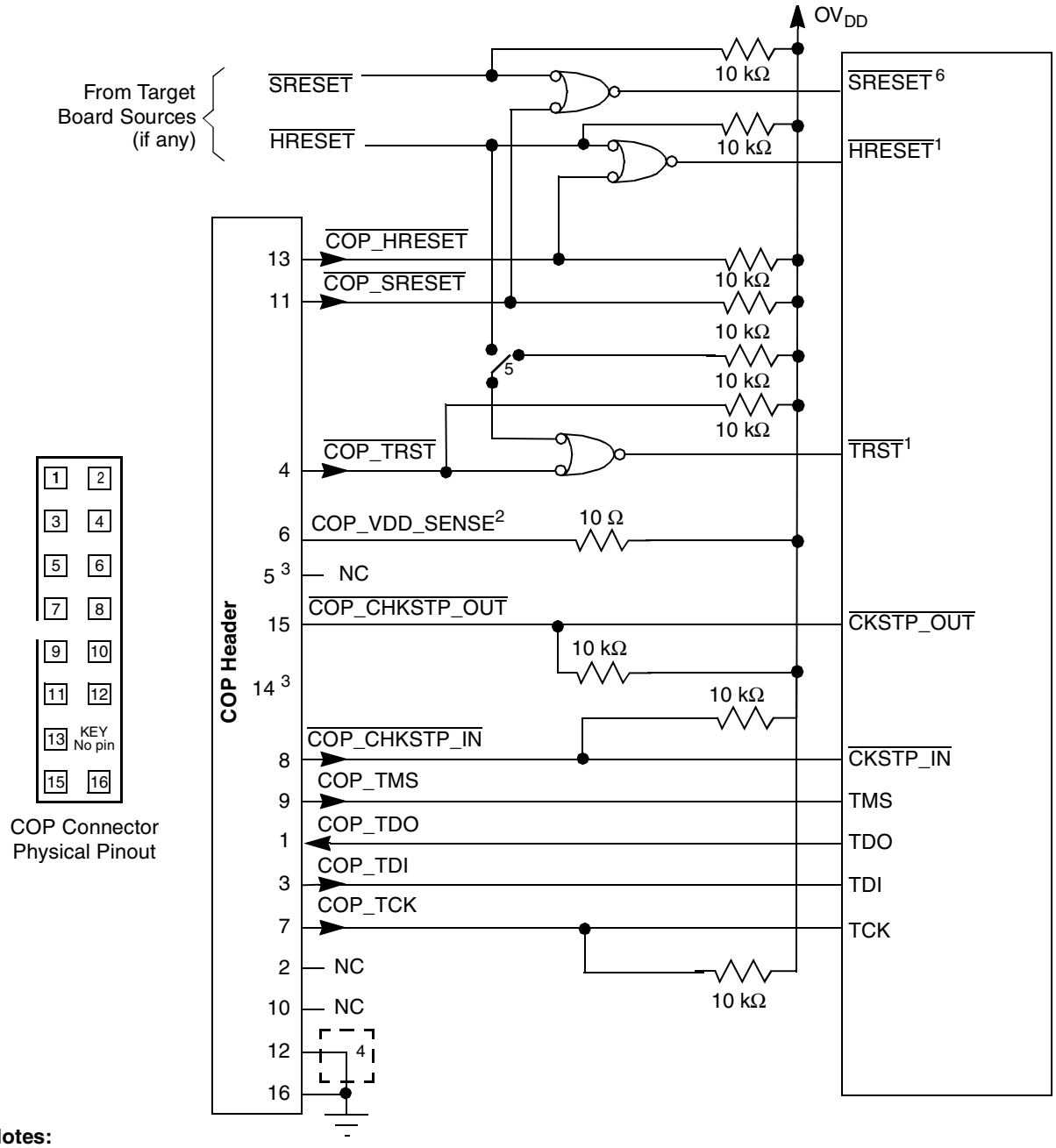


Figure 72. System-Level Thermal Model for the Chip (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

2.24.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 78. JTAG Interface Connection