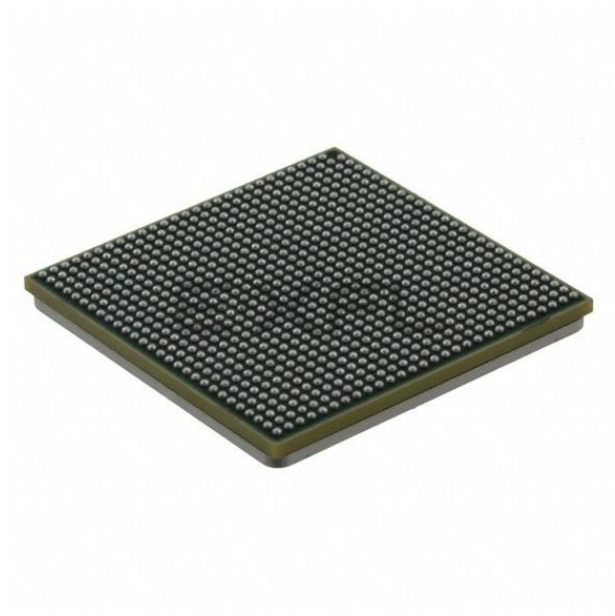

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535avtakga

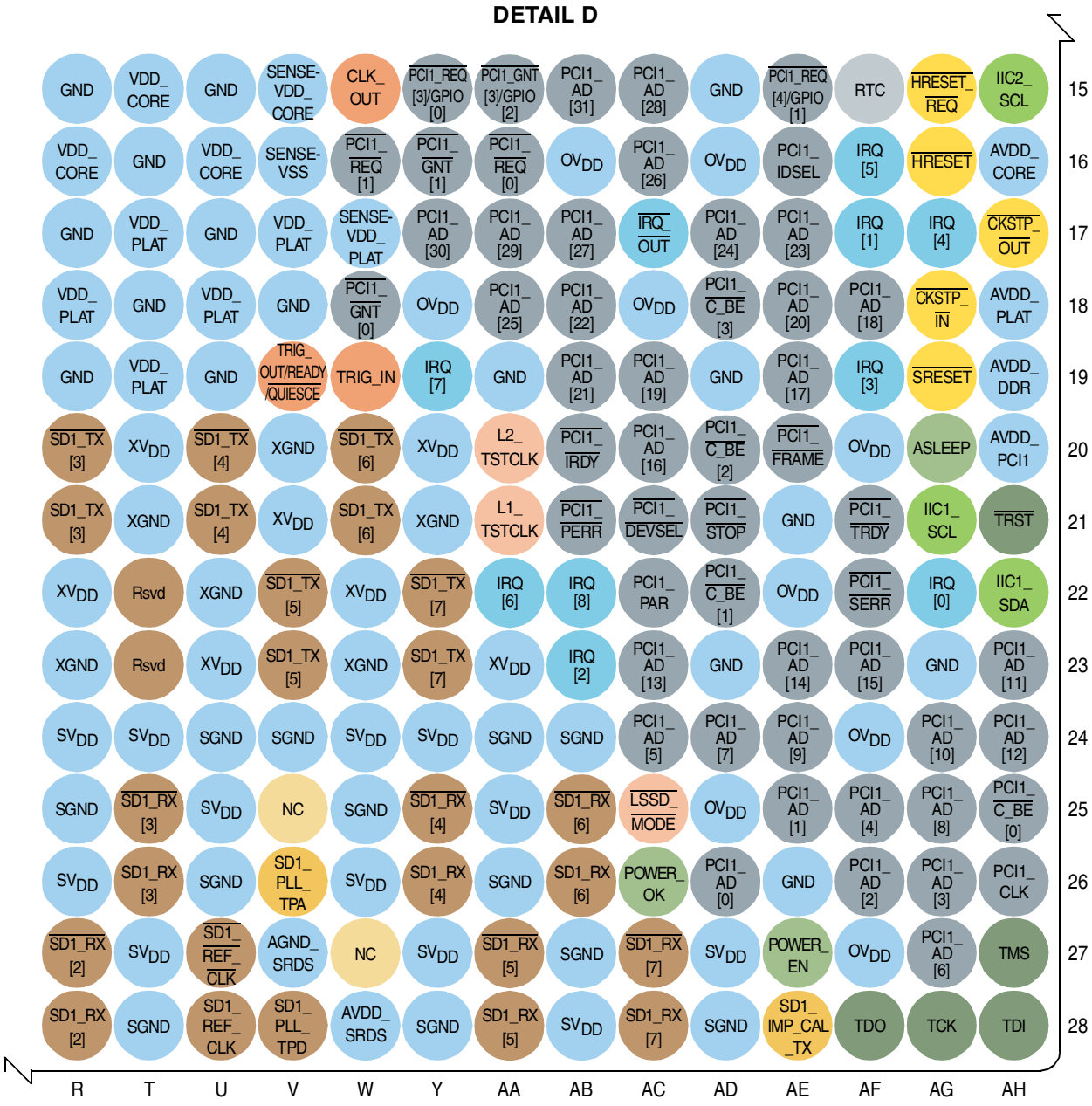


Figure 6. Chip Pin Map Detail D

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Programmable Interrupt Controller					
$\overline{\text{MCP}}$	Machine check processor	Y14	I	OV_{DD}	—
$\overline{\text{UDE}}$	Unconditional debug event	AB14	I	OV_{DD}	—
IRQ[0:8]	External interrupts	AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ[3]}}$	External interrupt/DMA request	AE13	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK[3]}}$	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE[3]}}$	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	Interrupt output	AC17	O	OV_{DD}	2,4
Ethernet Management Interface					
EC_MDC	Management data clock	Y10	O	OV_{DD}	5,9,22
EC_MDIO	Management data In/Out	Y11	I/O	OV_{DD}	—
Gigabit Reference Clock					
EC_GTX_CLK125	Reference clock	AA6	I	LV_{DD}	31
Three-Speed Ethernet Controller (Gigabit Ethernet 1)					
TSEC1_TXD[7:0]	Transmit data	AA8,AA5,Y8,Y5,W3, W5,W4,W6	O	LV_{DD}	5,9,22
TSEC1_TX_EN	Transmit Enable	W1	O	LV_{DD}	23
TSEC1_TX_ER	Transmit Error	AB5	O	LV_{DD}	5,9
TSEC1_TX_CLK	Transmit clock In	AB4	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit clock Out	W2	O	LV_{DD}	—
TSEC1_CRS	Carrier sense	AA9	I/O	LV_{DD}	17
TSEC1_COL	Collision detect	AB6	I	LV_{DD}	—
TSEC1_RXD[7:0]	Receive data	AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2	I	LV_{DD}	—
TSEC1_RX_DV	Receive data valid	AA1	I	LV_{DD}	—
TSEC1_RX_ER	Receive data error	Y9	I	LV_{DD}	—
TSEC1_RX_CLK	Receive clock	AA3	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)					
TSEC3_TXD[7:0]	Transmit data	T12,V8,U8,V9,T8,T7, T5,T6	O	TV_{DD}	5,9,22
TSEC3_TX_EN	Transmit Enable	V5	O	TV_{DD}	23
TSEC3_TX_ER	Transmit Error	U9	O	TV_{DD}	5,9

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_CLK	Transmit clock In	U10	I	TV_{DD}	—
TSEC3_GTX_CLK	Transmit clock Out	U5	O	TV_{DD}	—
TSEC3_CRS	Carrier sense	T10	I/O	TV_{DD}	17
TSEC3_COL	Collision detect	T9	I	TV_{DD}	—
TSEC3_RXD[7:0]	Receive data	U12,U13,U6,V6,V1,U3, U2,V3	I	TV_{DD}	—
TSEC3_RX_DV	Receive data valid	V2	I	TV_{DD}	—
TSEC3_RX_ER	Receive data error	T4	I	TV_{DD}	—
TSEC3_RX_CLK	Receive clock	U1	I	TV_{DD}	—
IEEE 1588					
TSEC_1588_CLK	Clock In	W9	I	LV_{DD}	29
TSEC_1588_TRIG_IN[0:1]	Trigger In	W8,W7	I	LV_{DD}	29
TSEC_1588_TRIG_OUT[0:1]	Trigger Out	U11,W10	O	LV_{DD}	5,9,29
TSEC_1588_CLK_OUT	Clock Out	V10	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT1	Pulse Out1	V11	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT2	Pulse Out2	T11	O	LV_{DD}	5,9,29
eSDHC					
SDHC_CMD	Command line	AH10	I/O	OV_{DD}	29
$\overline{\text{SDHC\_CD}}$/GPIO[4]	Card detection	AH11	I	OV_{DD}	—
SDHC_DAT[0:3]	Data line	AG12,AH12,AH13, AG11	I/O	OV_{DD}	29
SDHC_DAT[4:7] / SPI_CS[0:3]	8-bit MMC Data line / SPI chip select	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
SDHC_CLK	SD/MMC/SDIO clock	AG13	I/O	OV_{DD}	29
$\overline{\text{SDHC\_WP}}$/GPIO[5]	Card write protection	AG10	I	OV_{DD}	1, 32
eSPI					
SPI_MOSI	Master Out Slave In	AF8	I/O	OV_{DD}	29
SPI_MISO	Master In Slave Out	AD9	I	OV_{DD}	29
SPI_CLK	eSPI clock	AD8	I/O	OV_{DD}	29
SPI_CS[0:3] / SDHC_DAT[4:7]	eSPI chip select / SDHC 8-bit MMC data	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
DUART					
$\overline{\text{UART\_CTS}}$[0:1]	Clear to send	AE11,Y12	I	OV_{DD}	29
$\overline{\text{UART\_RTS}}$[0:1]	Ready to send	AB12,AD12	O	OV_{DD}	29
UART_SIN[0:1]	Receive data	AC12,AF12	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
General-Purpose Input/Output					
GPIO[0:1]/PCI1_REQ[3:4]	GPIO/PCI request	Y15,AE15	I/O	OV_{DD}	—
GPIO[2:3]/PCI1_GNT[3:4]	GPIO/PCI grant	AA15,AC14	I/O	OV_{DD}	—
GPIO[4]/SDHC_CD	GPIO/SDHC card detection	AH11	I/O	OV_{DD}	—
GPIO[5]/SDHC_WP	GPIO/SDHC write protection	AG10	I/O	OV_{DD}	32
GPIO[6]/USB1_PCTL0	GPIO/USB1 PCTL0	AC3	I/O	OV_{DD}	—
GPIO[7]/USB1_PCTL1	GPIO/USB1 PCTL1	AC4	I/O	OV_{DD}	—
GPIO[8]/USB2_PCTL0	GPIO/USB2 PCTL0	AG9	I/O	OV_{DD}	—
GPIO[9]/USB2_PCTL1	GPIO/USB2 PCTL1	AC9	I/O	OV_{DD}	—
GPIO[10:11] /DMA_DACK[0:1]	GPIO/DMA Ack	AD6,AE10	I/O	OV_{DD}	—
GPIO[12:13] /DMA_DDONE[0:1]	GPIO/DMA done	AA11,AB11	I/O	OV_{DD}	—
GPIO[14:15] /DMA_DREQ[0:1]	GPIO/DMA request	AB10,AD11	I/O	OV_{DD}	—
System Control					
HRESET	Hard reset	AG16	I	OV_{DD}	—
HRESET_REQ	Hard reset - request	AG15	O	OV_{DD}	22
SRESET	Soft reset	AG19	I	OV_{DD}	—
CKSTP_IN	CheckStop in	AG18	I	OV_{DD}	—
CKSTP_OUT	CheckStop Output	AH17	O	OV_{DD}	2,4
Debug					
TRIG_IN	Trigger in	W19	I	OV_{DD}	—
TRIG_OUT/READY /QUIESCE	Trigger out/Ready/Quiesce	V19	O	OV_{DD}	22
MSRCID[0:1]	Memory debug source port ID	W12,W13	O	OV_{DD}	6,9
MSRCID[2:4]	Memory debug source port ID	V12, W14,W11	O	OV_{DD}	6,9,22
MDVAL	Memory debug data valid	V13	O	OV_{DD}	6,22
CLK_OUT	Clock Out	W15	O	OV_{DD}	11
Clock					
RTC	Real time clock	AF15	I	OV_{DD}	—
SYSCLK	System clock / PCI clock	AH14	I	OV_{DD}	—
DDRCLK	DDR clock	AC13	I	OV_{DD}	30
JTAG					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals may be listed only once and may not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled-high.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD_CORE}/V_{DD_PLAT}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
17. This pin is only an output in FIFO mode when used as Rx Flow Control.
18. Do not connect.
19. These must be pulled up (100 Ω- 1 kΩ) to OVDD.
20. Independent supplies derived from board VDD.
21. Recommend a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD}.
22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.
23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
24. General-Purpose POR configuration of user system.

Table 5. Power Dissipation (continued)[5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	1250	500	500	1.0	1.0	105 / 90	—	5.3/4.4	—	5.0/4.0	1, 3, 8
Thermal (W)							—	4.4/3.6	—	5.0/4.0	1, 4, 8
Typical (W)						65	2.2		1.7		1
Doze (W)							1.6	2.4	1.5	2.1	1
Nap (W)							0.8	1.6	1.5	2.1	1
Sleep (W)							0.8	1.6	1.1	1.7	1
Deep Sleep (W)						35	0	0	0.6	1.2	1, 6

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 ^{0}C, for Industrial Tier is 105 ^{0}C.
9. Platform power is the power supplied to all the V_{DD_PLAT} pins.

See Section 2.23.6.1, "SYSCLK to Platform Frequency Options," for the full range of CCB frequencies that the chip supports.

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
<= 667 MHz		$0.9 \times t_{MCK}$			7
MDQS epilogue end	t_{DDKHME}			ns	6
<= 667 MHz		$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$		7

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR2 and DDR3 frequency is 667 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

Table 44. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.40	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDC frequency	f_{MDC}	0.74	2.5	8.3	MHz	2
EC_MDC period	t_{MDC}	120	400	1350	ns	—
EC_MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
EC_MDC to EC_MDIO delay	t_{MDKHDX}	(16 * t_{plb_clk})-3	—	(16 * t_{plb_clk})+3	ns	3,5,6
EC_MDIO to EC_MDC setup time	t_{MDDVKH}	5	—	—	ns	—

2.11.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 46. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.11.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the chip.

Table 47. USB General Timing Parameters[6]

Parameter	Symbol [1]	Min	Max	Unit	Notes
usb clock cycle time	t_{USCK}	15	—	ns	2-5
Input setup to usb clock - all inputs	t_{USIVKH}	4	—	ns	2-5
input hold to usb clock - all inputs	t_{USIXKH}	1	—	ns	2-5
usb clock to output valid - all outputs	t_{USKHOV}	—	7	ns	2-5
Output hold from usb clock - all outputs	t_{USKHOX}	2	—	ns	2-5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USBn_DIR pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC) (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	—	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	—	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	—	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 53. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.9	—	ns	3

Table 57. JTAG DC Electrical Characteristics (continued)

Parameter	Symbol [1]	Min	Max	Unit
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

This table provides the JTAG AC timing specifications as defined in the following figures.

Table 58. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions (see Table 3).

Parameter	Symbol [1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times:	t_{JTDVKH}	4	—	ns	
Input hold times:	t_{JTDXKH}	10	—	ns	
Output Valid times:	t_{JTKLDV}	—	10	ns	3
Output hold times:	t_{JTKLDX}	0	—	ns	3

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3.) The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

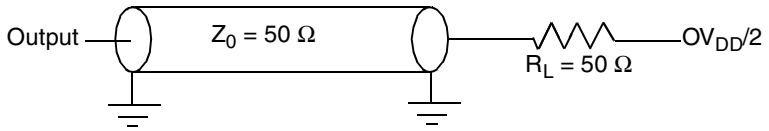


Figure 45. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

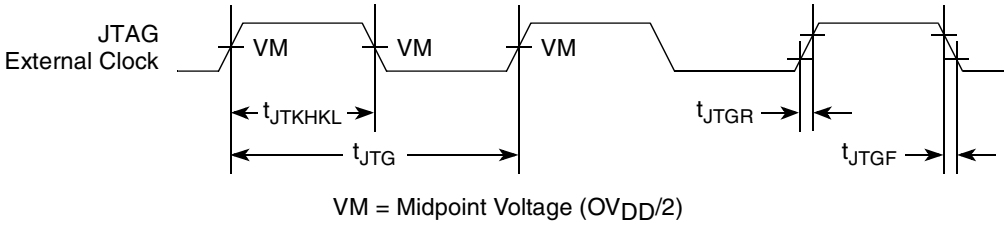


Figure 46. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

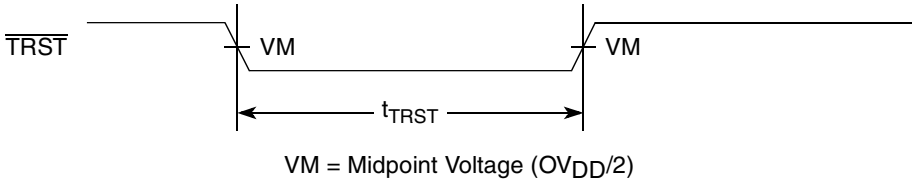


Figure 47. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

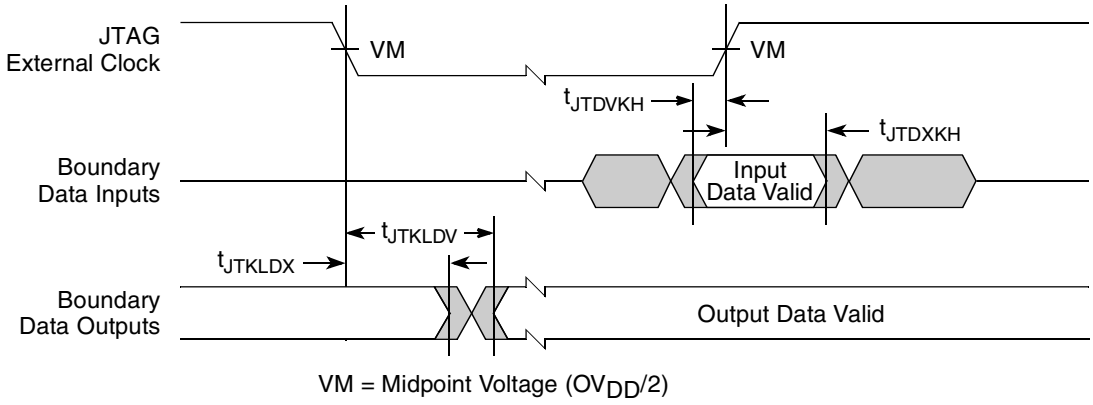


Figure 48. Boundary-Scan Timing Diagram

2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

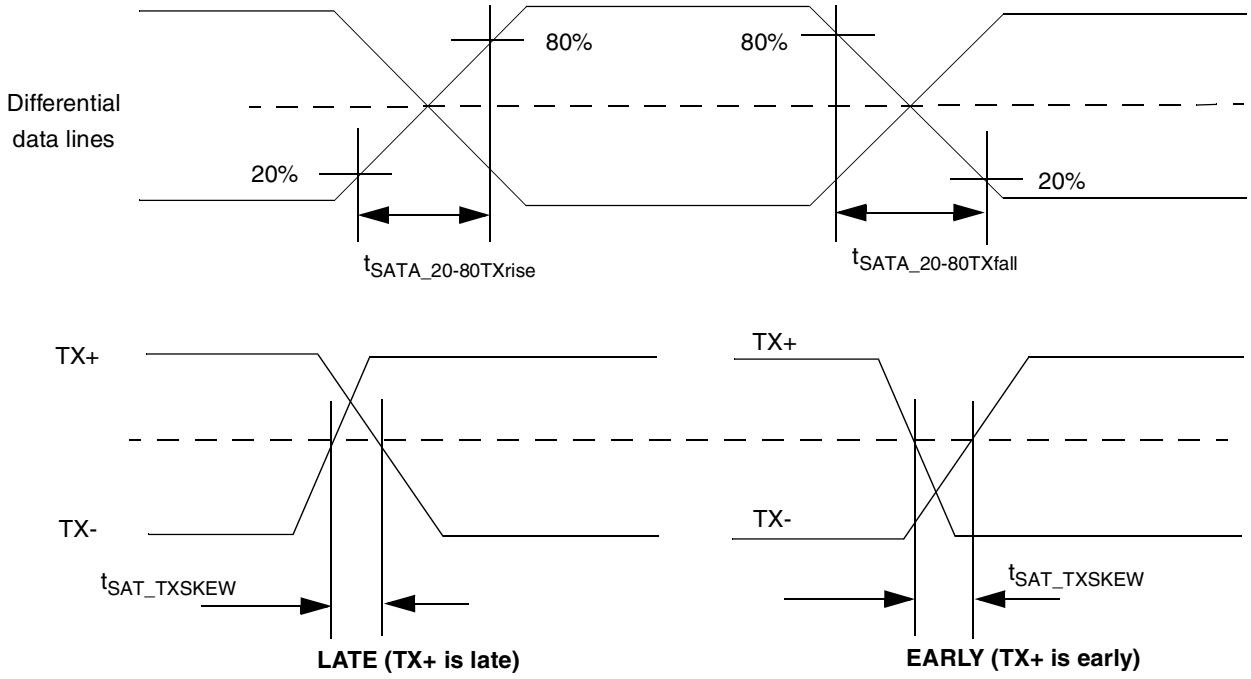


Figure 50. Signal Rise and Fall Times and Differential Skew

2.16.3 Differential Receiver (RX) Input Characteristics

This table provides the differential receiver (RX) input characteristics for the SATA interface.

Table 61. Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
RX Differential Input Voltage 1.5G 3.0G	V_{SATA_RXDIFF}	 240 240	 400 —	 600 750	mVp-p	1
RX rise/fall time 1.5G 3.0G	$t_{SATA\_20\text{-}80RX}$	100 67	— —	273 136	ps	—
RX Differential skew 1.5G 3.0G	t_{SATA_RXSKEW}	— —	— —	— 50	ps	—
RX Differential pair impedance 1.5G	$Z_{SATA\_RXDIFFIM}$	85	—	115	ohm	—
RX Single-Ended impedance 1.5G	Z_{SATA_RXSEIM}	40	—	—	ohm	—
DC Coupled Common Mode Voltage	V_{dc_cm}	200	250	450	mV	5

2.16.4 Out-of-Band (OOB) Electrical Characteristics

This table provides the Out-of-Band (OOB) electrical characteristics for the SATA interface of the chip.

Table 62. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	 mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	646.67	666.67	686.67	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTXWakeGap}$	—	160	—	UI	—
COMWAKE Gap Detection Windows	$T_{SATA\_OOBDetWakeGap}$	55	—	175	ns	—
COMINIT/ COMRESET Gap Detection Windows	$T_{SATA\_OOBDetCOMGap}$	175	—	525	ns	—

2.17 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interfaces of the chip.

2.17.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 63. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	OV_{DD}	3.13	3.47	V	—
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the chip's SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 59 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SnGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SnGND). Figure 60 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SDn\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 61 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SDn\_REF\_CLK}}$) through the same source impedance as the clock input (SDn_REF_CLK) in use.

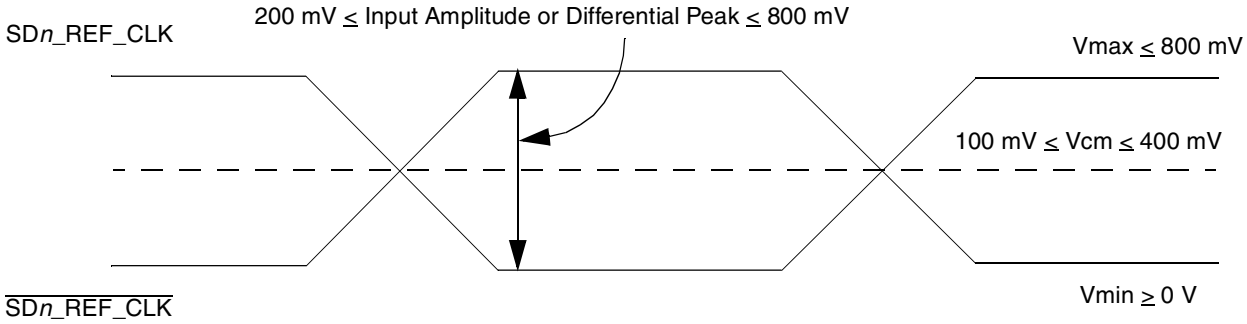


Figure 59. Differential Reference Clock Input DC Requirements (External DC-Coupled)

2.20.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 69. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.0V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 66.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 67.

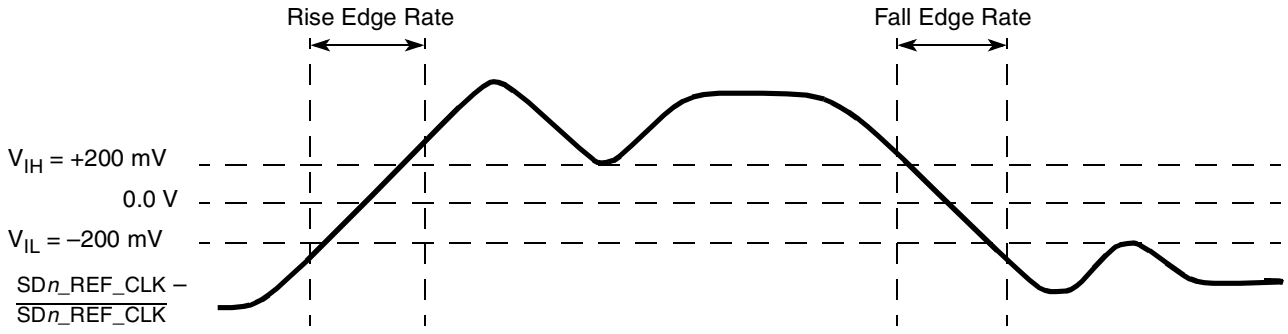


Figure 66. Differential Measurement Points for Rise and Fall Time

2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

2.21.1 DC Requirements for PCI Express SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$

For more information, see Section 2.20.2, "SerDes Reference Clocks."

2.21.2 AC Requirements for PCI Express SerDes Clocks

This table lists AC requirements.

Table 70. SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	1,2,3

Notes:
1. Tj at BER of 10E-6 86 ps Max.
2. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 42 ps.
3. Limits from "PCI Express CEM Rev 2.0" and measured per "PCI Express Rj, D, and Bit Error Rates".

2.21.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

2.21.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this chip. For further details as well as the specifications of the transport and data link layer, please use the PCI Express Base Specification. REV. 1.0a document.

2.21.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 71. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.

2.21.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 72. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = \|V_{RXD+} - V_{RXD-}\|/2 + V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and –300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Table 77. DDR Clock Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	cfg_ddr_pll[0:2]	000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

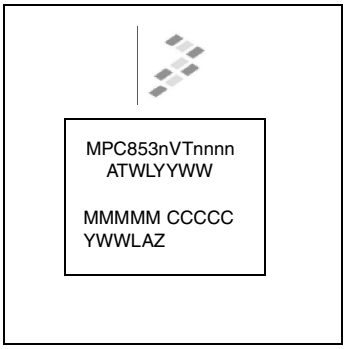
2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

4.2 Part Marking

Parts are marked as in the example shown in the following figure.



FC-PBGA

Notes:

MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 80. Part Marking for FC-PBGA

4.3 Part Numbering

These tables list all part numbers that are offered for the chip.

Table 83. MPC8535 Part Numbers Commercial Tier

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Notes
600/400/400	MPC8535AVTAKG(A)	MPC8535EAVTAKG(A)	—
800/400/400	MPC8535AVTANG(A)	MPC8535EAVTANG(A)	—
1000/400/400	MPC8535AVTAQG(A)	MPC8535EAVTAQG(A)	—
1250/500/500	MPC8535AVTATH(A)	MPC8535EAVTATH(A)	—
1250/500/667	MPC8535AVTATLA	MPC8535EAVTATLA	—

Table 84. MPC8535 Part Numbers Industrial Tier

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Extended Temp Without Security	Extended Temp With Security	Notes
600/400/400	MPC8535BVTAKG(A)	MPC8535EBVTAKG(A)	MPC8535CVTAKG(A)	MPC8535ECVTAKG(A)	1
800/400/400	MPC8535BVTANG(A)	MPC8535EBVTANG(A)	MPC8535CVTANG(A)	MPC8535ECVTANG(A)	
1000/400/400	MPC8535BVTAQG(A)	MPC8535EBVTAQG(A)	MPC8535CVTAQG(A)	MPC8535ECVTAQG(A)	
1250/500/500	MPC8535BVTATH(A)	MPC8535EBVTATH(A)	MPC8535CVTATH(A)	MPC8535ECVTATH(A)	
1250/500/667	MPC8535BVTATLA	MPC8535EBVTATLA	MPC8535CVTATLA	MPC8535ECVTATLA	

Note:

1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A