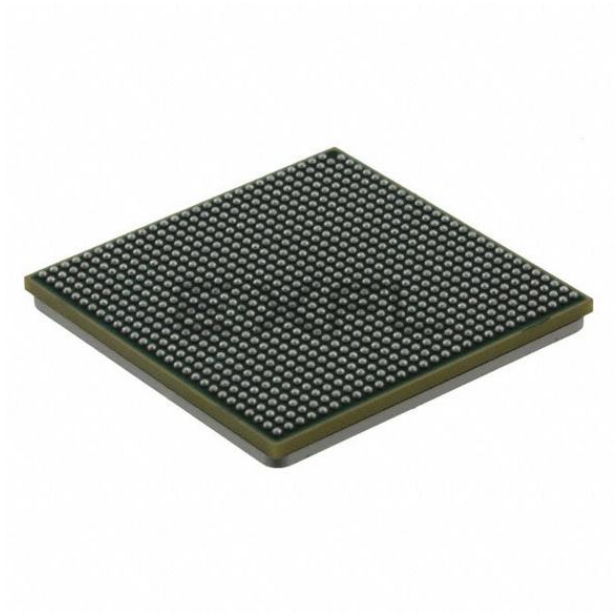

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8535avtaqg

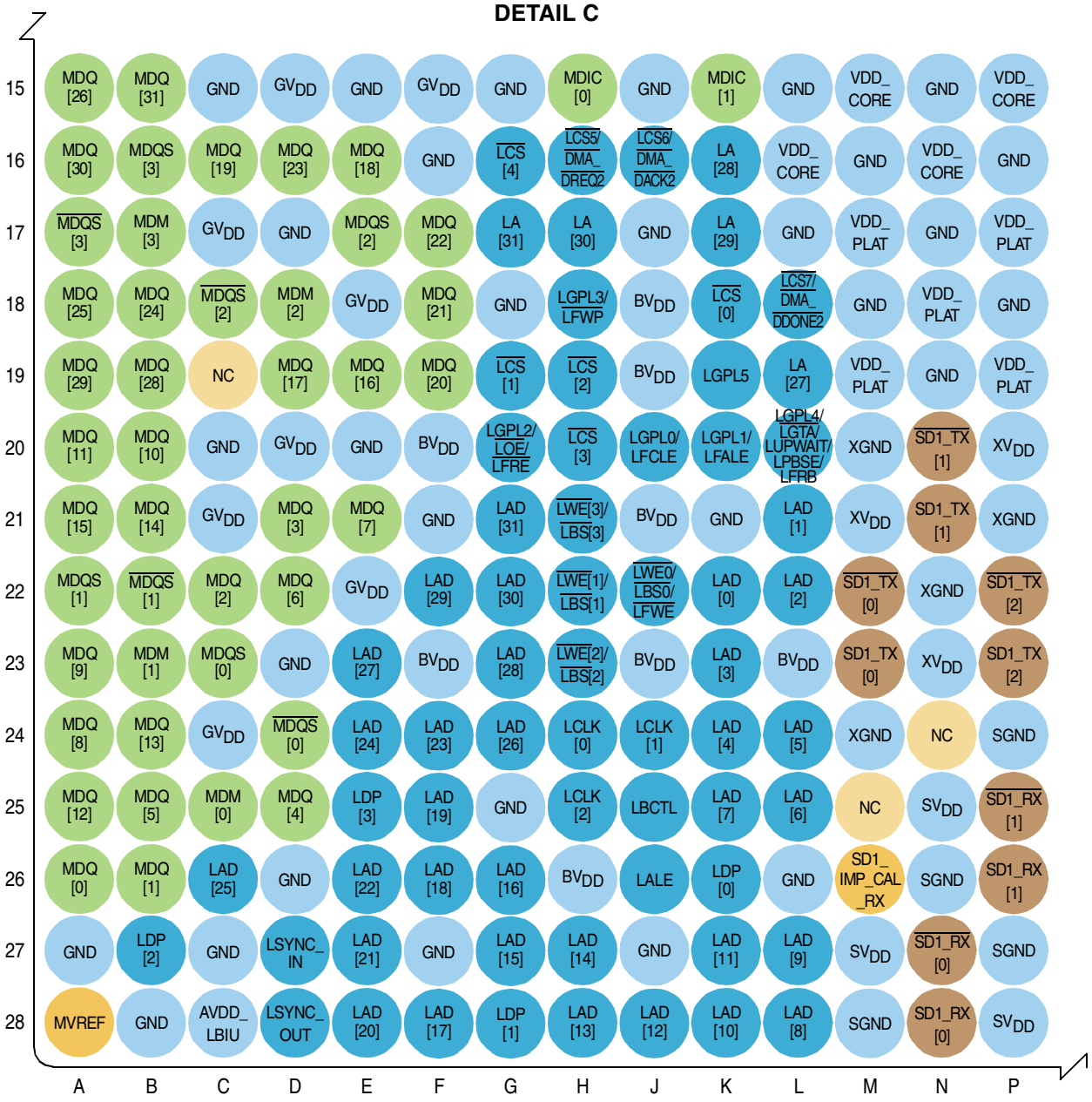


Figure 5. Chip Pin Map Detail C

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Programmable Interrupt Controller					
$\overline{\text{MCP}}$	Machine check processor	Y14	I	OV_{DD}	—
$\overline{\text{UDE}}$	Unconditional debug event	AB14	I	OV_{DD}	—
IRQ[0:8]	External interrupts	AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ[3]}}$	External interrupt/DMA request	AE13	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK[3]}}$	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE[3]}}$	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	Interrupt output	AC17	O	OV_{DD}	2,4
Ethernet Management Interface					
EC_MDC	Management data clock	Y10	O	OV_{DD}	5,9,22
EC_MDIO	Management data In/Out	Y11	I/O	OV_{DD}	—
Gigabit Reference Clock					
EC_GTX_CLK125	Reference clock	AA6	I	LV_{DD}	31
Three-Speed Ethernet Controller (Gigabit Ethernet 1)					
TSEC1_TXD[7:0]	Transmit data	AA8,AA5,Y8,Y5,W3, W5,W4,W6	O	LV_{DD}	5,9,22
TSEC1_TX_EN	Transmit Enable	W1	O	LV_{DD}	23
TSEC1_TX_ER	Transmit Error	AB5	O	LV_{DD}	5,9
TSEC1_TX_CLK	Transmit clock In	AB4	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit clock Out	W2	O	LV_{DD}	—
TSEC1_CRS	Carrier sense	AA9	I/O	LV_{DD}	17
TSEC1_COL	Collision detect	AB6	I	LV_{DD}	—
TSEC1_RXD[7:0]	Receive data	AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2	I	LV_{DD}	—
TSEC1_RX_DV	Receive data valid	AA1	I	LV_{DD}	—
TSEC1_RX_ER	Receive data error	Y9	I	LV_{DD}	—
TSEC1_RX_CLK	Receive clock	AA3	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)					
TSEC3_TXD[7:0]	Transmit data	T12,V8,U8,V9,T8,T7, T5,T6	O	TV_{DD}	5,9,22
TSEC3_TX_EN	Transmit Enable	V5	O	TV_{DD}	23
TSEC3_TX_ER	Transmit Error	U9	O	TV_{DD}	5,9

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
UART_SOUT[0:1]	Transmit data	AF10,AA12	O	OV_{DD}	5,9,22, 10,29
I^2C interface					
IIC1_SCL	Serial clock	AG21	I/O	OV_{DD}	4,21,29
IIC1_SDA	Serial data	AH22	I/O	OV_{DD}	4,21,29
IIC2_SCL	Serial clock	AH15	I/O	OV_{DD}	4,21,29
IIC2_SDA	Serial data	AG14	I/O	OV_{DD}	4,21,29
SerDes1(x4)					
SD1_TX[7:4]	Transmit Data (+)	Y23,W21,V23,U21	O	XV_{DD}	—
$\overline{\text{SD1\_TX}}$[7:4]	Transmit Data(-)	Y22,W20,V22,U20	O	XV_{DD}	—
SD1_RX[7:4]	Receive Data(+)	AC28,AB26,AA28,Y26	I	XV_{DD}	—
$\overline{\text{SD1\_RX}}$[7:4]	Receive Data(–)	AC27,AB25,AA27,Y25	I	XV_{DD}	—
Reserved	—	R21,P23,N21,M23, R20,P22,N20,M22	—	—	18
Reserved	—	T26,R28,P26,N28, T25,R27,P25,N27	—	—	33
SD1_PLL_TPD	PLL test point Digital	V28	O	XV_{DD}	18
SD1_REF_CLK	PLL Reference clock	U28	I	XV_{DD}	—
$\overline{\text{SD1\_REF\_CLK}}$	PLL Reference clock complement	U27	I	XV_{DD}	—
Reserved	—	T22	—	—	18
Reserved	—	T23	—	—	18
SerDes2(x1)					
SD2_TX[0]	Transmit data(+)	P11	O	$X2V_{DD}$	—
$\overline{\text{SD2\_TX[0]}}$	Transmit data(-)	P12	O	$X2V_{DD}$	—
SD2_RX[0]	Receive data(+)	P6	I	$X2V_{DD}$	—
$\overline{\text{SD2\_RX[0]}}$	Receive data(-)	P7	I	$X2V_{DD}$	—
Reserved	—	M11,M12	—	—	18
Reserved	—	N8, N9	—	—	34
SD2_PLL_TPD	PLL test point Digital	L7	O	$X2V_{DD}$	18
SD2_REF_CLK	PLL Reference clock	M6	I	$X2V_{DD}$	—
$\overline{\text{SD2\_REF\_CLK}}$	PLL Reference clock complement	M7	I	$X2V_{DD}$	—
Reserved	—	L8	—	$X2V_{DD}$	18
Reserved	—	L9	—	$X2V_{DD}$	18

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND	SerDes 1 Transceiver core logic GND (xcorevss)	M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28	—	—	—
X2GND	SerDes 2 Transceiver pad GND (xpadvss)	R12,M10,N11,L12	—	—	—
S2GND	SerDes 2 Transceiver core logic GND (xcorevss)	P8,P9,N6,M8	—	—	—
AGND_SRDS	SerDes 1 PLL GND	V27	—	—	—
AGND_SRDS2	SerDes 2 PLL GND	T2	—	—	—
SENSEVSS	GND Sensing	V16	—	—	13
Analog Signals					
MVREF	SSTL2 reference voltage	A28	Reference voltage for DDR	GVDD/2	—
SD1_IMP_CAL_RX	Rx impedance calibration	M26	—	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	Tx impedance calibration	AE28	—	100Ω (±1%) to GND	—
SD1_PLL_TPA	PLL test point analog	V26	—	AVDD_SRDS analog	18
SD2_IMP_CAL_RX	Rx impedance calibration	R7	—	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	Tx impedance calibration	L6	—	100Ω (±1%) to GND	—
SD2_PLL_TPA	PLL test point analog	T3	—	AVDD_SRDS2 analog	18
Reserved	—	R4	—	—	—
Reserved	—	R5	—	—	—
No Connect Pins					
NC	—	C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9	—	—	—

2.6 DDR2 and DDR3 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR2 SDRAM is GV_{DD}(type) = 1.8 V and DDR3 SDRAM is GV_{DD}(type) = 1.5 V.

2.6.1 DDR2 and DDR3 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the chip when interfacing to DDR2 SDRAM.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF}+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the chip. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller of the chip when interfacing to DDR3 SDRAM.

Table 13. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	—
Output leakage current	I_{OZ}	–50	50	μA	3

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 26. FIFO Mode Transmit AC Timing Specification (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}[1]	0.5	—	3.0	ns

Note:

1. Data valid t_{FITDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time – Max Hold)
2. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, "Platform to FIFO Restrictions," for more detailed description.

Table 27. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period[1]	t_{FIR}	6.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Note:

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, "Platform to FIFO Restrictions," for more detailed description.

Timing diagrams for FIFO appear in the following figures.

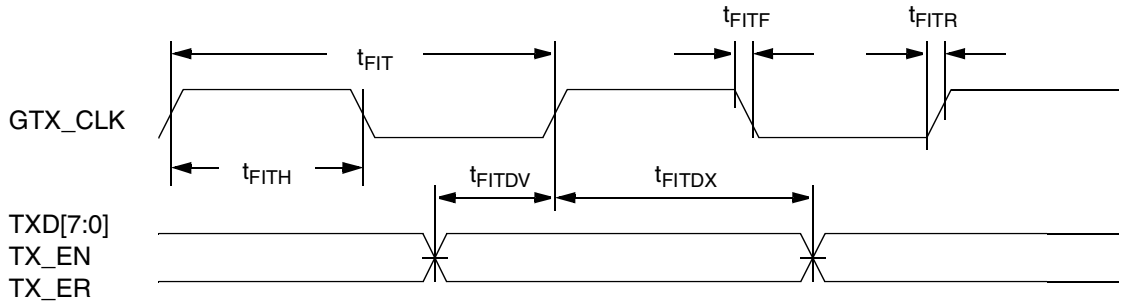


Figure 14. FIFO Transmit AC Timing Diagram

This figure shows the GMII transmit AC timing diagram.

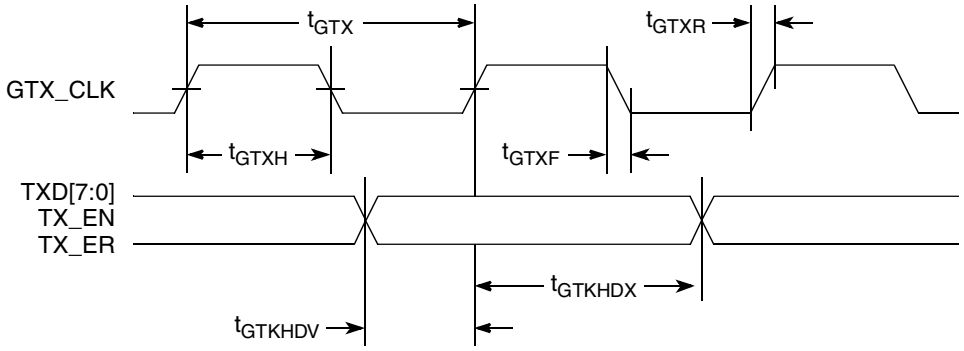


Figure 16. GMII Transmit AC Timing Diagram

2.9.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

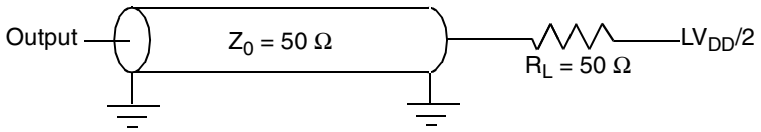


Figure 17. eTSEC AC Test Load

2.11.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 46. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.11.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the chip.

Table 47. USB General Timing Parameters[6]

Parameter	Symbol [1]	Min	Max	Unit	Notes
usb clock cycle time	t_{USCK}	15	—	ns	2-5
Input setup to usb clock - all inputs	t_{USIVKH}	4	—	ns	2-5
input hold to usb clock - all inputs	t_{USIXKH}	1	—	ns	2-5
usb clock to output valid - all outputs	t_{USKHOV}	—	7	ns	2-5
Output hold from usb clock - all outputs	t_{USKHOX}	2	—	ns	2-5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USBn_DIR pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 50. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	—	1.71	1.89	V
High-level input voltage	V_{IH}	—	0.65*BV_{DD}	0.3+BV_{DD}	V
Low-level input voltage	V_{IL}	—	–0.3	0.35*BV_{DD}	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	-15	10	μA
High-level output voltage	V_{OH}	I_{OH} = –100 μA	BV_{DD} – 0.2	—	V
		I_{OH} = –2 mA	BV_{DD} – 0.45	—	
Low-level output voltage	V_{OL}	I_{OH} = 100 μA	—	0.2	V
		I_{OH} = 2 mA	—	0.45	

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

2.12.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V DC. For information about the frequency range of local bus see Section 2.23.1, “Clock Ranges.”

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.4	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3

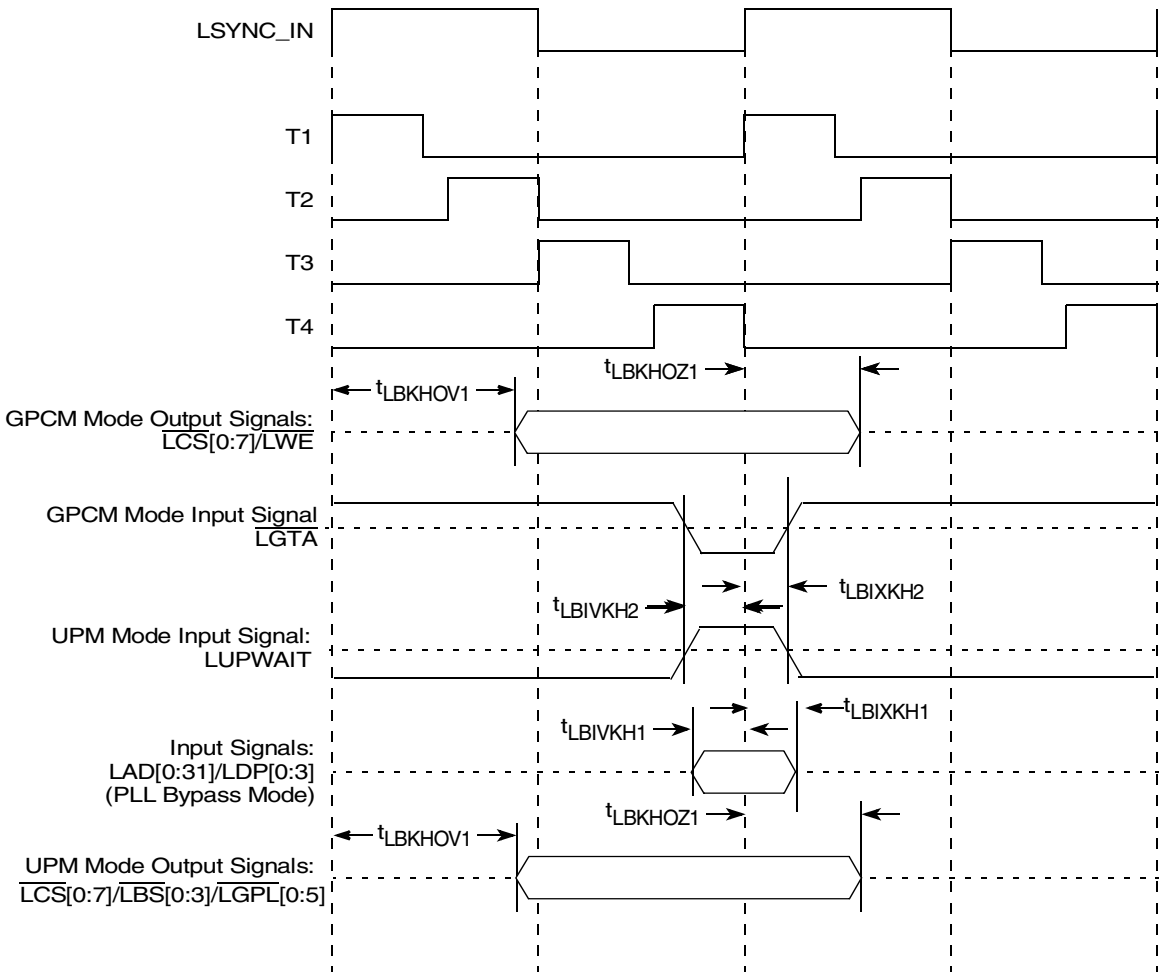


Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 * OVDD	OVDD+0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.25 * OVDD	V	—
Input/Output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—
Output high voltage	V_{OH}	I_{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	—

Table 57. JTAG DC Electrical Characteristics (continued)

Parameter	Symbol [1]	Min	Max	Unit
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

This table provides the JTAG AC timing specifications as defined in the following figures.

Table 58. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions (see Table 3).

Parameter	Symbol [1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times:	t_{JTDVKH}	4	—	ns	
Input hold times:	t_{JTDXKH}	10	—	ns	
Output Valid times:	t_{JTKLDV}	—	10	ns	3
Output hold times:	t_{JTKLDX}	0	—	ns	3

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3.) The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

Table 59. Reference Clock Input Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD2_REF_CLK/_B reference clock cycle time	t_{CLK_REF}	100	—	150	MHz	1
SD2_REF_CLK/_B frequency tolerance	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/_B rise/fall time (80%-20%)	$t_{CLK\_RISE}/t_{CLK\_FALL}$	—	—	1	ns	—
SD_REF_CLK/_B duty cycle (@50% X2VDD)	t_{CLK_DUTY}	45	50	55	%	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter (peak-to-peak)	t_{CLK_PJ}	–50	—	+50	ps	2,3

Note:

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

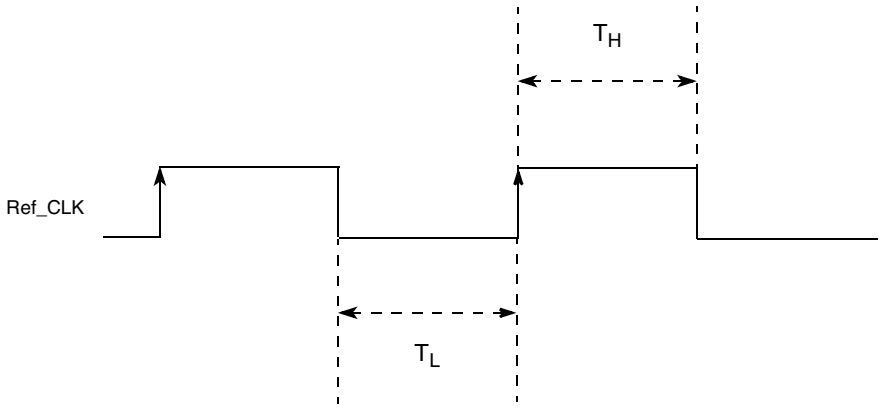


Figure 49. Reference Clock Timing Waveform

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 65. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	7.5	ns	3
GPIO outputs—minimum pulse width	t_{GTOWID}	12	ns	—

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

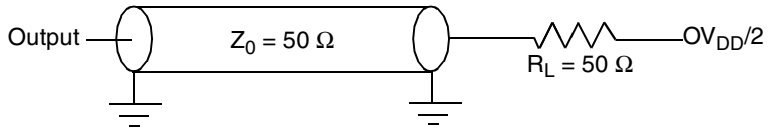


Figure 53. GPIO AC Test Load

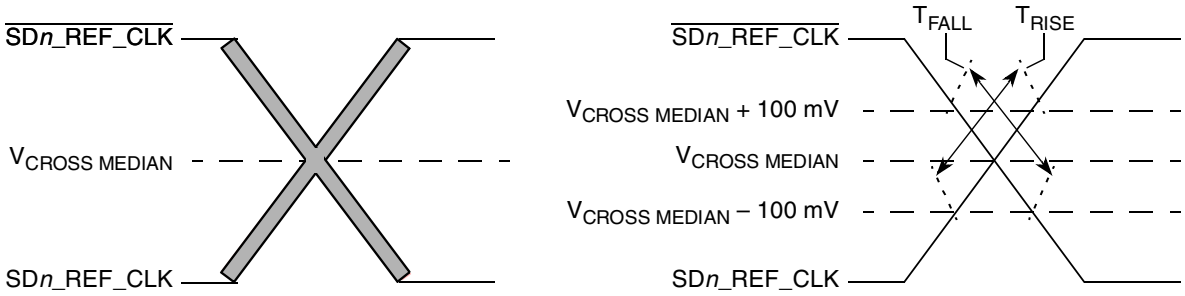


Figure 67. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 2.9.3.2, "AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK"
- Section 2.21.2, "AC Requirements for PCI Express SerDes Clocks"

2.20.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

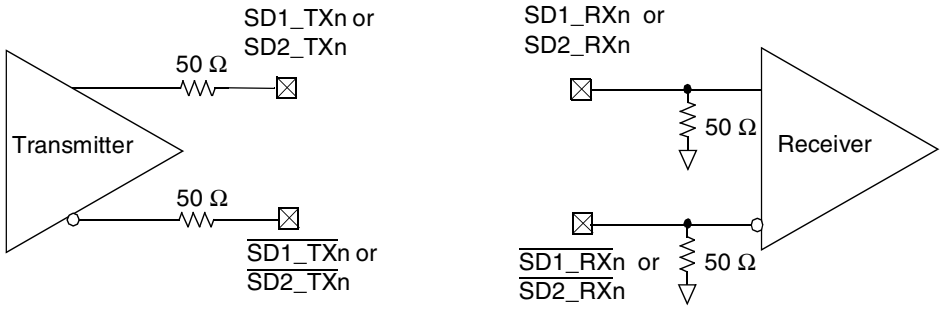


Figure 68. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SATA or SGMII) in this document based on the application usage:

- Section 2.9.3, "SGMII Interface Electrical Characteristics"
- Section 2.21, "PCI Express"
- Section 2.16, "Serial ATA (SATA)"

Please note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

2.21.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 69 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

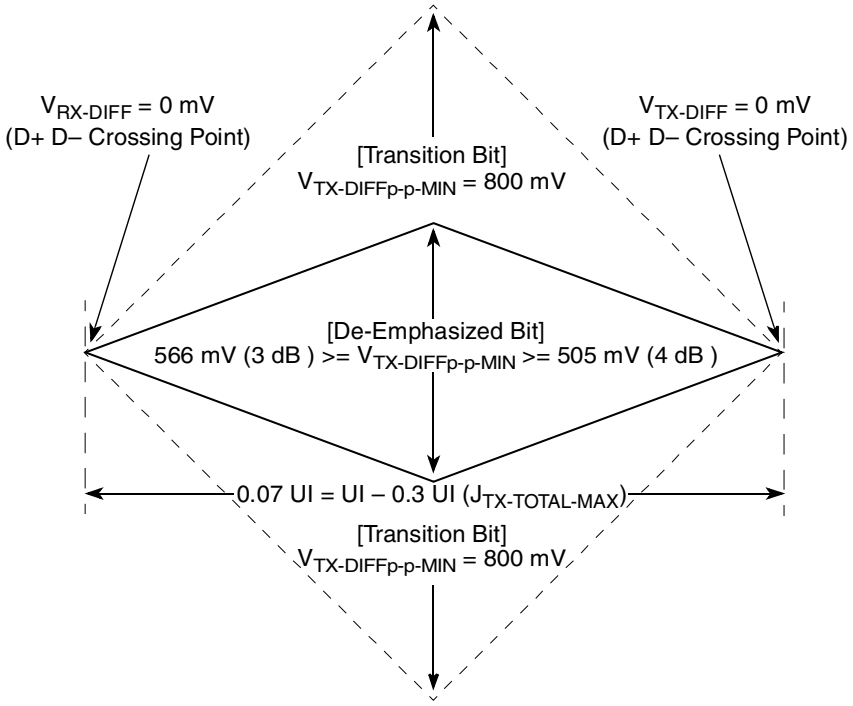


Figure 69. Minimum Transmitter Timing and Voltage Output Compliance Specifications

2.23.1 Clock Ranges

This table provides the clocking specifications for the processor cores and Table 74 provides the clocking specifications for the memory bus.

Table 73. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	600 MHz		800 MHz		1000 MHz		1250 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	600	600	600	800	600	1000	600	1250	MHz	1, 2
CCB frequency	400	400	400	400	333	400	333	500		
DDR Data Rate	400	400	400	400	400	400	400	500		

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, “CCB/SYSCLK PLL Ratio,” Section 2.23.3, “e500 Core PLL Ratio,“and Section 2.23.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. This table provides the clocking specifications for the memory bus.

Table 74. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	600, 800, 1000, 1250			
	Min	Max		
DDR Memory bus clock speed	200	250	MHz	1, 2, 3, 4

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, “CCB/SYSCLK PLL Ratio,” Section 2.23.3, “e500 Core PLL Ratio,” and Section 2.23.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The Memory bus clock refers to the chip’s memory controllers’ MCK[0:5] and $\overline{\text{MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 2.23.4, “DDR/DDRCLK PLL Ratio.” The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

This figure shows the PLL power supply filter circuit.

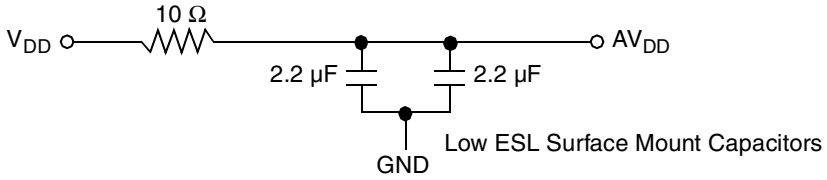
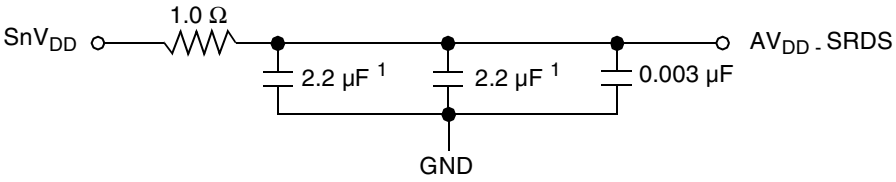


Figure 75. Chip PLL Power Supply Filter Circuit

The AV_{DD}_SRDS*n* signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 76. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up

Figure 76. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD} should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

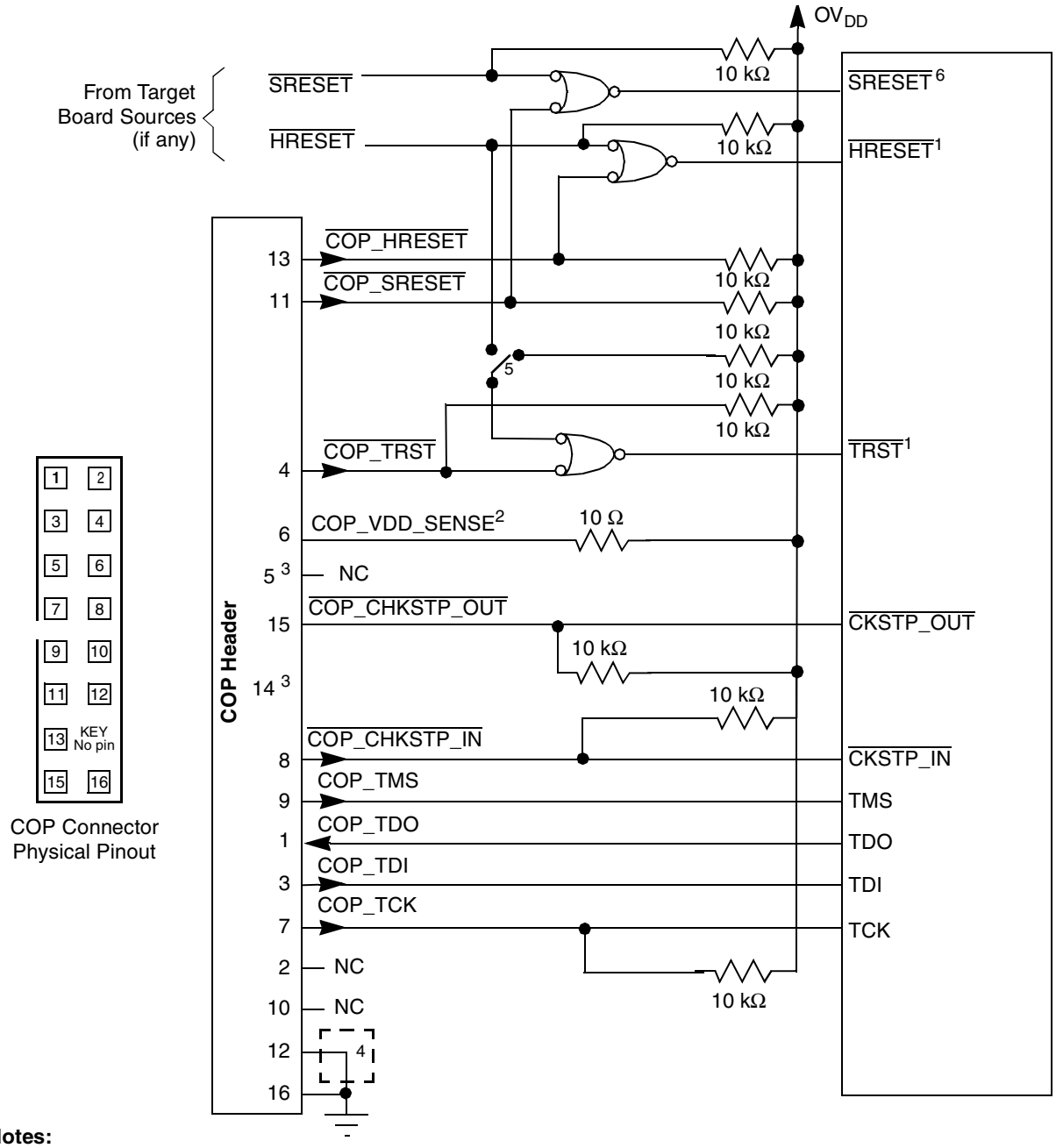
3.3 Pin States in Deep Sleep State

In all low power mode by default, all input and output pads remain driven as per normal functional operation. The inputs remain enabled.

The exception is that in Deep Sleep mode, GCR[DEEPSLEEP_Z] can be used to tristate a subset of output pads, and disable the receivers of input pads as defined in Table 1. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for details.

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, this chip can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the chip. These decoupling capacitors should receive their power from separate V_{DD},TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the chip using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it should be routed with short and large trace to minimize the inductance.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 78. JTAG Interface Connection

The following pins must be connected to XGND if not used:

- SD1_RX[7:4]
- $\overline{\text{SD1\_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

3.11.3 SerDes 2 Interface Entirely Unused

If the high-speed SerDes 2 interface (SGMII/ SATA) is not used at all, the unused pin should be terminated as described in this section. There are several Reserved pins that need to be either left floating or connected to X2GND. See SerDes2 in Table 1Table 1 for details.

The following pins must be left unconnected (float):

- SD2_TX[0]
- $\overline{\text{SD2\_TX[0]}}$
- Reserved pins L8, L9

The following pins must be connected to X2GND:

- SD2_RX[0]
- $\overline{\text{SD2\_RX[0]}}$
- SD2_REF_CLK
- $\overline{\text{SD2\_REF\_CLK}}$

The POR configuration pin cfg_srds2_prtcl[0:2] on TSEC1_TXD[2], TSEC3_TXD[2], TSEC_1588_PUSLE_OUT1 can be used to power down SerDes 2 block for power saving. Note that both S2VDD and X2VDD must remain powered.

4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, “Part Numbers Fully Addressed by this Document.”

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