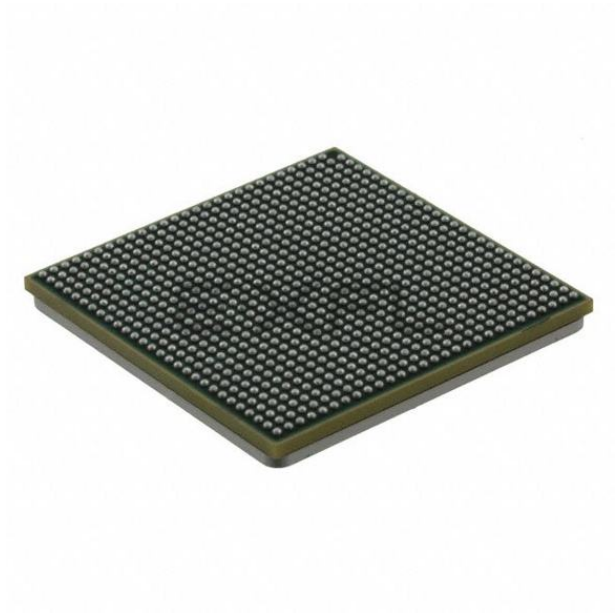

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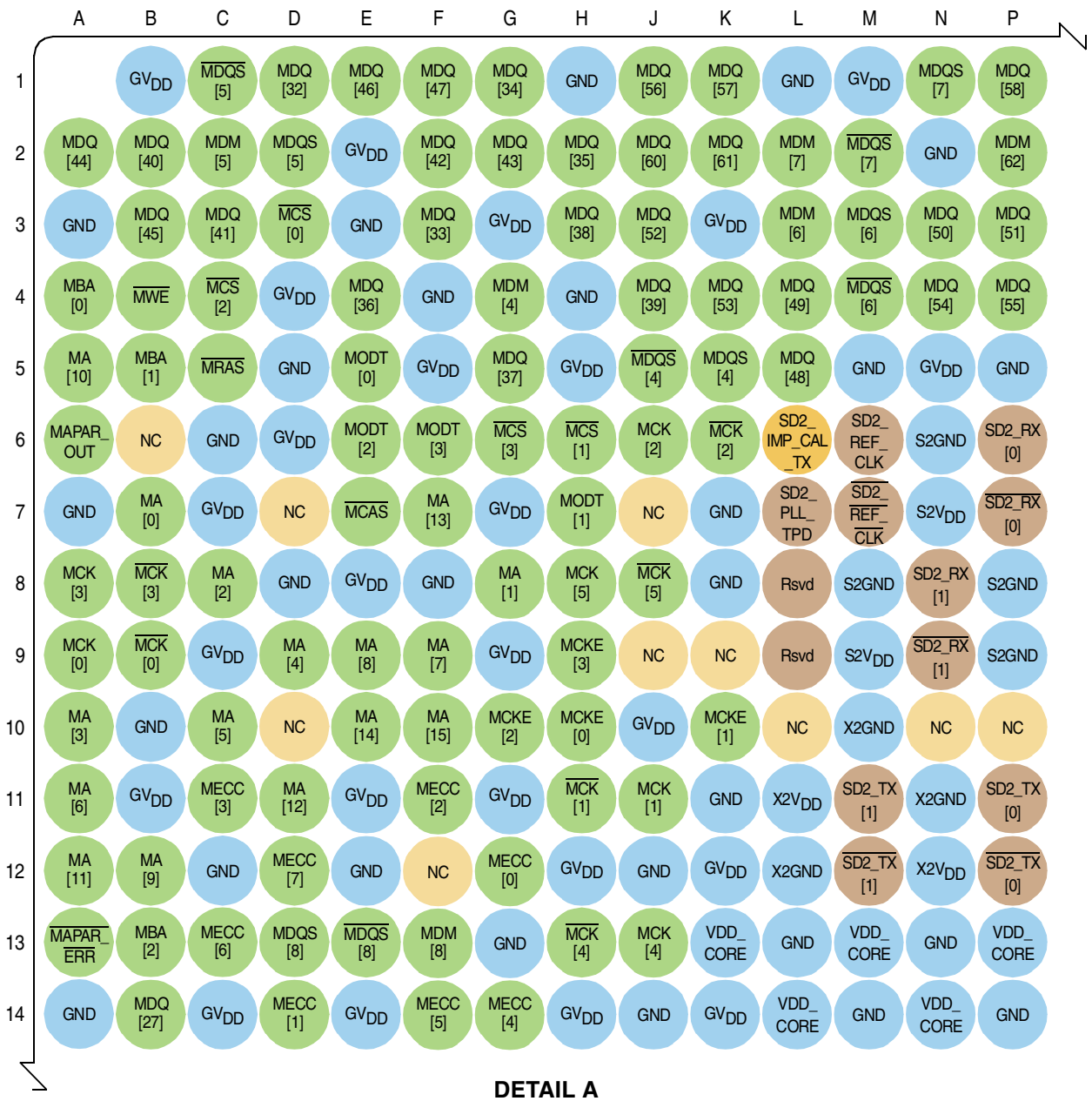
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8535avtatha



DETAIL A

Figure 3. Chip Pin Map Detail A

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
General-Purpose Input/Output					
GPIO[0:1]/PCI1_REQ[3:4]	GPIO/PCI request	Y15,AE15	I/O	OV_{DD}	—
GPIO[2:3]/PCI1_GNT[3:4]	GPIO/PCI grant	AA15,AC14	I/O	OV_{DD}	—
GPIO[4]/SDHC_CD	GPIO/SDHC card detection	AH11	I/O	OV_{DD}	—
GPIO[5]/SDHC_WP	GPIO/SDHC write protection	AG10	I/O	OV_{DD}	32
GPIO[6]/USB1_PCTL0	GPIO/USB1 PCTL0	AC3	I/O	OV_{DD}	—
GPIO[7]/USB1_PCTL1	GPIO/USB1 PCTL1	AC4	I/O	OV_{DD}	—
GPIO[8]/USB2_PCTL0	GPIO/USB2 PCTL0	AG9	I/O	OV_{DD}	—
GPIO[9]/USB2_PCTL1	GPIO/USB2 PCTL1	AC9	I/O	OV_{DD}	—
GPIO[10:11] /DMA_DACK[0:1]	GPIO/DMA Ack	AD6,AE10	I/O	OV_{DD}	—
GPIO[12:13] /DMA_DDONE[0:1]	GPIO/DMA done	AA11,AB11	I/O	OV_{DD}	—
GPIO[14:15] /DMA_DREQ[0:1]	GPIO/DMA request	AB10,AD11	I/O	OV_{DD}	—
System Control					
HRESET	Hard reset	AG16	I	OV_{DD}	—
HRESET_REQ	Hard reset - request	AG15	O	OV_{DD}	22
SRESET	Soft reset	AG19	I	OV_{DD}	—
CKSTP_IN	CheckStop in	AG18	I	OV_{DD}	—
CKSTP_OUT	CheckStop Output	AH17	O	OV_{DD}	2,4
Debug					
TRIG_IN	Trigger in	W19	I	OV_{DD}	—
TRIG_OUT/READY /QUIESCE	Trigger out/Ready/Quiesce	V19	O	OV_{DD}	22
MSRCID[0:1]	Memory debug source port ID	W12,W13	O	OV_{DD}	6,9
MSRCID[2:4]	Memory debug source port ID	V12, W14,W11	O	OV_{DD}	6,9,22
MDVAL	Memory debug data valid	V13	O	OV_{DD}	6,22
CLK_OUT	Clock Out	W15	O	OV_{DD}	11
Clock					
RTC	Real time clock	AF15	I	OV_{DD}	—
SYSCLK	System clock / PCI clock	AH14	I	OV_{DD}	—
DDRCLK	DDR clock	AC13	I	OV_{DD}	30
JTAG					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST\_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

25. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as “No Connect” or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
26. When operating in DDR2 mode, connect MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect MDIC[0] to ground through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
27. Connect to GND through a pull down 1 kΩ resistor.
28. It must be the same as VDD_CORE
29. The output pads are tristated and the receivers of pad inputs are disabled during the Deep Sleep state when GCR[DEEPSLEEP_Z] =1.
30. DDRCLK input is only required when the DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *MPC8536E PowerQUICC III Integrated Host Processor Family Reference Manual* , Table 4-3 in section 4.2.2 “Clock Signals”, section 4.4.3.2 “DDR PLL Ratio” and Table 4-10 “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
31. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
32. $\overline{\text{SDHC\_WP}}$ is active low signal, which follows SDHC Host controller specification. However, it is reversed polarity for SD/MMC card specification.
33. Must connect to XGND.
34. Must connect to X2GND
35. For systems which boot from Local Bus(GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required.

2 Electrical Characteristics

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

This figure shows the MII transmit AC timing diagram.

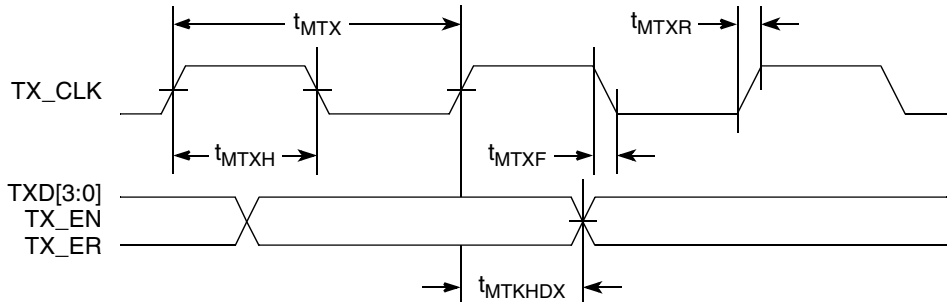


Figure 19. MII Transmit AC Timing Diagram

2.9.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 31. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

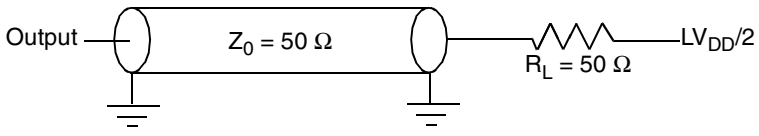


Figure 20. eTSEC AC Test Load

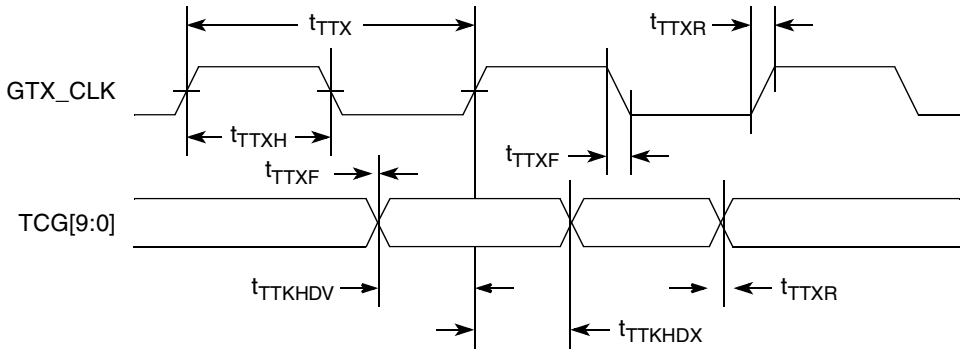


Figure 22. TBI Transmit AC Timing Diagram

2.9.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition[2]	Symbol [1]	Min	Typ	Max	Unit
Clock period for TBI Receive Clock 0, 1	t_{TRX}	—	16.0	—	ns
Skew for TBI Receive Clock 0, 1	t_{SKTRX}	7.5	—	8.5	ns
Duty cycle for TBI Receive Clock 0, 1	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1	t_{TRDXKH}	1.5	—	—	ns
Clock rise time (20%-80%) for TBI Receive Clock 0, 1	t_{TRXR}	0.7	—	2.4	ns
Clock fall time (80%-20%) for TBI Receive Clock 0, 1	t_{TRXF}	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. The signals “TBI Receive Clock 0” and “TBI Receive Clock 1” refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

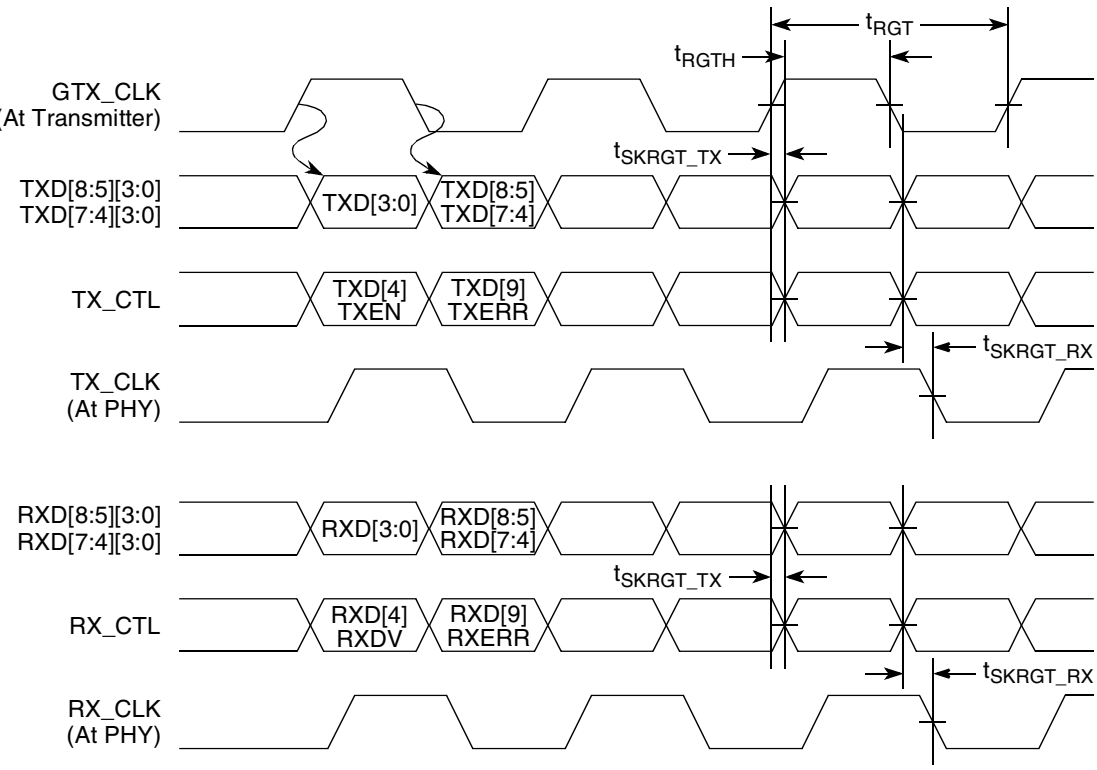


Figure 25. RGMII and RTBI AC Timing and Multiplexing Diagrams

2.9.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.9.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in the following table.

Table 36. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps

2.9.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 31 shows the SGMII Receiver Input Compliance Mask eye diagram.

Table 42. SGMII Receive AC Timing Specifications

At recommended operating conditions with $X2V_{DD}$ = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the chip transmitter outputs.

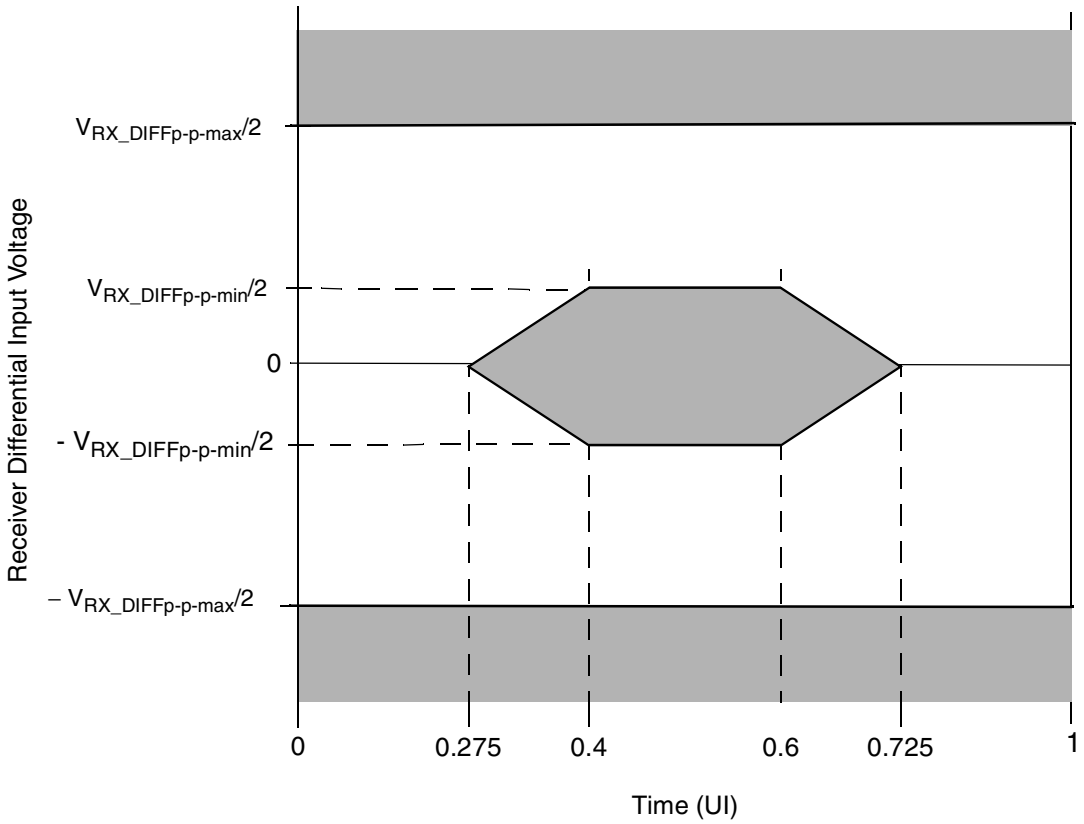


Figure 31. SGMII Receiver Input Compliance Mask

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC) (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	—	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	—	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	—	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 53. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.9	—	ns	3

Table 54. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	0.5	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	0.5	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.5	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	—	2.2	ns	4,8
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	—	2.2	ns	4,8
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.1	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.1	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. These timing parameters for PLL bypass mode are defined in the opposite direction of the PLL enabled output hold timing parameters.

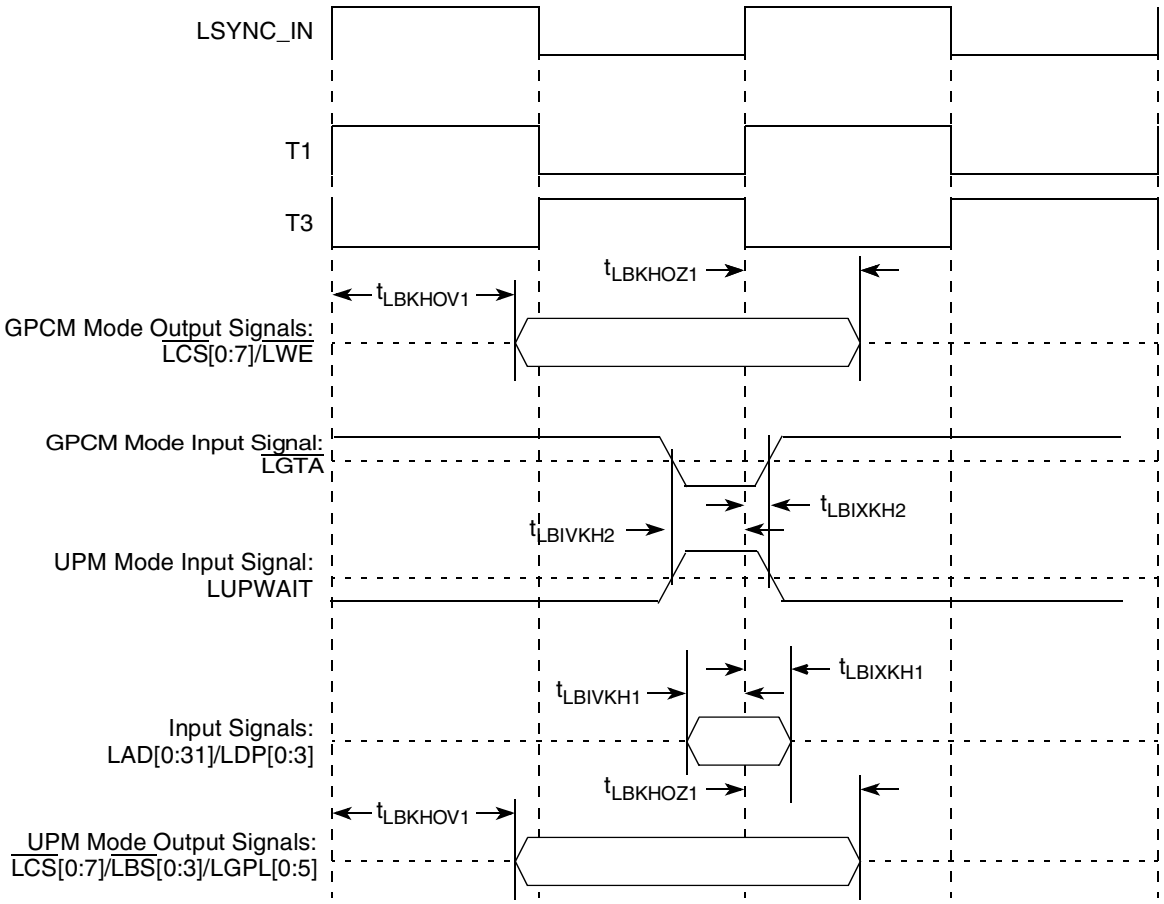


Figure 41. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4(PLL Enabled)

This figure provides the eSDHC clock input timing diagram.

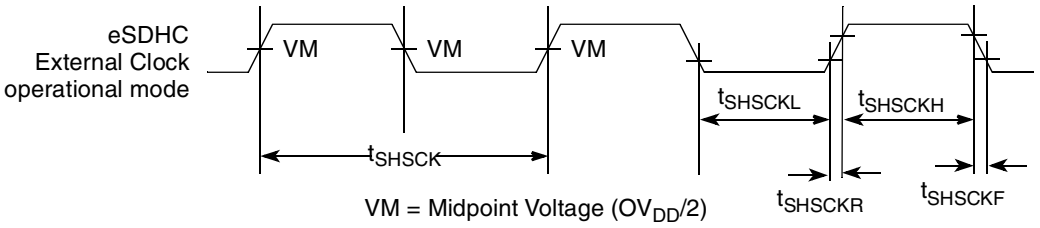


Figure 43. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

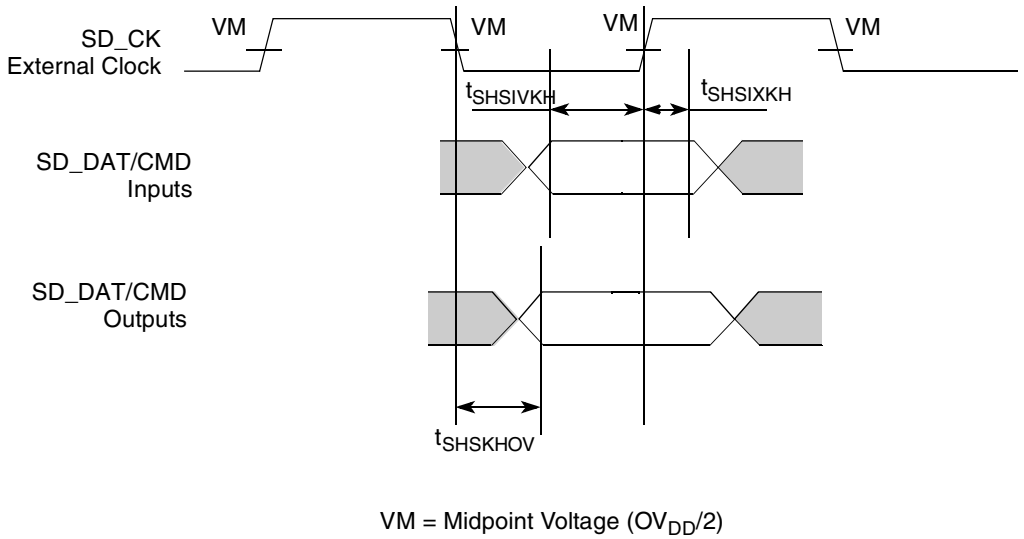


Figure 44. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.14 Programmable Interrupt Controller (PIC)

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

2.15 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

2.15.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Table 57. JTAG DC Electrical Characteristics

Parameter	Symbol [1]	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V

Table 57. JTAG DC Electrical Characteristics (continued)

Parameter	Symbol [1]	Min	Max	Unit
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

This table provides the JTAG AC timing specifications as defined in the following figures.

Table 58. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions (see Table 3).

Parameter	Symbol [1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times:	t_{JTDVKH}	4	—	ns	
Input hold times:	t_{JTDXKH}	10	—	ns	
Output Valid times:	t_{JTKLDV}	—	10	ns	3
Output hold times:	t_{JTKLDX}	0	—	ns	3

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3.) The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

Table 59. Reference Clock Input Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD2_REF_CLK/_B reference clock cycle time	t_{CLK_REF}	100	—	150	MHz	1
SD2_REF_CLK/_B frequency tolerance	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/_B rise/fall time (80%-20%)	$t_{CLK\_RISE}/t_{CLK\_FALL}$	—	—	1	ns	—
SD_REF_CLK/_B duty cycle (@50% X2VDD)	t_{CLK_DUTY}	45	50	55	%	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter (peak-to-peak)	t_{CLK_PJ}	–50	—	+50	ps	2,3

Note:

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

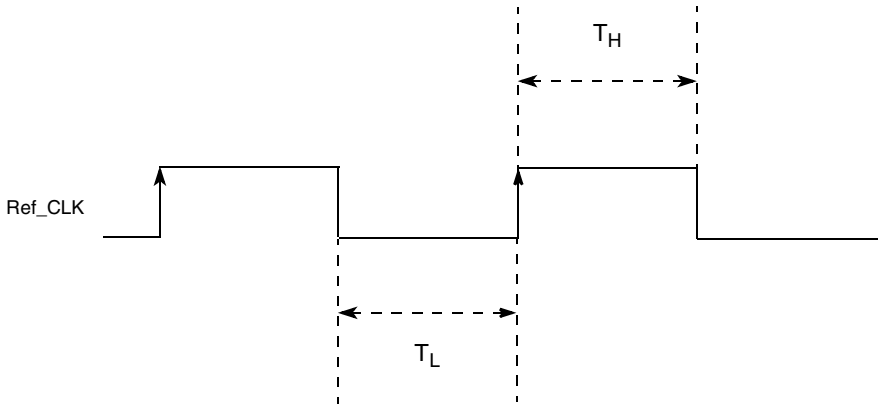


Figure 49. Reference Clock Timing Waveform

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 65. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	7.5	ns	3
GPIO outputs—minimum pulse width	t_{GTOWID}	12	ns	—

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

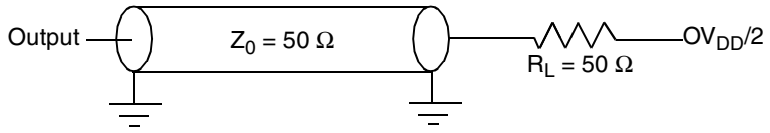


Figure 53. GPIO AC Test Load

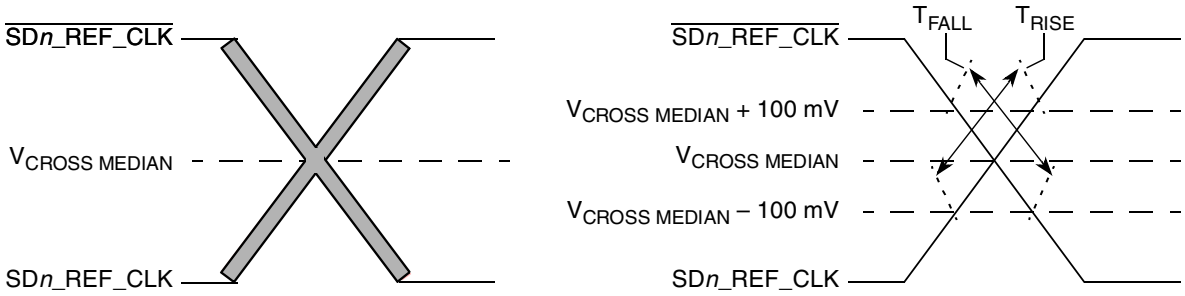


Figure 67. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 2.9.3.2, "AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK"
- Section 2.21.2, "AC Requirements for PCI Express SerDes Clocks"

2.20.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

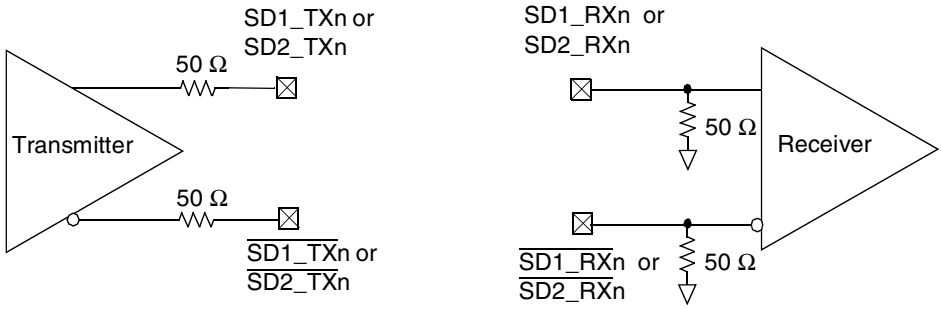


Figure 68. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SATA or SGMII) in this document based on the application usage:

- Section 2.9.3, "SGMII Interface Electrical Characteristics"
- Section 2.21, "PCI Express"
- Section 2.16, "Serial ATA (SATA)"

Please note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

2.21.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 69 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

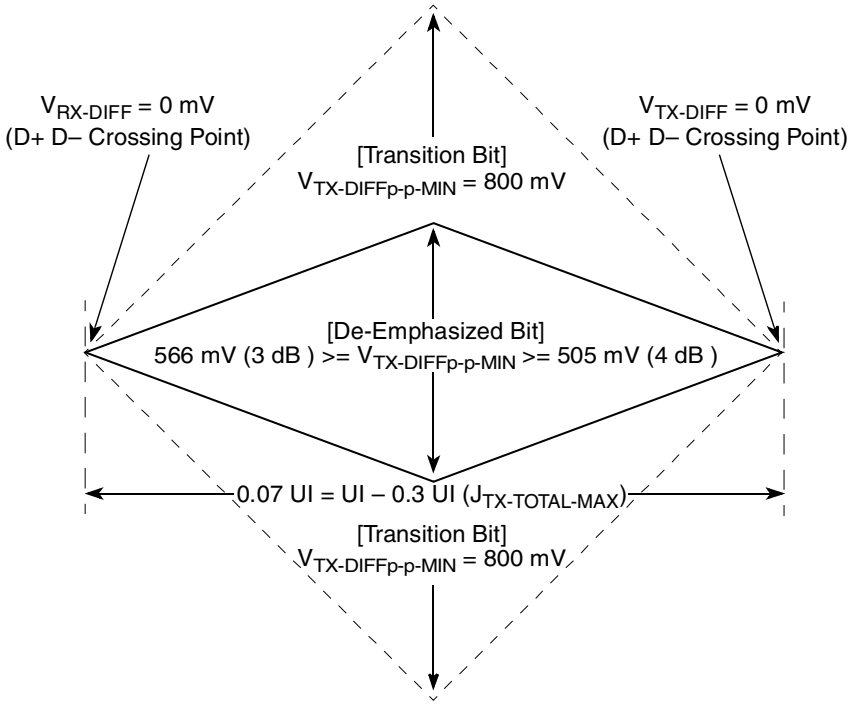


Figure 69. Minimum Transmitter Timing and Voltage Output Compliance Specifications

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Table 77. DDR Clock Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	cfg_ddr_pll[0:2]	000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, “CCB/SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, “e500 Core PLL Ratio.”
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, “DDR/DDRCLK PLL Ratio.”

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

3.10 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredicatable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The chip requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 78 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 79, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 79 is common to all known emulators.

3.10.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 78. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.