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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535bvjakga

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Assignments and Reset States

This table provides the pin-out listing for the 783 FC-PBGA package.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
		PCI			
PCI1_AD[31:0]	Muxed Address / data	AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26	I/O	OV _{DD}	_
PCI1_C_BE[3:0]	Command/Byte Enable	AD18, AD20,AD22, AH25	I/O	OV _{DD}	29
PCI1_PAR	Parity	AC22	I/O	OV _{DD}	29
PCI1_FRAME	Frame	AE20	I/O	OV _{DD}	2,29
PCI1_TRDY	Target Ready	AF21	I/O	OV _{DD}	2,29
PCI1_IRDY	Initiator Ready	AB20	I/O	OV _{DD}	2,29
PCI1_STOP	Stop	AD21	I/O	OV _{DD}	2,29
PCI1_DEVSEL	Device Select	AC21	I/O	OV _{DD}	2,29
PCI1_IDSEL	Init Device Select	AE16	I	OV _{DD}	29
PCI1_PERR	Parity Error	AB21	I/O	OV _{DD}	2,29
PCI1_SERR	System Error	AF22	I/O	OV _{DD}	2,4,29
PCI1_REQ[4:3]/GPIO[1:0]	Request	AE15,Y15	I	OV _{DD}	—
PCI1_REQ[2:1]	Request	AF13,W16	I	OV _{DD}	29
PCI1_REQ[0]	Request	AA16	I/O	OV _{DD}	29
PCI1_GNT[4:3]/GPIO[3:2]	Grant	AC14, AA15	0	OV _{DD}	
PCI1_GNT[2:1]	Grant	AF14,Y16	0	OV _{DD}	5,9,25,29
PCI1_GNT[0]	Grant	W18	I/O	OV _{DD}	29
PCI1_CLK	PCI Clock	AH26	I	OV _{DD}	29

Pin Assignments and Reset States

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
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Notes:

- 1. All multiplexed signals may be listed only once and may not re-occur.
- 2. Recommend a weak pull-up resistor (2–10 K Ω) be placed on this pin to OV_{DD}.
- 3. This pin must always be pulled-high.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
- 8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
- 10.For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V_{DD_CORE}/V_{DD_PLAT}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
- 16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 17. This pin is only an output in FIFO mode when used as Rx Flow Control.
- 18. Do not connect.
- 19.These must be pulled up (100 Ω 1 k Ω) to OVDD.
- 20. Independent supplies derived from board VDD.
- 21. Recommend a pull-up resistor (1 K Ω) be placed on this pin to OV_{DD}.
- 22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP.
- 23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
- 24. General-Purpose POR configuration of user system.

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes		
25. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device.							
26. When operating in DDR2 mode, connect MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect MDIC[0] to ground through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.							
27. Connect to GND through a	pull down 1 k Ω resistor.						
28. It must be the same as \ensuremath{VD}	D_CORE						
29. The output pads are tristate GCR[DEEPSLEEP_Z] =1.	ed and the receivers of pad inp	uts are disabled during th	e Deep Sleer	o state when			
 GCR[DEEPSLEEP_Z] =1. 30. DDRCLK input is only required when the DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the <i>MPC8536E PowerQUIC III Integrated Host Processor Family Reference Manual</i>, Table 4-3 in section 4.2.2 "Clock Signals", section 4.4.3.2 "DD PLL Ratio" and Table 4-10 "DDR Complex Clock PLL Ratio" for more detailed description regarding DDR controller operation in asynchronous and synchronous modes. 							
31 EC GTX CLK125 is a 125	-MHz input clock shared among	n all eTSEC ports in the fo	llowing mode	s GMILTRI	RGMII and		

- 31. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
- 32. SDHC_WP is active low signal, which follows SDHC Host controller specification. However, it is reversed polarity for SD/MMC card specification.
- 33. Must connect to XGND.
- 34. Must connect to X2GND
- 35. For systems which boot from Local Bus(GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required.

2 Electrical Characteristics

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[n]/MCK[n] crossing	t _{MCK}	3.0	5	ns	2
ADDR/CMD output setup with respect to MCK	t _{DDKHAS}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t _{DDKHAX}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
MCS[n] output setup with respect to MCK	t _{DDKHCS}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
MCS[n] output hold with respect to MCK	t _{DDKHCX}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t _{DDKHMH}			ns	4
<= 667 MHz		-0.6	0.6		7
MDQ/MECC/MDM output setup with respect to MDQS	t _{DDKHDS,} t _{DDKLDS}			ps	5
667 MHz		450	—		7
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	^t DDKHDX, ^t DDKLDX			ps	5
667 MHz		450	—		7
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t _{DDKHMP}			ns	6

2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

2.8.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	- 0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD})$	I _{IN}	—	±5	μA
High-level output voltage (OV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	2.4	—	V
Low-level output voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}		0.4	V

Table 22. DUART DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.8.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23	DUART	AC Timing	Specifications
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Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	2
Maximum baud rate	CCB clock/16	baud	2,3
Oversample rate	16	—	4

Notes:

2. CCB clock refers to the platform clock.

3. Actual attainable baud rate will be limited by the latency of interrupt processing.

4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.



Figure 15. FIFO Receive AC Timing Diagram

2.9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

2.9.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 28. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
GTX_CLK clock period	t _{GTK}	_	8.0	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX} 3	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t _{GTXR}	_	—	1.0	ns
GTX_CLK data clock fall time (80%-20%)	t _{GTXF}	_	—	1.0	ns

Notes:

- 1. The symbols used for timing specifications herein follow the pattern t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. Data valid tGTKHDV to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time Max Hold)

This figure shows the GMII transmit AC timing diagram.



Figure 16. GMII Transmit AC Timing Diagram

2.9.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period	t _{GRX}	_	8.0	—	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	35	—	65	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0	_	—	ns
RX_CLK clock rise (20%-80%)	t _{GRXR}	-	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t _{GRXF}	_	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

This figure provides the AC test load for eTSEC.



Figure 17. eTSEC AC Test Load

This figure shows the GMII receive AC timing diagram.



Figure 18. GMII Receive AC Timing Diagram

2.9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.9.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 30. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TX_CLK clock period 10 Mbps	t _{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	—	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t _{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t _{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

Deverseter	Cumhal	Min	Max	11
Parameter	Symbol	IVIIN	wax	Unit
Supply voltage (3.3 V)	OV _{DD}	3.13	3.47	V
Output high voltage (OV _{DD} = Min, I _{OH} = −4.0 mA)	V _{OH}	2.40	OV _{DD} + 0.3	V
Output low voltage (OV _{DD} =Min, I _{OL} = 4.0 mA)	V _{OL}	GND	0.40	V
Input high voltage	V _{IH}	2.0	—	V
Input low voltage	V _{IL}	_	0.90	V
Input high current (OV _{DD} = Max, V _{IN} ¹ = 2.1 V)	Ι _{ΙΗ}	—	40	μA
Input low current (OV _{DD} = Max, V _{IN} = 0.5 V)	IIL	-600	_	μA

Table 44. MII Management DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with OVDD is 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
EC_MDC frequency	f _{MDC}	0.74	2.5	8.3	MHz	2
EC_MDC period	t _{MDC}	120	400	1350	ns	
EC_MDC clock pulse width high	t _{MDCH}	32	—	—	ns	
EC_MDC to EC_MDIO delay	t _{MDKHDX}	(16 * t _{plb_clk})-3	—	(16 * t _{plb_clk})+3	ns	3,5,6
EC_MDIO to EC_MDC setup time	t _{MDDVKH}	5	_		ns	

This figures provide the AC test load and signals for the USB, respectively.



Parameter	Symbol ¹	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}		2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.5	ns	5

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC) (continued)

Note:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6.t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. tLBOTOT is guaranteed with LBCR[AHD] = 0.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BVDD/2.

This table describes the general timing parameters of the local bus interface at $BV_{DD} = 2.5 \text{ V DC}$.

Parameter	Configuration	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	—	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t _{LBKH/} t _{LBK}	43	57	%	_
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	tlbkskew	Ι	150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	t _{LBIVKH1}	1.9	_	ns	3, 4
LUPWAIT input setup to local bus clock	—	t _{LBIVKH2}	1.8	_	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	t _{LBIXKH1}	1.1	_	ns	3, 4
LUPWAIT input hold from local bus clock	—	t _{LBIXKH2}	1.1	_	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t _{LBOTOT}	1.5		ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	t _{LBKHOV1}	_	2.4	ns	_
Local bus clock to data valid for LAD/LDP	—	t _{LBKHOV2}	_	2.5	ns	3
Local bus clock to address valid for LAD	—	t _{LBKHOV3}	_	2.4	ns	3
Local bus clock to LALE assertion	—	t _{LBKHOV4}	_	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	_	t _{LBKHOX1}	0.8	_	ns	3

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)

Table 55. eSDHC interface DC Electrical Characteristics (continued)

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output low voltage	V _{OL}	I _{OL} = 100uA @OVDDmin	—	0.125 * OVDD	V	_
Output high voltage	V _{OH}	I _{OH} = -100 uA	OV _{DD} - 0.2	—	_	2
Output low voltage	V _{OL}	I _{OL} =2 mA	_	0.3	_	2

Notes:

1. The min V_{IL} and V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. Open drain mode for MMC cards only.

2.13.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in the following figure.

Table 56. eSDHC AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full speed/high speed mode MMC Full speed/high speed mode	fsнsск	0	25/50 20/52	MHz	2, 5
SD_CLK clock frequency - identification mode	fsidck	0 100	400	KHz	3, 5
SD_CLK clock low time - High speed/Full speed mode	t _{SHSCKL}	7/10	—	ns	5
SD_CLK clock high time - High speed/Full speed mode	tsнsскн	7/10	—	ns	5
SD_CLK clock rise and fall times	t _{SHSCKR∕} t _{SHSCKF}	_	3	ns	5
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	t _{SHSIVKH}	2.5	_	ns	4,5,6
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	t _{SHSIXKH}	2.5	_	ns	5,6
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	t _{SHSKHOV}	-3	3	ns	5,6

Notes:

- The symbols used for timing specifications herein follow the pattern of t<sub>(first three letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first three letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{FHSKHOV} symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- 2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52MHz for a MMC card.
- 3. 0 Hz means to stop the clock. The given minimum frequency range is for cases were a continuous clock is required.
- 4. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns.
- 5. $C_{CARD} \le 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \le 40$ pF
- 6. The parameter values apply to both full speed and high speed modes.

Table 63. I²C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 \times OV_{DD} and 0.9 \times OV_{DD}(max)	Ι _Ι	-10	10	μA	3
Capacitance for each I/O pin	CI		10	pF	—

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. See the MPC8536E PowerQUICC III Integrated Processor Reference Manual for information on the digital filter used.

3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.17.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 64. I²C AC Electrical Specifications

All values refer to $V_{IH} \, (min)$ and $V_{IL} \, (max)$ levels (see Table 63).

Parameter	Symbol ¹	Min	Max	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	
Low period of the SCL clock	t _{I2CL}	1.3	—	μs	—
High period of the SCL clock	t _{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	—
Data setup time	t _{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I ² C bus devices	t _{i2DXKL}	0	-	μs	2
Data output delay time	t _{I2OVKL}	_	0.9	μs	3
Set-up time for STOP condition	t _{I2PVKH}	0.6	-	μs	—
Rise time of both SDA and SCL signals	t _{l2CR}	—	300	ns	4
Fall time of both SDA and SCL signals	t _{I2CF}		300	ns	4

2.20.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 69. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or $XV_{DD_SRDS2} = 1.0V \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200	—	mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate (SDn_REF_CLK) matching	Rise-Fall Matching		20	%	1, 4

Notes:

- 1. Measurement taken from single ended waveform.
- 2. Measurement taken from differential waveform.
- 3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus SDn_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 66.
- 4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of SDn_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 67.



Figure 66. Differential Measurement Points for Rise and Fall Time

2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

2.21.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 2.20.2, "SerDes Reference Clocks."

2.21.2 AC Requirements for PCI Express SerDes Clocks

This table lists AC requirements.

	Table 70. SD1	REF CLK an	d SD1 REF	CLK AC Re	quirements
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Symbol	Parameter Description	Min	Typical	Мах	Units	Notes
t _{REF}	REFCLK cycle time	—	10		ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	-50	—	50	ps	1,2,3

Notes:

1. Tj at BER of 10E-6 86 ps Max.

2. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 42 ps.

3. Limits from "PCI Express CEM Rev 2.0" and measured per "PCI Express Rj, D, and Bit Error Rates".

2.21.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/-300 ppm tolerance.

2.21.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this chip. For further details as well as the specifications of the transport and data link layer, please use the PCI Express Base Specification. REV. 1.0a document.

2.21.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
V _{TX-DIFFp-p}	Differential Peak-to-Peak Output Voltage	0.8	_	1.2	V	$V_{TX-DIFFp-p} = 2^* V_{TX-D+} - V_{TX-D-} $ See Note 2.

Table 71. Differential Transmitter (TX) Output Specifications

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 71). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 70. Minimum Receiver Eye Timing and Voltage Compliance Specification

2.22.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 71. Compliance Test/Measurement Load

2.23 Clocking

This section describes the PLL configuration of the chip. Note that the platform clock is identical to the core complex bus (CCB) clock.

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{ extsf{ heta}JA}$	14	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	—	R _{θJC}	< 0.1	°C/W	4

Table 79. Package Thermal Characteristics (continued)

Notes

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
- 3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 •C/W

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the chip's thermal model without a lid is shown in Figure 72 The substrate is modeled as a block 29 x 29 x 1.2 mm with an in-plane conductivity of 19.8 W/m•K and a through-plane conductivity of 1.13 W/m•K. The solder balls and air are modeled as a single block 29 x 29 x 0.5 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 9.6 x 9.57 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 7.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

2.24.2 Recommended Thermal Model

This table shows the chip's thermal model.

Conductivity	Value	Units				
Die (9.6x9.6 × 0.85 mm)						
Silicon	Temperature dependent	—				
Bump/Underfill (9.6 x 9.6 \times 0.07 mm) Collapsed Thermal Resistance						
Kz	7.5	W/m•K				
Substrate (29 $ imes$ 29 $ imes$ 1.2 mm)						
Kx	19.8	W/m•K				
Ку	19.8					
Kz	1.13					
Solder and Air (29 \times 29 \times 0.5 mm)						
Kx	0.034	W/m•K				
Ку	0.034					
Kz	12.1					

Table 80. Thermal Model



Figure 72. System-Level Thermal Model for the Chip (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

2.24.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

Hardware Design Considerations

This figure shows the PLL power supply filter circuit.

$$V_{DD} \circ \underbrace{10 \Omega}_{2.2 \mu F} \circ AV_{DD}$$

2.2 $\mu F \underbrace{-}_{GND} 2.2 \mu F$
Low ESL Surface Mount Capacitors

Figure 75. Chip PLL Power Supply Filter Circuit

The AV_{DD}_SRDS*n* signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 76. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003- μ F capacitor is closest to the balls, followed by the 1- μ F capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up

Figure 76. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD} should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

3.3 Pin States in Deep Sleep State

In all low power mode by default, all input and output pads remain driven as per normal functional operation. The inputs remain enabled.

The exception is that in Deep Sleep mode, GCR[DEEPSLEEP_Z] can be used to tristate a subset of output pads, and disable the receivers of input pads as defined in Table 1. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for details.

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, this chip can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the chip. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the chip using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it should be routed with short and large trace to minimize the inductance.

Ordering Information

4.2 Part Marking

Parts are marked as in the example shown in the following figure.



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 80. Part Marking for FC-PBGA

4.3 Part Numbering

These tables list all part numbers that are offered for the chip.

Table 83. MPC8535 Part Numbers Commercial T

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Notes
600/400/400	MPC8535AVTAKG(A)	MPC8535EAVTAKG(A)	—
800/400/400	MPC8535AVTANG(A) MPC8535EAVTANG(A)		—
1000/400/400	MPC8535AVTAQG(A)	MPC8535EAVTAQG(A)	—
1250/500/500	MPC8535AVTATH(A)	MPC8535EAVTATH(A)	—
1250/500/667	MPC8535AVTATLA	MPC8535EAVTATLA	—

Table 84. MPC8535 Part Numbers Industrial Tier

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Extended Temp Without Security	Extended Temp With Security	Notes
600/400/400	MPC8535BVTAKG(A)	MPC8535EBVTAKG(A)	MPC8535CVTAKG(A)	MPC8535ECVTAKG(A)	1
800/400/400	MPC8535BVTANG(A)	MPC8535EBVTANG(A)	MPC8535CVTANG(A)	MPC8535ECVTANG(A)	
1000/400/400	MPC8535BVTAQG(A)	MPC8535EBVTAQG(A)	MPC8535CVTAQG(A)	MPC8535ECVTAQG(A)	
1250/500/500	MPC8535BVTATH(A)	MPC8535EBVTATH(A)	MPC8535CVTATH(A)	MPC8535ECVTATH(A)	
1250/500/667	MPC8535BVTATLA	MPC8535EBVTATLA	MPC8535CVTATLA	MPC8535ECVTATLA	

Note:

1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A