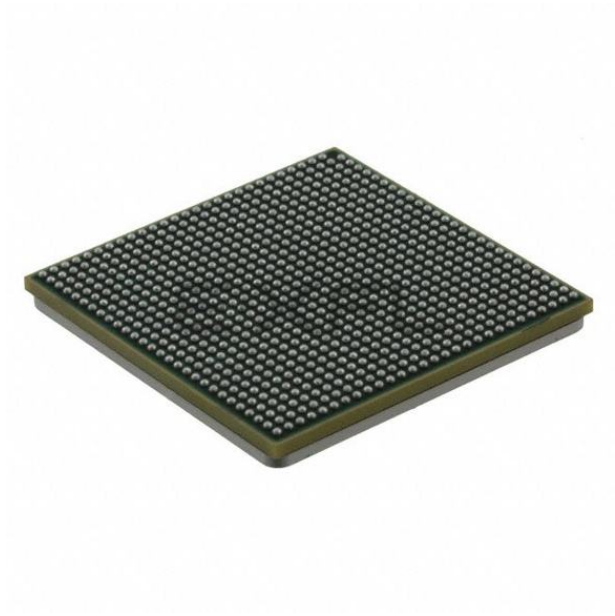

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535bvjatha

This figure shows the major functional units within the chip.

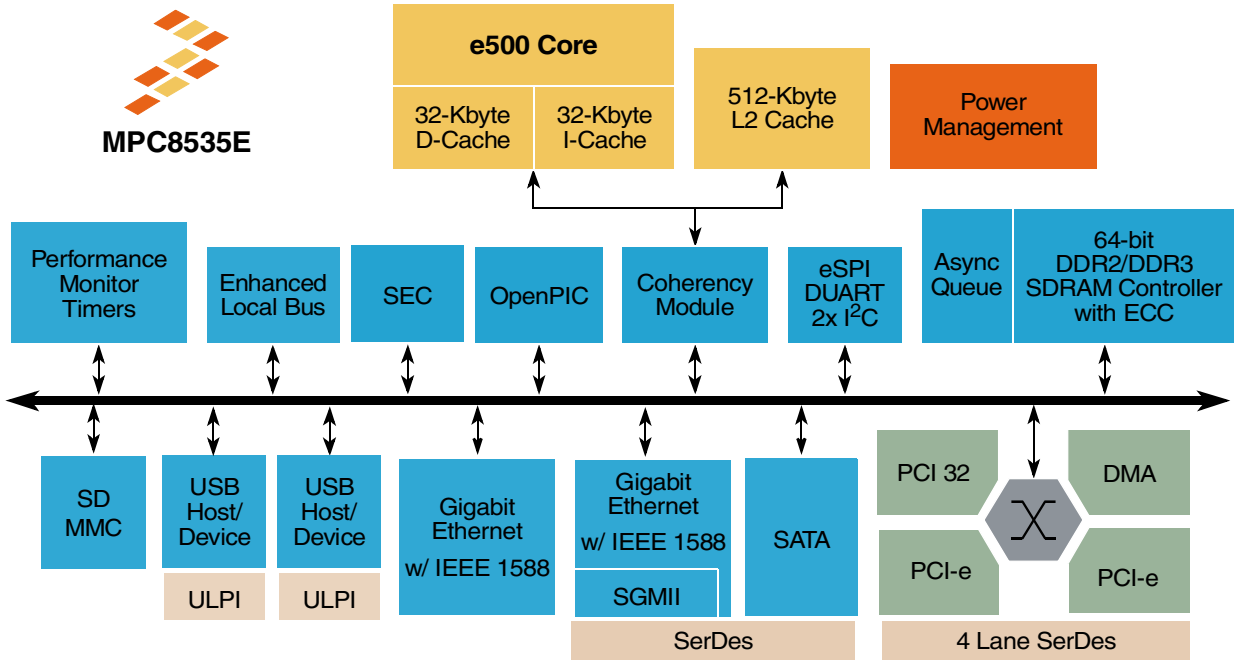


Figure 1. Chip Block Diagram

1 Pin Assignments and Reset States

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

1.1 Pin Map

See Table 1 for the MPC8535E pinout, which is a subset of the MPC8536E.

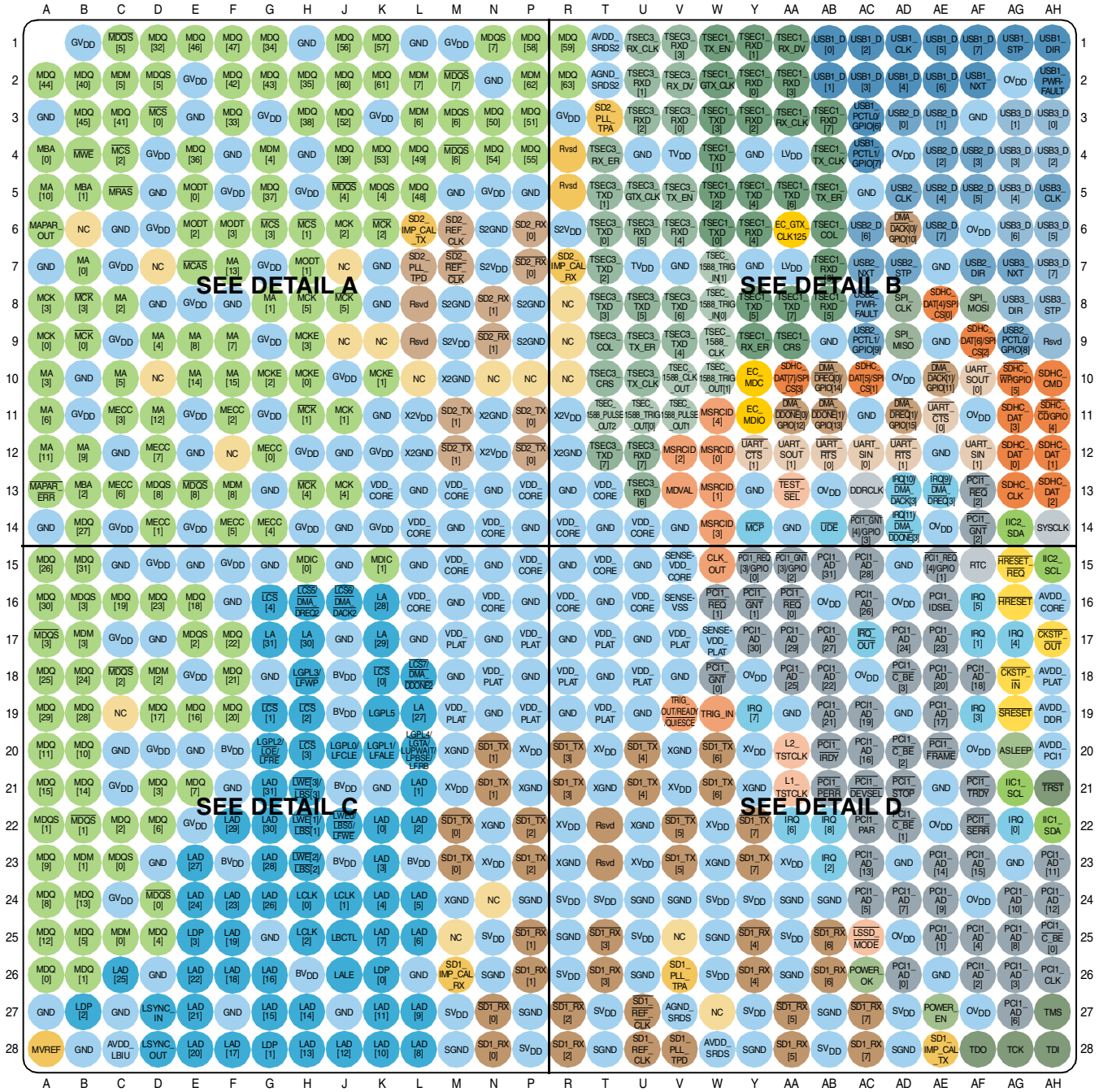


Figure 2. Chip Pin Map Bottom View

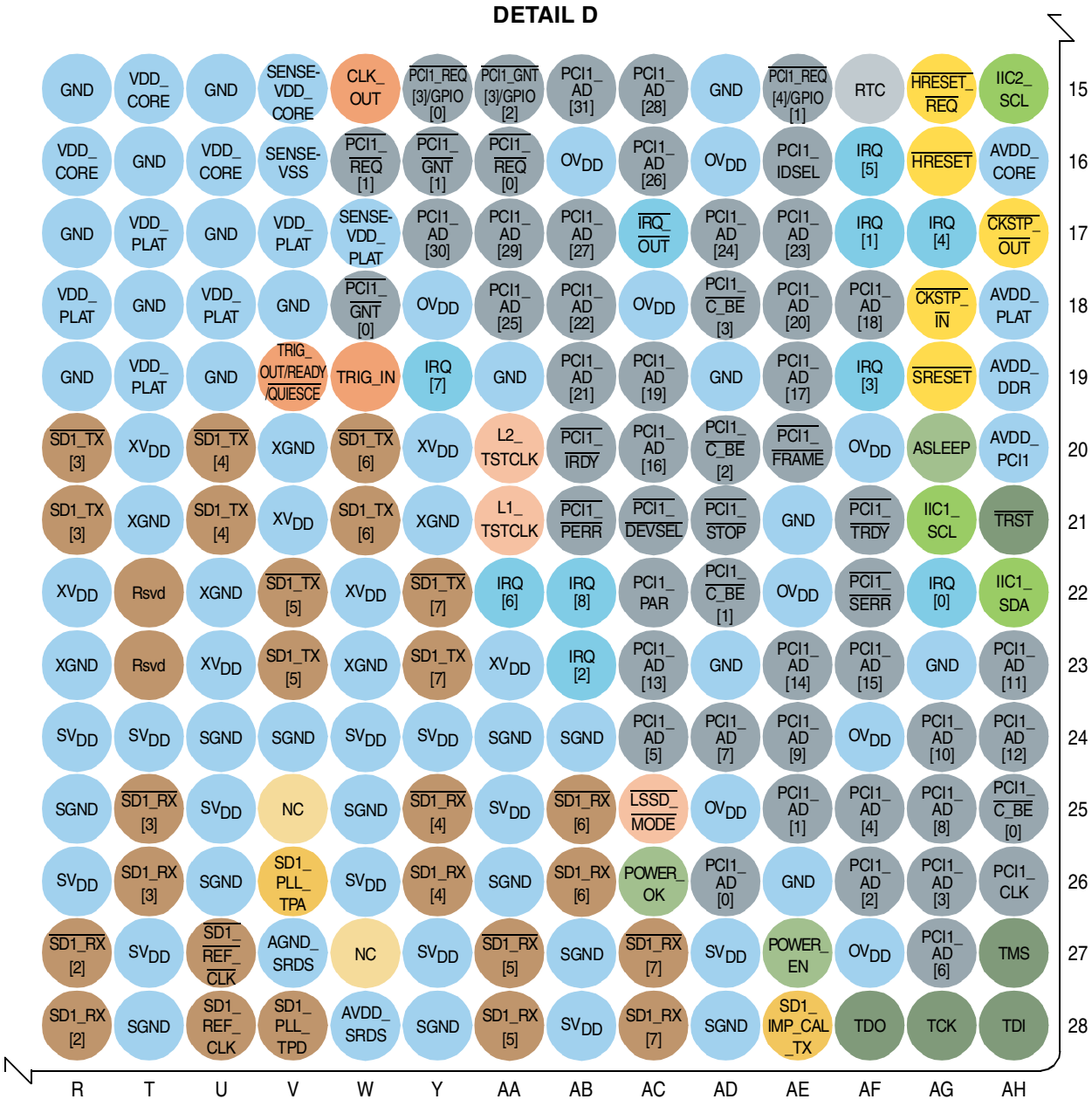


Figure 6. Chip Pin Map Detail D

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST\_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	—	XV_{DD}	—
S2VDD	SerDes 2 core logic supply	R6,N7,M9	—	$S2V_{DD}$	—
X2VDD	SerDes 2 transceiver supply	R11,N12,L11	—	$X2V_{DD}$	—
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13	—	V_{DD_CORE}	—
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	—	V_{DD_PLAT}	—
AVDD_CORE	CPU PLL supply	AH16	—	AV_{DD_CORE}	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV_{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV_{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV_{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV_{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	—	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V_{DD_CORE}	13
SENSEVDD_PLAT	—	W17	—	V_{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13	—	—	—
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals may be listed only once and may not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled-high.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD_CORE}/V_{DD_PLAT}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
17. This pin is only an output in FIFO mode when used as Rx Flow Control.
18. Do not connect.
19. These must be pulled up (100 Ω- 1 kΩ) to OVDD.
20. Independent supplies derived from board VDD.
21. Recommend a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD}.
22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.
23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
24. General-Purpose POR configuration of user system.

2.4.4 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the chip.

Table 8. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD}, TV_{DD} = 2.5V LV_{DD}, TV_{DD} = 3.3V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TVDD=2.5V, and from 0.6 and 2.7V for L/TVDD=3.3V at 0.6 V and 2.7 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.9.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.4.5 DDR Clock Timing

This table provides the DDR clock (DDRCLK) AC timing specifications for the chip.

Table 9. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66	—	166	MHz	1
DDRCLK cycle time	t_{DDRCLK}	6.0	—	15.15	ns	—
DDRCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	—
DDRCLK jitter	—	—	—	+/– 150	ps	3, 4

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. See Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

Table 21. SPI AC Timing Specifications[1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_CS outputs—Master data delay	$t_{NIKHOV2}$	—	6.0	ns	—
SPI inputs—Master data input setup time	t_{NIIVKH}	5	—	ns	—
SPI inputs—Master data input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. SPCOM[RxDelay] is set to 0.
4. SPCOM[RxDelay] is set to 1.

This figure provides the AC test load for the SPI.

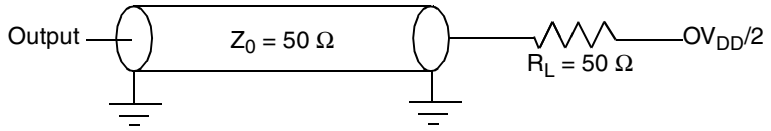
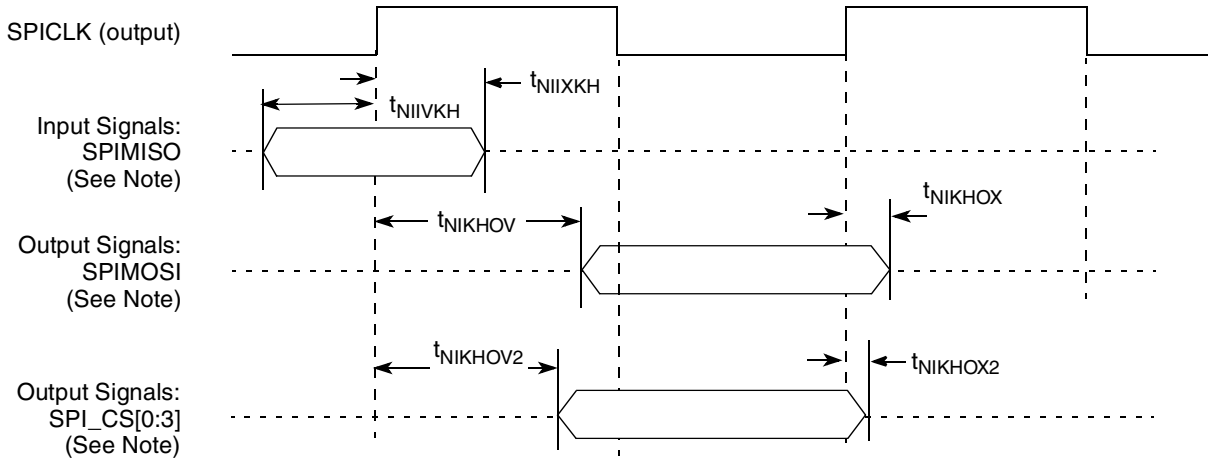


Figure 12. SPI AC Test Load

This figure represents the AC timing from Table 21. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on SPI.

Figure 13. SPI AC Timing in Master mode (Internal Clock) Diagram

2.9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps) — FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 2.10, "Ethernet Management Interface Electrical Characteristics."

The electrical characteristics for SGMII is specified in Section 2.9.3, "SGMII Interface Electrical Characteristics." The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

2.9.1.1 GMII, MII, TBI, RGMII, RMII and RTBI DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in the following tables. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	1.90	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	3

Notes:

1 LV_{DD} supports eTSECs 1.

2 TV_{DD} supports eTSECs 3.

3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 36. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

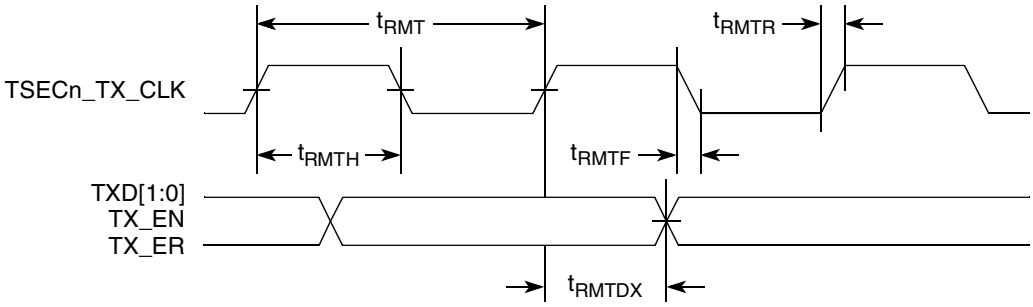


Figure 26. RMII Transmit AC Timing Diagram

2.9.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_RX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_RX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns

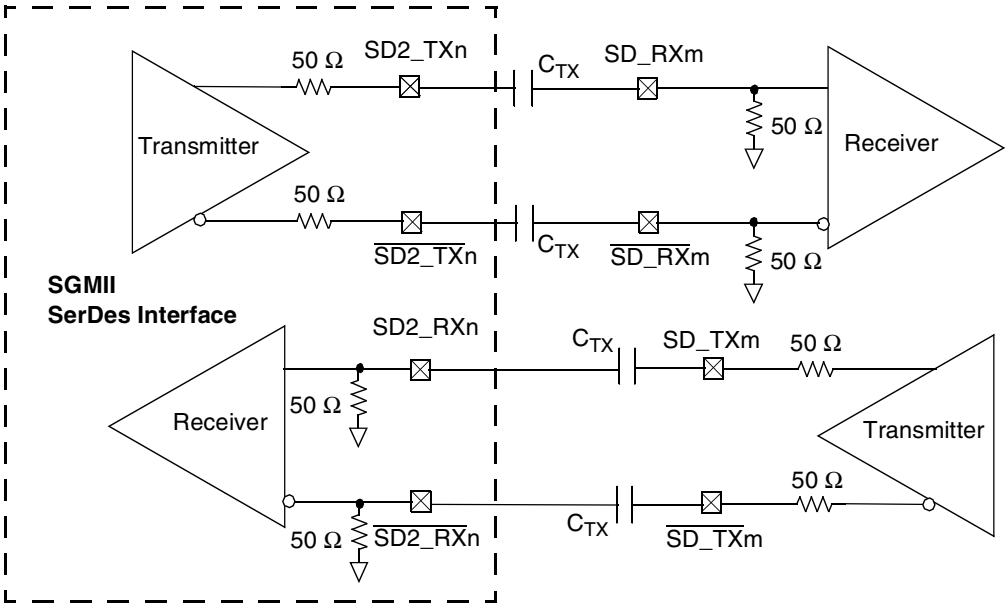


Figure 29. 4-Wire AC-Coupled SGMII Serial Link Connection Example

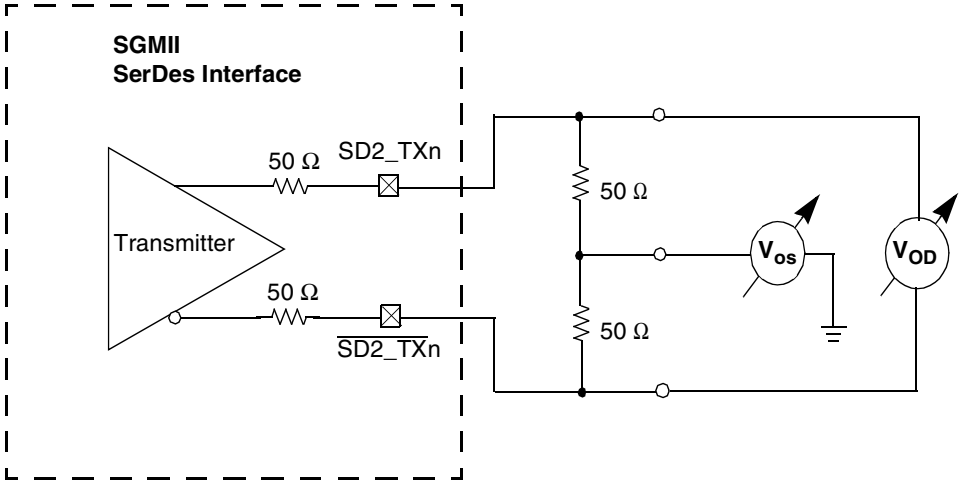


Figure 30. SGMII Transmitter DC Measurement Circuit

Table 40. SGMII DC Receiver Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage		$X2V_{DD}$	0.95	1.0	1.05	V	—
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 0	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	VLOS	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Input AC common mode voltage		$V_{CM\_ACp\text{-}p}$	—	—	100	mV	5

2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

Table 44. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.40	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDC frequency	f_{MDC}	0.74	2.5	8.3	MHz	2
EC_MDC period	t_{MDC}	120	400	1350	ns	—
EC_MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
EC_MDC to EC_MDIO delay	t_{MDKHDX}	(16 * t_{plb_clk})-3	—	(16 * t_{plb_clk})+3	ns	3,5,6
EC_MDIO to EC_MDC setup time	t_{MDDVKH}	5	—	—	ns	—

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDIO to EC_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
EC_MDC rise time	t_{MDCR}	—	—	10	ns	—
EC_MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. t_{CLKplb_clk} is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time t_{MDKHDX}. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

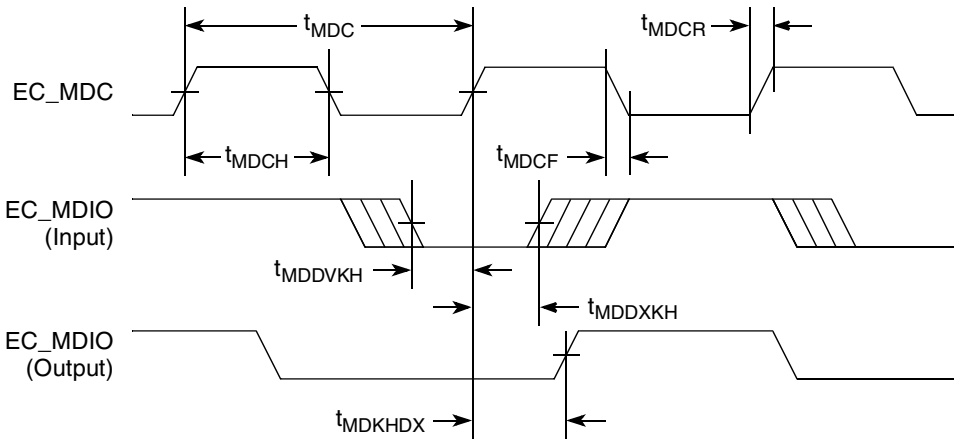


Figure 35. MII Management Interface Timing Diagram

2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

2.16.2 Differential Transmitter (TX) Output Characteristics

This table provides the differential transmitter (TX) output characteristics for the SATA interface.

Table 60. Differential Transmitter (TX) Output Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Channel Speed 1.5G 3.0G	t_{CH_SPEED}	—	 1.5 3.0	—	Gbps	—
Unit Interval 1.5G 3.0G	T_{UI}	666.4333 333.2167	666.4333 333.3333	670.2333 335.1167	ps	—
DC Coupled Common Mode Voltage	V_{dc_cm}	200	250	450	mV	3
TX Diff Output Voltage 1.5G 3.0G	V_{SATA_TXDIFF}	400 400	500 —	600 700	mV	—
TX rise/fall time 1.5G 3.0G	$t_{SATA\_20\text{-}80TX}$	100 67	— —	273 136	ps	—
TX differential skew	t_{SATA_TXSKEW}	—	—	20	ps	—
TX Differential pair impedance 1.5G	$Z_{SATA\_TXDIFFIM}$	 85	 —	 115	ohm	—
TX Single ended impedance 1.5G	Z_{SATA_TXSEIM}	 40	 —	 —	ohm	—
TX AC common mode voltage (peak to peak) 1.5G 3.0G	$V_{SATA\_TXCMMOD}$	 — —	 — —	 — 50	mV	—
OOB Differential Delta	$V_{SATA\_OOBvdoff}$	—	—	25	mV	1
OOB Common mode Delta	V_{SATA_OOBcm}	—	—	50	mV	1
TX Rise/Fall Imbalance	$T_{SATA\_TXR/Fbal}$	—	—	20	%	—
TX Amplitude Imbalance	$T_{SATA\_TXampbal}$	—	—	10	%	—
TX Differential Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXDD11}	 — — — — — —	 — — — — — —	 14 8 6 6 3 1	 dB	 1, 2

Table 60. Differential Transmitter (TX) Output Characteristics (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
TX Common Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXCC11}	 — — — — — —	 — — — — — —	 5 5 2 2 1 1	 dB	 1, 2
TX Impedance Balance 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXDC11}	 — — — — — —	 — — — — — —	 30 20 10 10 4 4	 dB	 1, 2
Deterministic jitter 1.5G 3.0G	U_{SATA_TXDJ}	—	—	 0.18 0.14	 UI	—
Total Jitter 1.5G 3.0G	U_{SATA_TXTJ}	—	—	 0.42 0.32	 UI	—

Notes:
1. Only applies when operating in 3.0Gb data rate mode.
2. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
3. Only applies to Gen1i mode.

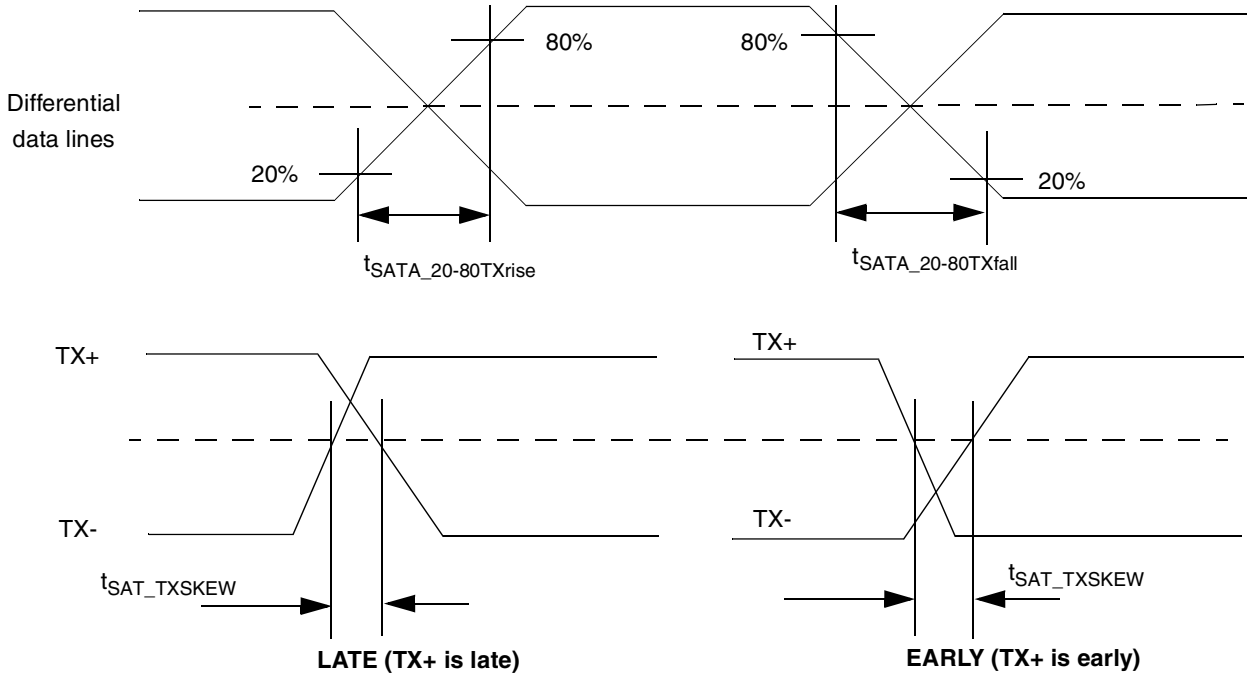


Figure 50. Signal Rise and Fall Times and Differential Skew

2.16.3 Differential Receiver (RX) Input Characteristics

This table provides the differential receiver (RX) input characteristics for the SATA interface.

Table 61. Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
RX Differential Input Voltage 1.5G 3.0G	V_{SATA_RXDIFF}	 240 240	 400 —	 600 750	mVp-p	1
RX rise/fall time 1.5G 3.0G	$t_{SATA\_20\text{-}80RX}$	100 67	— —	273 136	ps	—
RX Differential skew 1.5G 3.0G	t_{SATA_RXSKEW}	— —	— —	— 50	ps	—
RX Differential pair impedance 1.5G	$Z_{SATA\_RXDIFFIM}$	85	—	115	ohm	—
RX Single-Ended impedance 1.5G	Z_{SATA_RXSEIM}	40	—	—	ohm	—
DC Coupled Common Mode Voltage	V_{dc_cm}	200	250	450	mV	5

Table 68. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Failing time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 22, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.

This figure provides the AC test load for PCI.

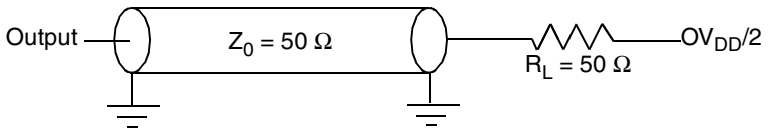


Figure 54. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

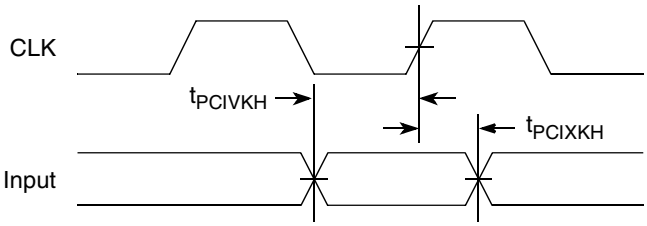


Figure 55. PCI Input AC Timing Measurement Conditions

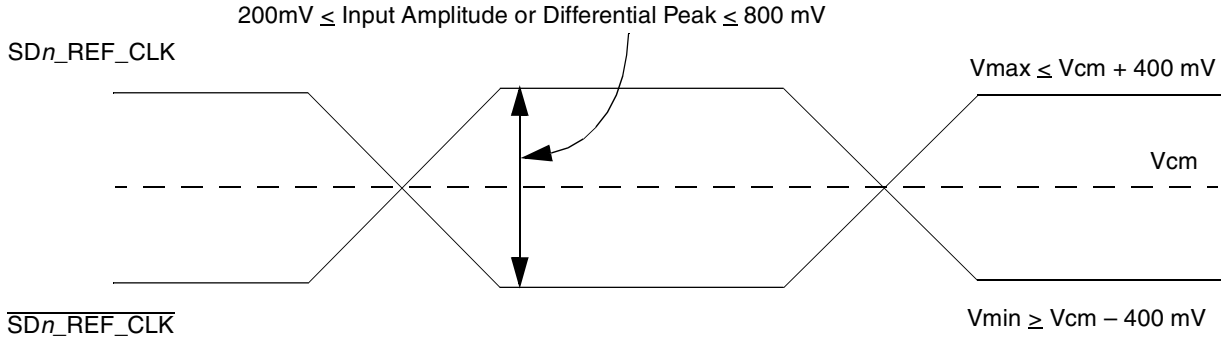


Figure 60. Differential Reference Clock Input DC Requirements (External AC-Coupled)

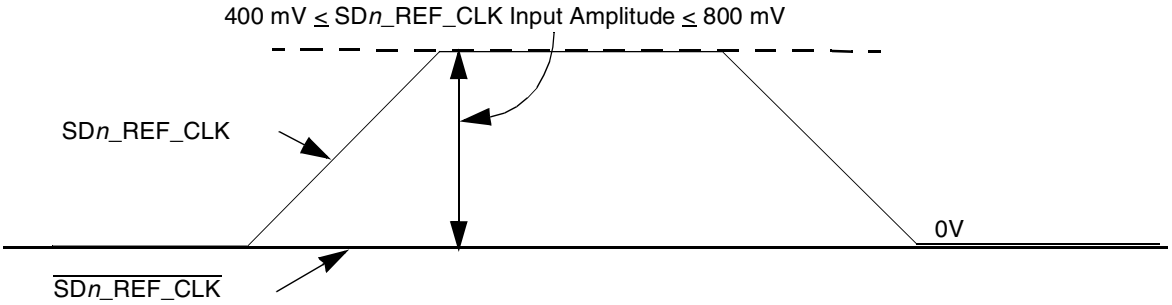


Figure 61. Single-Ended Reference Clock Input DC Requirements

2.20.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SnGND (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL (Low Voltage Positive Emitter-Coupled Logic) outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 62 to Figure 65 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the chip's SerDes reference clock receiver requirement provided in this document.

The following pins must be connected to XGND if not used:

- SD1_RX[7:4]
- $\overline{\text{SD1\_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

3.11.3 SerDes 2 Interface Entirely Unused

If the high-speed SerDes 2 interface (SGMII/ SATA) is not used at all, the unused pin should be terminated as described in this section. There are several Reserved pins that need to be either left floating or connected to X2GND. See SerDes2 in Table 1Table 1 for details.

The following pins must be left unconnected (float):

- SD2_TX[0]
- $\overline{\text{SD2\_TX[0]}}$
- Reserved pins L8, L9

The following pins must be connected to X2GND:

- SD2_RX[0]
- $\overline{\text{SD2\_RX[0]}}$
- SD2_REF_CLK
- $\overline{\text{SD2\_REF\_CLK}}$

The POR configuration pin cfg_srds2_prtcl[0:2] on TSEC1_TXD[2], TSEC3_TXD[2], TSEC_1588_PUSLE_OUT1 can be used to power down SerDes 2 block for power saving. Note that both S2VDD and X2VDD must remain powered.

4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, “Part Numbers Fully Addressed by this Document.”

5. Capacitors may not be present on all devices
6. Caution must be taken not to short exposed metal capacitor pads on package top.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

6 Product Documentation

The following documents are required for a complete description of the chip and are needed to design properly with the part.

- *MPC8536E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8536ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)

7 Document Revision History

This table provides a revision history for this hardware specification.

Table 85. Document Revision History

Revision	Date	Substantive Change(s)
5	09/2011	• Removed PVDD from Table 1, “Pinout Listing.”
4	06/2011	• In Table 1, “Pinout Listing,” updated the power supply for TSEC3 pins to TVDD. • Updated Table 56, “eSDHC AC Timing Specifications.” • In Section 4.3, “Part Numbering,” added an extra bin (1250/500/667) to support DDR3.
3	11/2010	• In Table 1, “Pinout Listing,” added the following note: “For systems that boot from Local Bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required...” In addition, updated footnote 26 and added footnote 29 to PCI1_AD. • Updated Table 21 • Updated Figure 25, “RGMII and RTBI AC Timing and Multiplexing Diagrams.” • In Table 44, “MII Management DC Electrical Characteristics,” changed the Voh/Vol values for MDIO/MDC. • Added Note 6 regarding USB*n*_DIR pin to Table 47, “USB General Timing Parameters6.” • In Table 64, “I2C AC Electrical Specifications,” updated footnote 2. • In Table 82, , Table 83, , Table 84, added the Revision Level A for Rev 1.2
2	09/2009	**Note:** • In Section 1, “Pin Assignments and Reset States,”updated the first sentence of the note to say, “The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration.” • In Table 40, “SGMII DC Receiver Electrical Characteristics,” changed LSTSAB to LSTSA and LSTSEF to LSTSE for Note 4. • Updated Die value and Bump/Underfill value in Table 84 **Note:** Updated Figure 81, “Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA,” and its notes.
1	09/2009	• In Table 3, “Recommended Operating Conditions,” for V_{DD_CORE}, removed 1.1 ± 55 mV. • In Table 5, “Power Dissipation 5,” remove note 5. • In Table 5, ”Power Dissipation 5,” changed an “—” to “0.”
0	08/2009	• Initial public release.