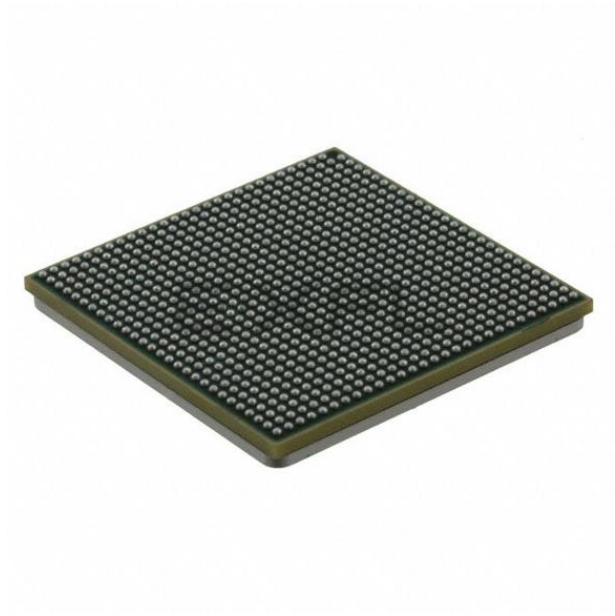

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535bvjatla

1.1 Pin Map

See Table 1 for the MPC8535E pinout, which is a subset of the MPC8536E.

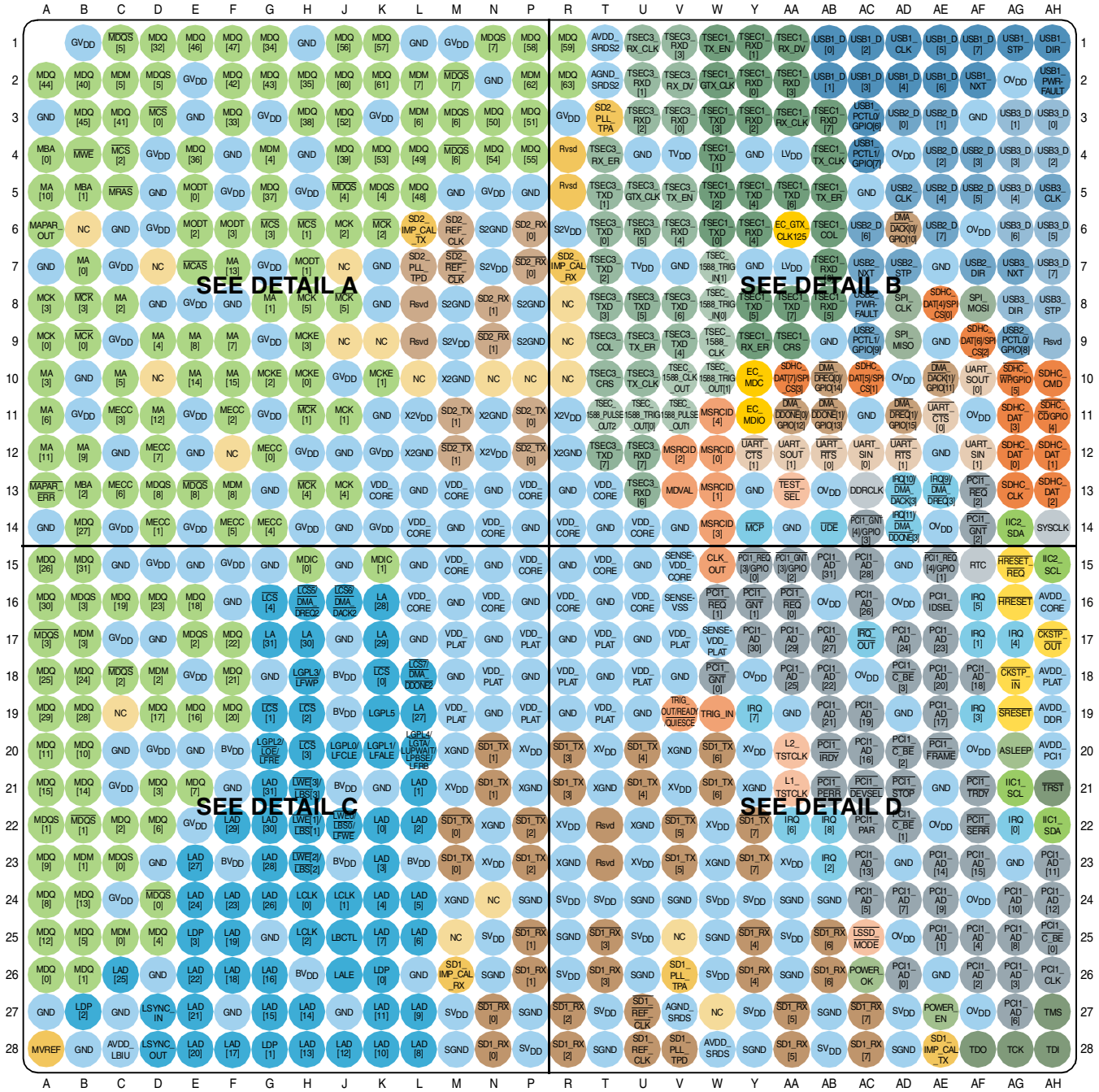

Figure 2. Chip Pin Map Bottom View

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
General-Purpose Input/Output					
GPIO[0:1]/PCI1_REQ[3:4]	GPIO/PCI request	Y15,AE15	I/O	OV_{DD}	—
GPIO[2:3]/PCI1_GNT[3:4]	GPIO/PCI grant	AA15,AC14	I/O	OV_{DD}	—
GPIO[4]/SDHC_CD	GPIO/SDHC card detection	AH11	I/O	OV_{DD}	—
GPIO[5]/SDHC_WP	GPIO/SDHC write protection	AG10	I/O	OV_{DD}	32
GPIO[6]/USB1_PCTL0	GPIO/USB1 PCTL0	AC3	I/O	OV_{DD}	—
GPIO[7]/USB1_PCTL1	GPIO/USB1 PCTL1	AC4	I/O	OV_{DD}	—
GPIO[8]/USB2_PCTL0	GPIO/USB2 PCTL0	AG9	I/O	OV_{DD}	—
GPIO[9]/USB2_PCTL1	GPIO/USB2 PCTL1	AC9	I/O	OV_{DD}	—
GPIO[10:11] /DMA_DACK[0:1]	GPIO/DMA Ack	AD6,AE10	I/O	OV_{DD}	—
GPIO[12:13] /DMA_DDONE[0:1]	GPIO/DMA done	AA11,AB11	I/O	OV_{DD}	—
GPIO[14:15] /DMA_DREQ[0:1]	GPIO/DMA request	AB10,AD11	I/O	OV_{DD}	—
System Control					
HRESET	Hard reset	AG16	I	OV_{DD}	—
HRESET_REQ	Hard reset - request	AG15	O	OV_{DD}	22
SRESET	Soft reset	AG19	I	OV_{DD}	—
CKSTP_IN	CheckStop in	AG18	I	OV_{DD}	—
CKSTP_OUT	CheckStop Output	AH17	O	OV_{DD}	2,4
Debug					
TRIG_IN	Trigger in	W19	I	OV_{DD}	—
TRIG_OUT/READY /QUIESCE	Trigger out/Ready/Quiesce	V19	O	OV_{DD}	22
MSRCID[0:1]	Memory debug source port ID	W12,W13	O	OV_{DD}	6,9
MSRCID[2:4]	Memory debug source port ID	V12, W14,W11	O	OV_{DD}	6,9,22
MDVAL	Memory debug data valid	V13	O	OV_{DD}	6,22
CLK_OUT	Clock Out	W15	O	OV_{DD}	11
Clock					
RTC	Real time clock	AF15	I	OV_{DD}	—
SYSCLK	System clock / PCI clock	AH14	I	OV_{DD}	—
DDRCLK	DDR clock	AC13	I	OV_{DD}	30
JTAG					

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	3
DDR3 signal	20 40 (half strength mode)	GV_{DD} = 1.5 V	2
TSEC signals	42	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I^2C	150	OV_{DD} = 3.3 V	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI1\_GNT1}}$ signal at reset.
3. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min)

2.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper chip operation. These requirements are as follows for power up:

1. V_{DD_PLAT}, V_{DD_CORE} (if POWER_EN is not used to control V_{DD_CORE}), AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD},$S2V_{DD}$, TV_{DD}, XV_{DD} and $X2V_{DD}$
2. [Wait for POWER_EN to assert], then V_{DD_CORE} (if POWER_EN is used to control V_{DD_CORE})
3. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD platform supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the chip.

During the Deep Sleep state, the VDD core supply is removed. But all other power supplies remain applied. Therefore, there is no requirement to apply the VDD core supply before any other power rails when the silicon waking from Deep Sleep.

2.4.6 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. The “platform clock (CCB) frequency” in the following formula refers to the maximum platform (CCB) frequency of the speed bins the part belongs to, which is defined in Table 73.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

2.4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

2.5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the chip. This table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	Sysclk	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configurations (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configurations (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1
$\overline{\text{HRESET}}$ rise time	—	1	SYSCLK	—

Notes:

1. SYSCLK is the primary clock input for the chip.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
Local bus PLL	—	50	µs	—
PCI bus lock time	—	50	µs	—

Table 17. DDR3 SDRAM Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606MHz and 667MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
667 MHz	—	–240	240	—	3
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} =+/-(T/4 - abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR2 and DDR3 frequency is 667MHz.

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

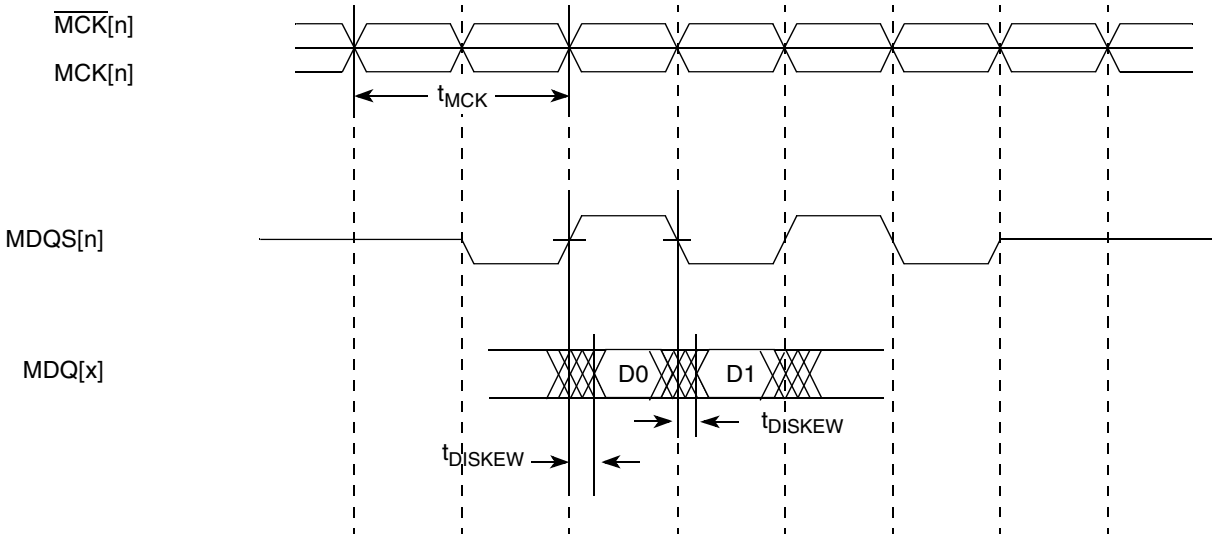

Figure 8. DDR SDRAM Input Timing Diagram

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

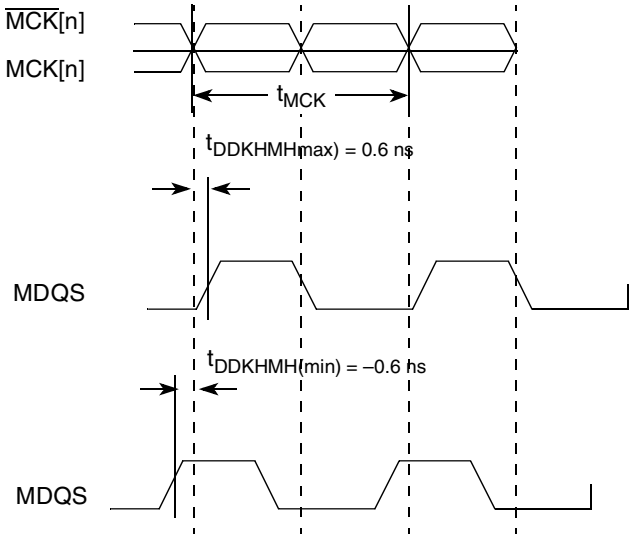

Figure 9. Timing Diagram for tDDKHMH

This figure shows the DDR SDRAM output timing diagram.

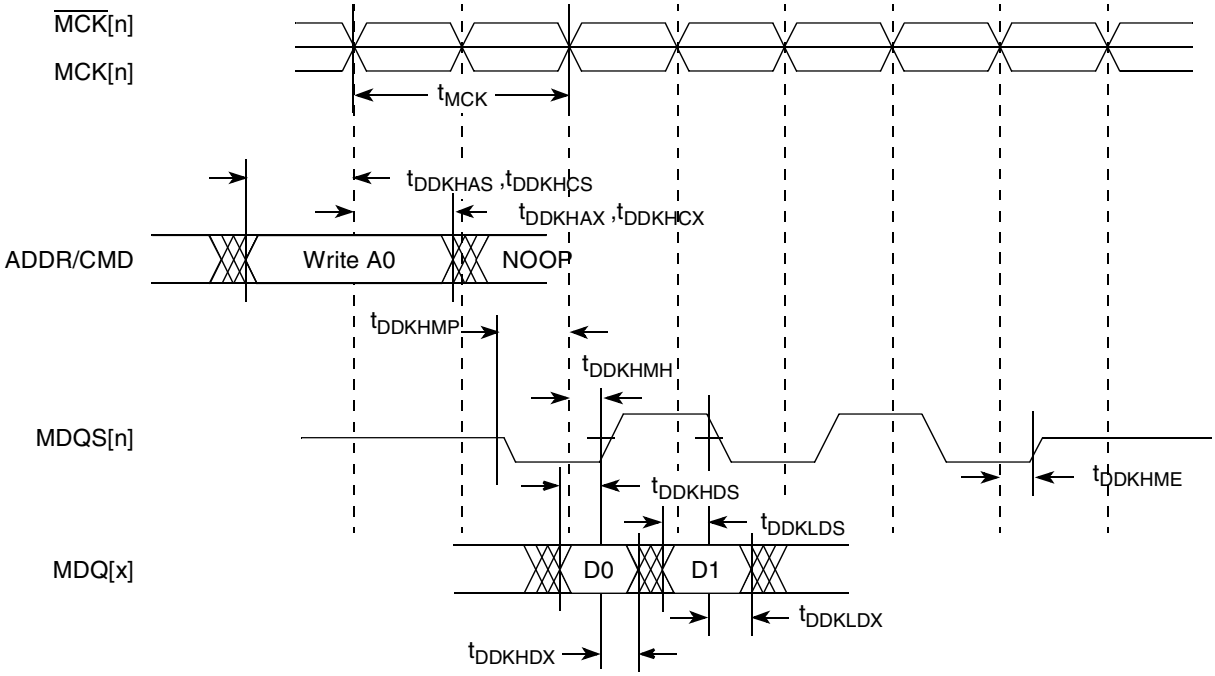

Figure 10. DDR SDRAM Output Timing Diagram

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ pins.

2.9.3.1 DC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.20, "High-Speed Serial Interfaces."

2.9.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 38. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10 (8)	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	2,3

Notes:

1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected via cfg_srds_sgmii_refclk during POR.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 50 ps.

2.12 enhanced Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

2.12.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 48. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	1.9	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 49. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 50. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	—	1.71	1.89	V
High-level input voltage	V_{IH}	—	0.65*BV_{DD}	0.3+BV_{DD}	V
Low-level input voltage	V_{IL}	—	–0.3	0.35*BV_{DD}	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	-15	10	μA
High-level output voltage	V_{OH}	I_{OH} = –100 μA	BV_{DD} – 0.2	—	V
		I_{OH} = –2 mA	BV_{DD} – 0.45	—	
Low-level output voltage	V_{OL}	I_{OH} = 100 μA	—	0.2	V
		I_{OH} = 2 mA	—	0.45	

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

2.12.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V DC. For information about the frequency range of local bus see Section 2.23.1, “Clock Ranges.”

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.4	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC) (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	—	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	—	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	—	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 53. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.9	—	ns	3

This figures show the local bus signals.

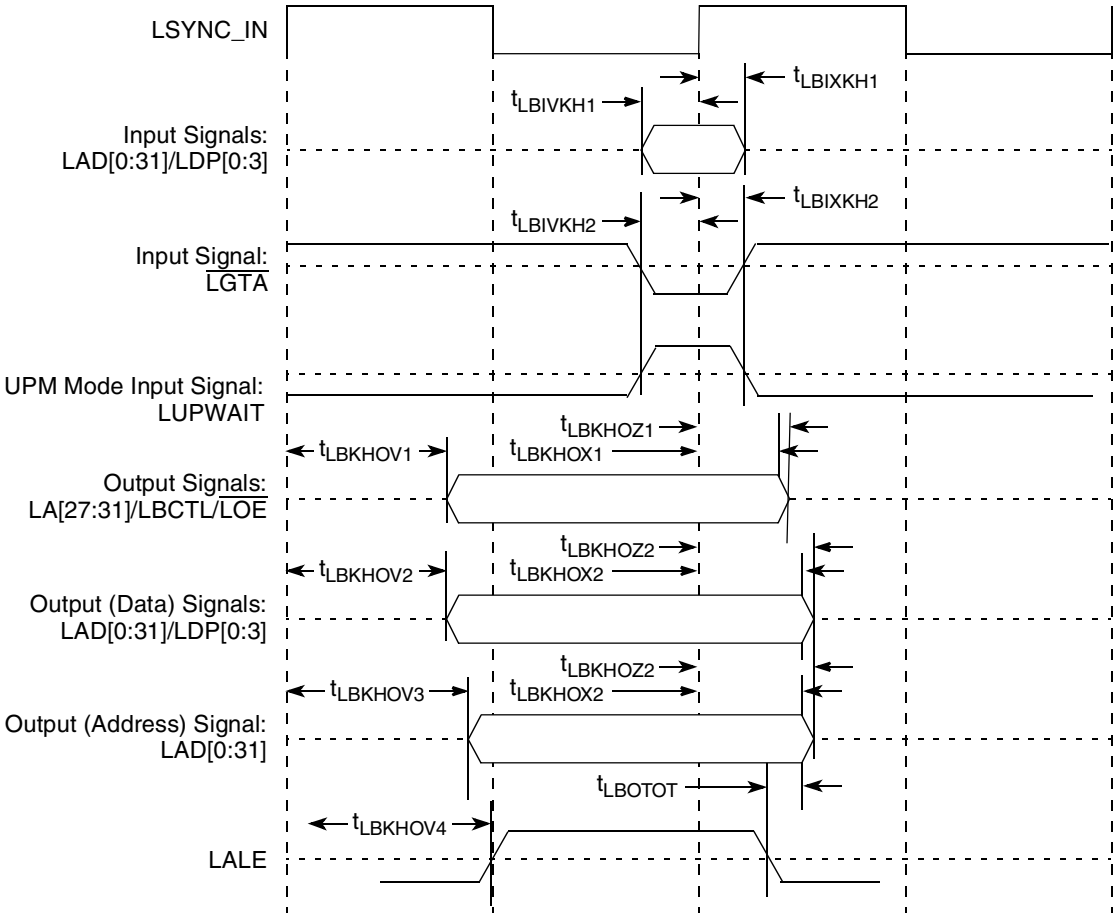

Figure 39. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

NOTE

In PLL bypass mode, some signals are launched and captured on the opposite edge of LCLK[n] to that used in PLL Enable Mode. In this mode, output signals are launched at the falling edge of the LCLK[n] and inputs signals are captured at the rising edge of LCLK[n] with the exception of LGTA/LUPWAIT (which is captured at the falling edge of the LCLK[n]).

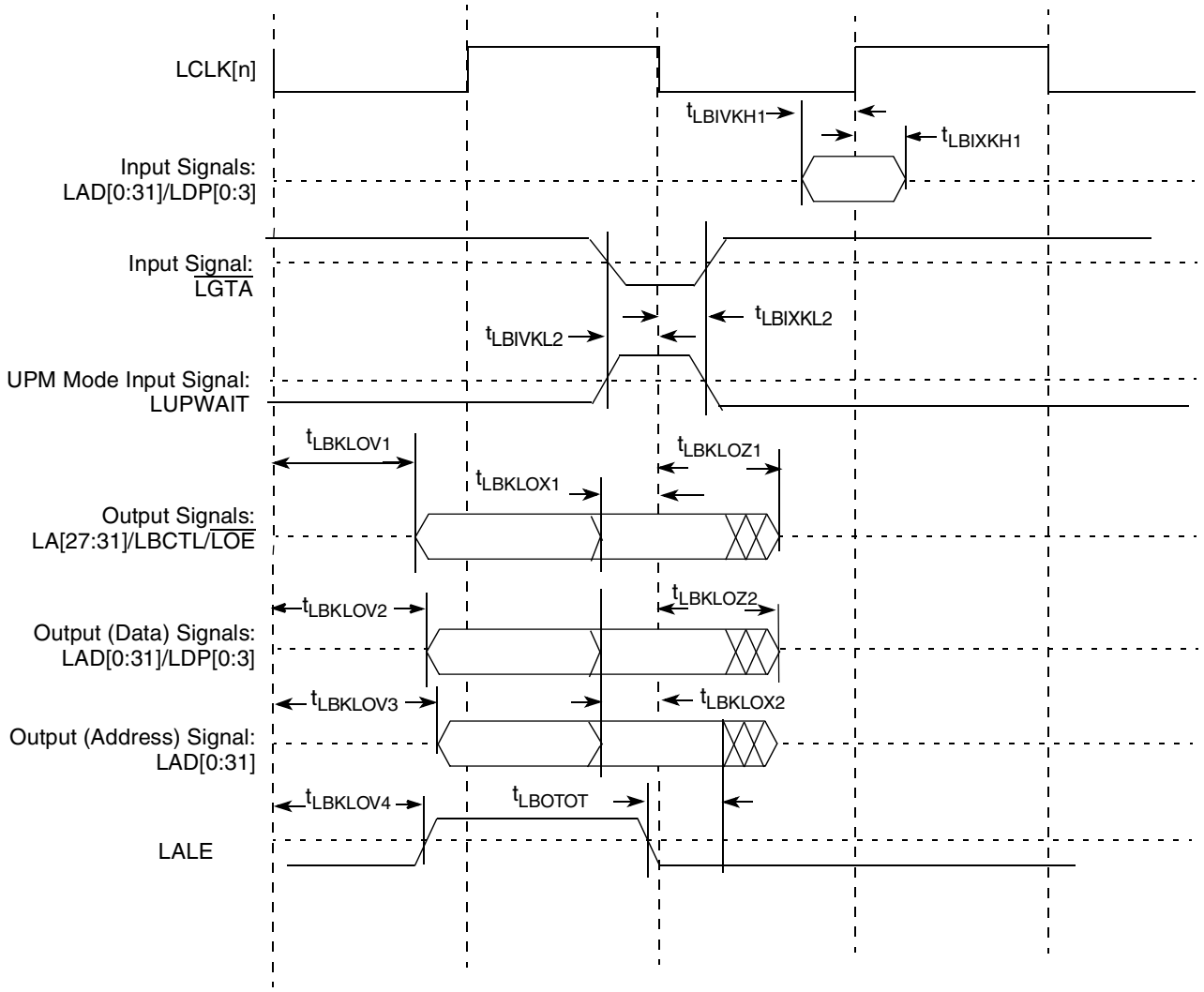

Figure 40. Local Bus Signals (PLL Bypass Mode)

This table describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 54. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	5.1	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	4.2	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	-1.4	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-2.0	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.4	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	0.5	ns	4

Table 54. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	0.5	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	0.5	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.5	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	—	2.2	ns	4,8
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	—	2.2	ns	4,8
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.1	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.1	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. These timing parameters for PLL bypass mode are defined in the opposite direction of the PLL enabled output hold timing parameters.

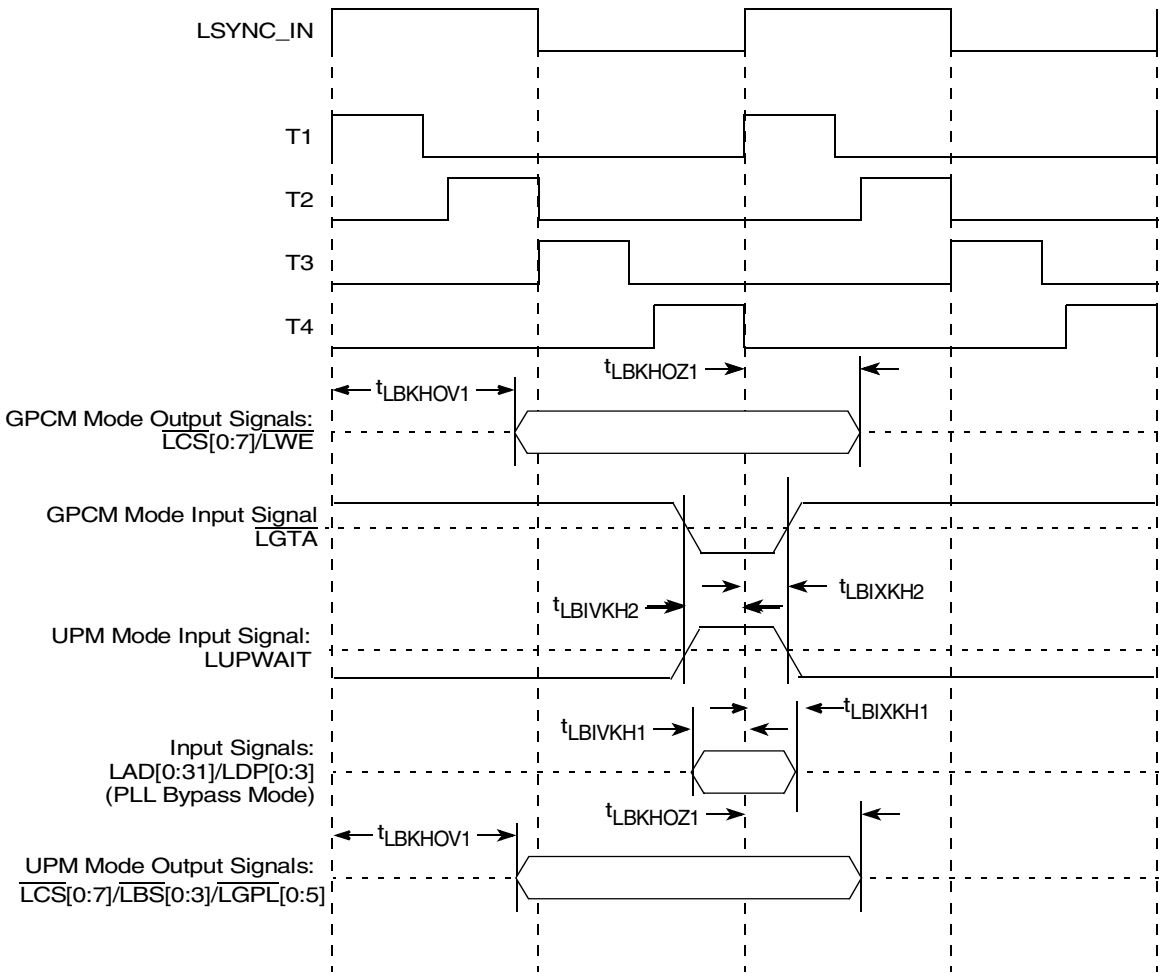

Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 * OVDD	OVDD+0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.25 * OVDD	V	—
Input/Output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—
Output high voltage	V_{OH}	I_{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	—

Table 57. JTAG DC Electrical Characteristics (continued)

Parameter	Symbol [1]	Min	Max	Unit
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

This table provides the JTAG AC timing specifications as defined in the following figures.

Table 58. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions (see Table 3).

Parameter	Symbol [1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times:	t_{JTDVKH}	4	—	ns	
Input hold times:	t_{JTDXKH}	10	—	ns	
Output Valid times:	t_{JTKLDV}	—	10	ns	3
Output hold times:	t_{JTKLDX}	0	—	ns	3

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3.) The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.

6. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = V_{SDn\_TX} + V_{\overline{SDn\_TX}} = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

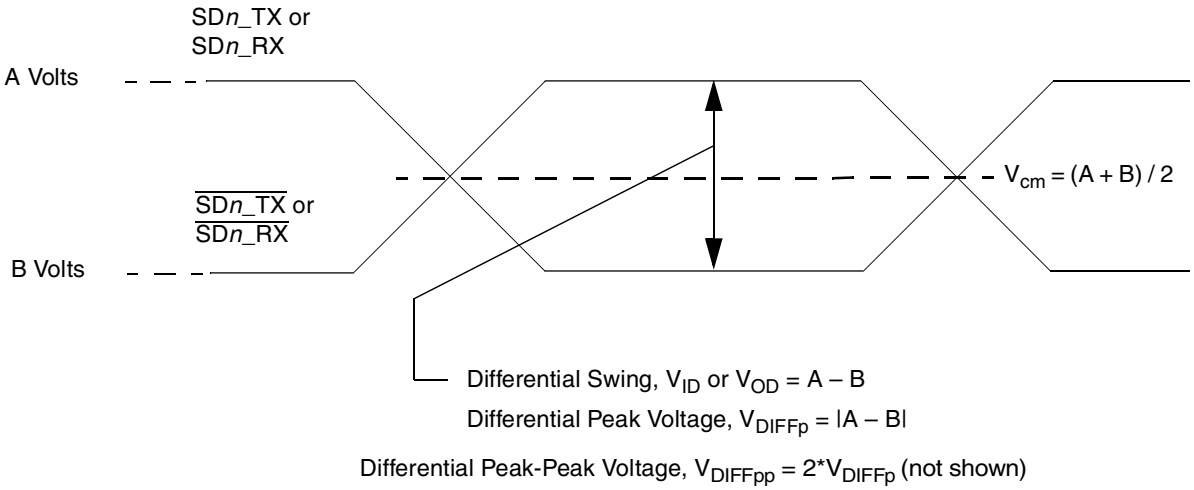

Figure 57. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks for PCI Express are SD1_REF_CLK and, $\overline{SD1\_REF\_CLK}$. The SerDes reference clocks for the SATA and SGMII interfaces are SD2_REF_CLK and, $\overline{SD2\_REF\_CLK}$.

The following sections describe the SerDes reference clock requirements and some application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

Figure 58 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $X2V_{DD}$ are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SDn_REF_CLK and $\overline{SDn\_REF\_CLK}$ are internally AC-coupled differential inputs as shown in Figure 58. Each differential clock input (SD*n*_REF_CLK or $\overline{SDn\_REF\_CLK}$) has a 50-Ω termination to SGND (xcorevss) followed by on-chip AC-coupling.

2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

2.21.1 DC Requirements for PCI Express SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$

For more information, see Section 2.20.2, "SerDes Reference Clocks."

2.21.2 AC Requirements for PCI Express SerDes Clocks

This table lists AC requirements.

Table 70. SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	1,2,3

Notes:
1. Tj at BER of 10E-6 86 ps Max.
2. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 42 ps.
3. Limits from "PCI Express CEM Rev 2.0" and measured per "PCI Express Rj, D, and Bit Error Rates".

2.21.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

2.21.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this chip. For further details as well as the specifications of the transport and data link layer, please use the PCI Express Base Specification. REV. 1.0a document.

2.21.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 71. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.

Table 79. Package Thermal Characteristics (continued)

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	< 0.1	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 •C/W

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.For system thermal modeling, the chip's thermal model without a lid is shown in Figure 72 The substrate is modeled as a block 29 x 29 x 1.2 mm with an in-plane conductivity of 19.8 W/m•K and a through-plane conductivity of 1.13 W/m•K. The solder balls and air are modeled as a single block 29 x 29 x 0.5 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 9.6 x 9.57 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 7.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

2.24.2 Recommended Thermal Model

This table shows the chip's thermal model.

Table 80. Thermal Model

Conductivity	Value	Units
Die (9.6x9.6 × 0.85 mm)		
Silicon	Temperature dependent	—
Bump/Underfill (9.6 x 9.6 × 0.07 mm) Collapsed Thermal Resistance		
Kz	7.5	W/m•K
Substrate (29 × 29 × 1.2 mm)		
Kx	19.8	W/m•K
Ky	19.8	
Kz	1.13	
Solder and Air (29 × 29 × 0.5 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 77). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

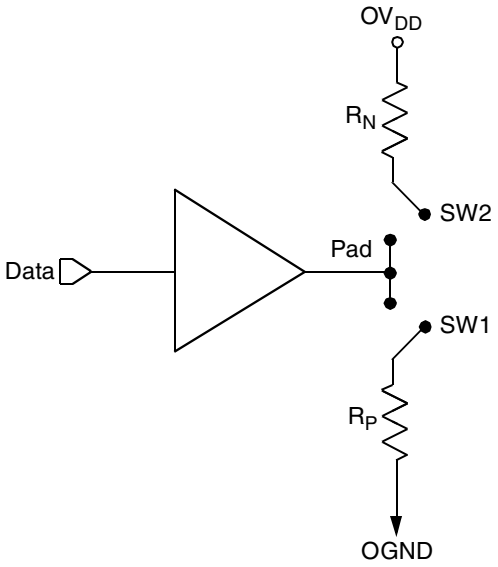

Figure 77. Driver Impedance Measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 81. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	45 Target	45 Target (cfg_pci_impd=1) 25 Target (cfg_pci_impd=0)	18 Target (full strength mode) 36 Target (full strength mode)	Z_0	Ω
R_P	45 Target	45 Target (cfg_pci_impd=1) 25 Target (cfg_pci_impd=0)	18 Target (full strength mode) 36 Target (full strength mode)	Z_0	Ω

Note: Nominal supply voltages. See Table 1.

3.9 Configuration Pin Muxing

The chip provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the chip into the default state and external resistors are needed only when non-default settings are required by the user.

The following pins must be connected to XGND if not used:

- SD1_RX[7:4]
- $\overline{\text{SD1\_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

3.11.3 SerDes 2 Interface Entirely Unused

If the high-speed SerDes 2 interface (SGMII/ SATA) is not used at all, the unused pin should be terminated as described in this section. There are several Reserved pins that need to be either left floating or connected to X2GND. See SerDes2 in Table 1Table 1 for details.

The following pins must be left unconnected (float):

- SD2_TX[0]
- $\overline{\text{SD2\_TX[0]}}$
- Reserved pins L8, L9

The following pins must be connected to X2GND:

- SD2_RX[0]
- $\overline{\text{SD2\_RX[0]}}$
- SD2_REF_CLK
- $\overline{\text{SD2\_REF\_CLK}}$

The POR configuration pin cfg_srds2_prtcl[0:2] on TSEC1_TXD[2], TSEC3_TXD[2], TSEC_1588_PUSLE_OUT1 can be used to power down SerDes 2 block for power saving. Note that both S2VDD and X2VDD must remain powered.

4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, “Part Numbers Fully Addressed by this Document.”