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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8535bvtatla

This figure shows the major functional units within the chip.

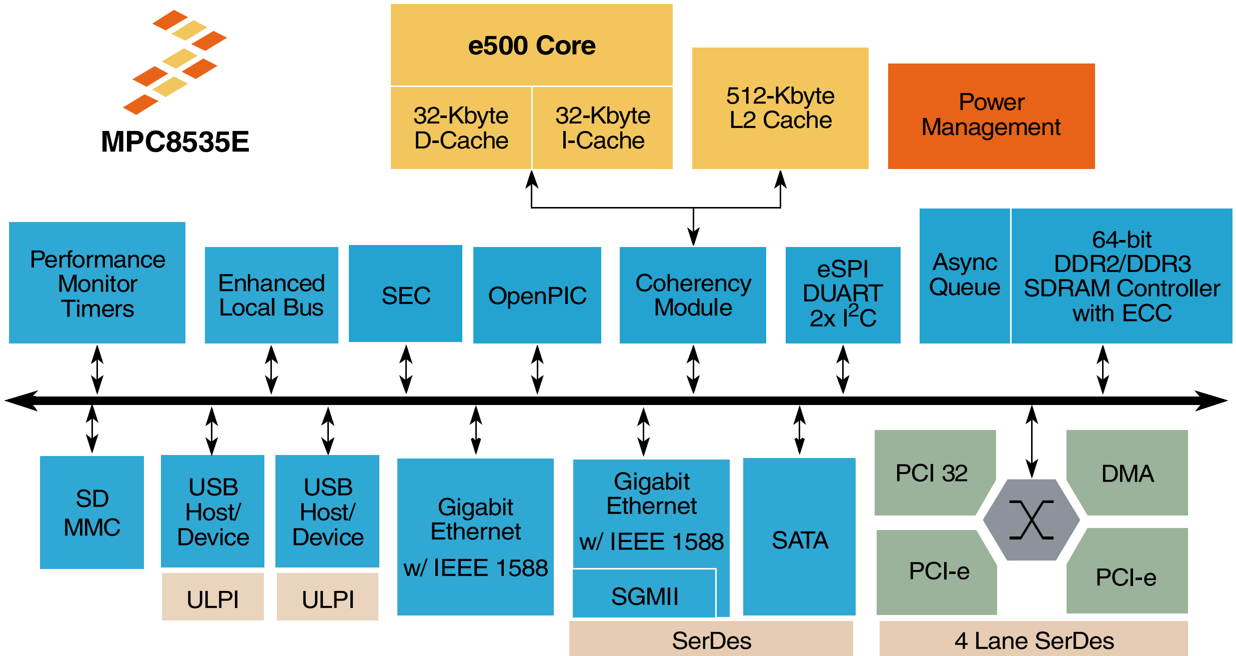

Figure 1. Chip Block Diagram

1 Pin Assignments and Reset States

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
UART_SOUT[0:1]	Transmit data	AF10,AA12	O	OV$_{DD}$	5,9,22, 10,29
I^{2}C interface					
IIC1_SCL	Serial clock	AG21	I/O	OV$_{DD}$	4,21,29
IIC1_SDA	Serial data	AH22	I/O	OV$_{DD}$	4,21,29
IIC2_SCL	Serial clock	AH15	I/O	OV$_{DD}$	4,21,29
IIC2_SDA	Serial data	AG14	I/O	OV$_{DD}$	4,21,29
SerDes1(x4)					
SD1_TX[7:4]	Transmit Data (+)	Y23,W21,V23,U21	O	XV$_{DD}$	—
$\overline{\text{SD1\_TX}}$[7:4]	Transmit Data(-)	Y22,W20,V22,U20	O	XV$_{DD}$	—
SD1_RX[7:4]	Receive Data(+)	AC28,AB26,AA28,Y26	I	XV$_{DD}$	—
$\overline{\text{SD1\_RX}}$[7:4]	Receive Data(–)	AC27,AB25,AA27,Y25	I	XV$_{DD}$	—
Reserved	—	R21,P23,N21,M23, R20,P22,N20,M22	—	—	18
Reserved	—	T26,R28,P26,N28, T25,R27,P25,N27	—	—	33
SD1_PLL_TPD	PLL test point Digital	V28	O	XV$_{DD}$	18
SD1_REF_CLK	PLL Reference clock	U28	I	XV$_{DD}$	—
$\overline{\text{SD1\_REF\_CLK}}$	PLL Reference clock complement	U27	I	XV$_{DD}$	—
Reserved	—	T22	—	—	18
Reserved	—	T23	—	—	18
SerDes2(x1)					
SD2_TX[0]	Transmit data(+)	P11	O	X2V$_{DD}$	—
$\overline{\text{SD2\_TX[0]}}$	Transmit data(-)	P12	O	X2V$_{DD}$	—
SD2_RX[0]	Receive data(+)	P6	I	X2V$_{DD}$	—
$\overline{\text{SD2\_RX}}$[0]	Receive data(-)	P7	I	X2V$_{DD}$	—
Reserved	—	M11,M12	—	—	18
Reserved	—	N8, N9	—	—	34
SD2_PLL_TPD	PLL test point Digital	L7	O	X2V$_{DD}$	18
SD2_REF_CLK	PLL Reference clock	M6	I	X2V$_{DD}$	—
$\overline{\text{SD2\_REF\_CLK}}$	PLL Reference clock complement	M7	I	X2V$_{DD}$	—
Reserved	—	L8	—	X2V$_{DD}$	18
Reserved	—	L9	—	X2V$_{DD}$	18

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	—	XV_{DD}	—
S2VDD	SerDes 2 core logic supply	R6,N7,M9	—	$S2V_{DD}$	—
X2VDD	SerDes 2 transceiver supply	R11,N12,L11	—	$X2V_{DD}$	—
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13	—	V_{DD_CORE}	—
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	—	V_{DD_PLAT}	—
AVDD_CORE	CPU PLL supply	AH16	—	AV_{DD_CORE}	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV_{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV_{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV_{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV_{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	—	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V_{DD_CORE}	13
SENSEVDD_PLAT	—	W17	—	V_{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13	—	—	—
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	—	—	—

2.4.4 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the chip.

Table 8. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD}, TV_{DD} = 2.5V LV_{DD}, TV_{DD} = 3.3V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TVDD=2.5V, and from 0.6 and 2.7V for L/TVDD=3.3V at 0.6 V and 2.7 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.9.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.4.5 DDR Clock Timing

This table provides the DDR clock (DDRCLK) AC timing specifications for the chip.

Table 9. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66	—	166	MHz	1
DDRCLK cycle time	t_{DDRCLK}	6.0	—	15.15	ns	—
DDRCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	—
DDRCLK jitter	—	—	—	+/– 150	ps	3, 4

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. See Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

This figure provides the AC test load for the DDR bus.

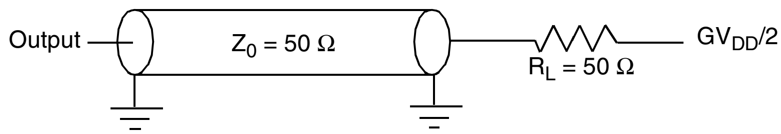

Figure 11. DDR AC Test Load

2.7 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the chip.

2.7.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the chip eSPI.

Table 20. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0\ V \le V_{IN} \le OV_{DD}$	—	±10	µA

2.7.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

Table 21. SPI AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_MOSI output—Master data hold time	t_{NIKHOX}	0.5	—	ns	3
	t_{NIKHOX}	4.0			4
SPI_MOSI output—Master data delay	t_{NIKHOV}	—	6.0	ns	3
	t_{NIKHOV}		7.4		4
SPI_CS outputs—Master data hold time	$t_{NIKHOX2}$	0	—	ns	—

2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

2.8.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.8.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	2
Maximum baud rate	CCB clock/16	baud	2,3
Oversample rate	16	—	4

Notes:

2. CCB clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

This figure shows the MII transmit AC timing diagram.

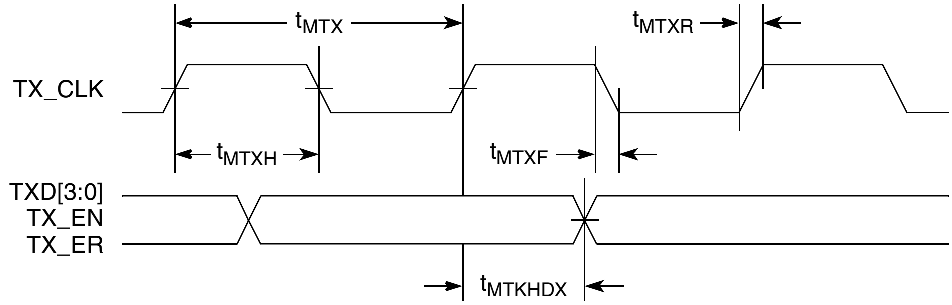

Figure 19. MII Transmit AC Timing Diagram

2.9.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 31. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

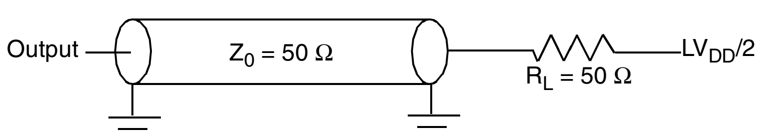

Figure 20. eTSEC AC Test Load

A timing diagram for TBI receive appears in the following figure.

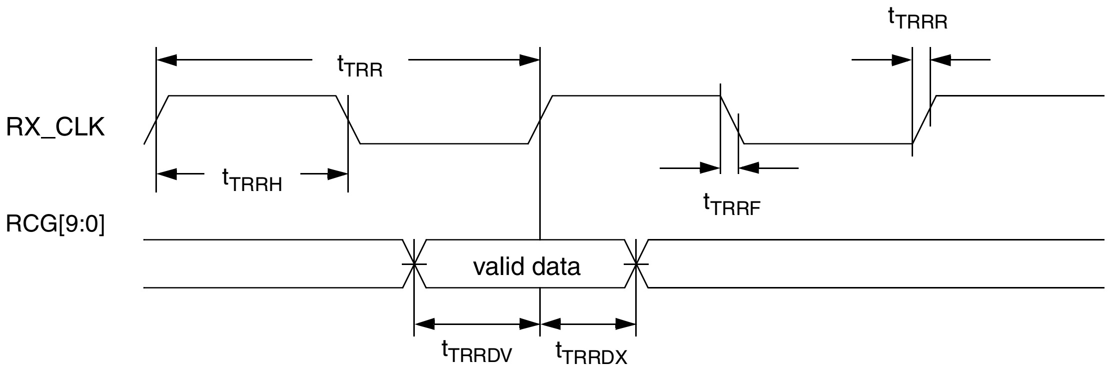

Figure 24. TBI Single-Clock Mode Receive AC Timing Diagram

2.9.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT_RX}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000BASE-T[4]	t_{RGTH}/t_{RGT}	45	—	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transition to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

2.9.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

The following tables describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) as depicted in Figure 30.

Table 39. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	$X2V_{DD}$	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$X2V_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	VOL	$X2V_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between "0" and "1"	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between "0" and "1"	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Notes:

1. This will not align to DC-coupled SGMII. $X2V_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of the chip's SerDes 2 control register:

- The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
- The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.

4. V_{OS} is also referred to as output common mode voltage.

- 5.The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $X2V_{DD\text{-}Typ}$=1.0V, no common mode offset variation (VOS =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

2.12 enhanced Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

2.12.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 48. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	1.9	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 49. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This figures show the local bus signals.

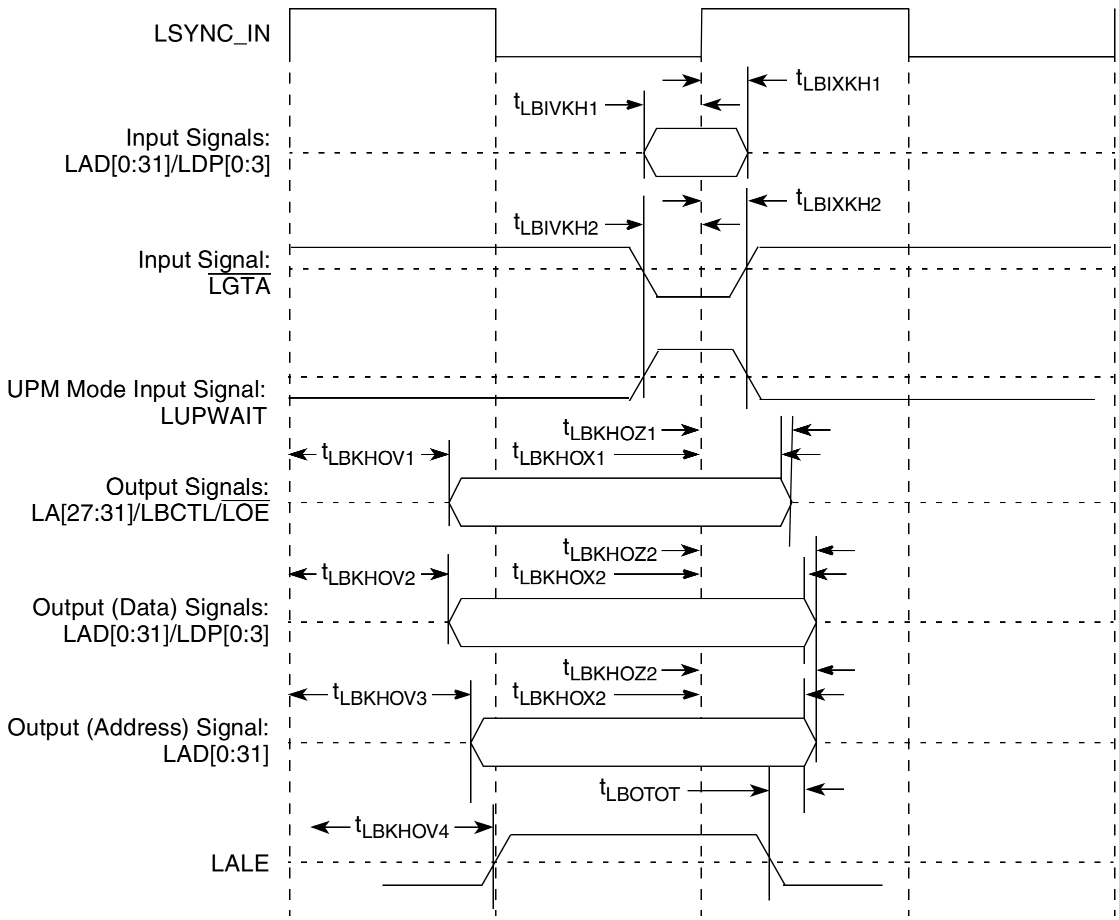

Figure 39. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

NOTE

In PLL bypass mode, some signals are launched and captured on the opposite edge of LCLK[n] to that used in PLL Enable Mode. In this mode, output signals are launched at the falling edge of the LCLK[n] and inputs signals are captured at the rising edge of LCLK[n] with the exception of LGTA/LUPWAIT (which is captured at the falling edge of the LCLK[n]).

This figure provides the AC test load for TDO and the boundary-scan outputs.

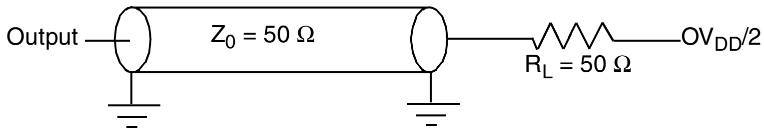

Figure 45. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

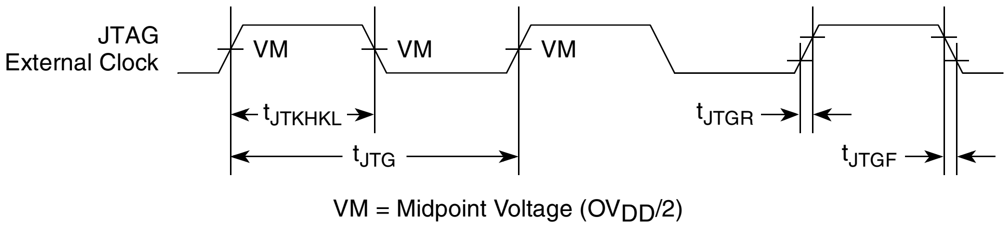

Figure 46. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

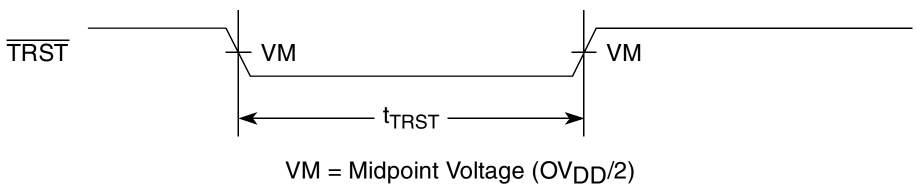

Figure 47. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

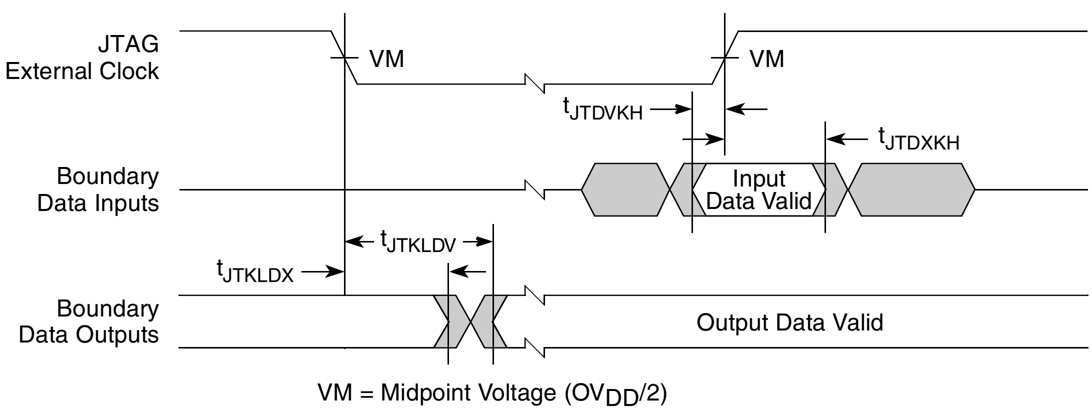

Figure 48. Boundary-Scan Timing Diagram

2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

Table 59. Reference Clock Input Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD2_REF_CLK/_B reference clock cycle time	t_{CLK_REF}	100	—	150	MHz	1
SD2_REF_CLK/_B frequency tolerance	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/_B rise/fall time (80%-20%)	$t_{CLK\_RISE}/t_{CLK\_FALL}$	—	—	1	ns	—
SD_REF_CLK/_B duty cycle (@50% X2VDD)	t_{CLK_DUTY}	45	50	55	%	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter (peak-to-peak)	t_{CLK_PJ}	–50	—	+50	ps	2,3

Note:

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

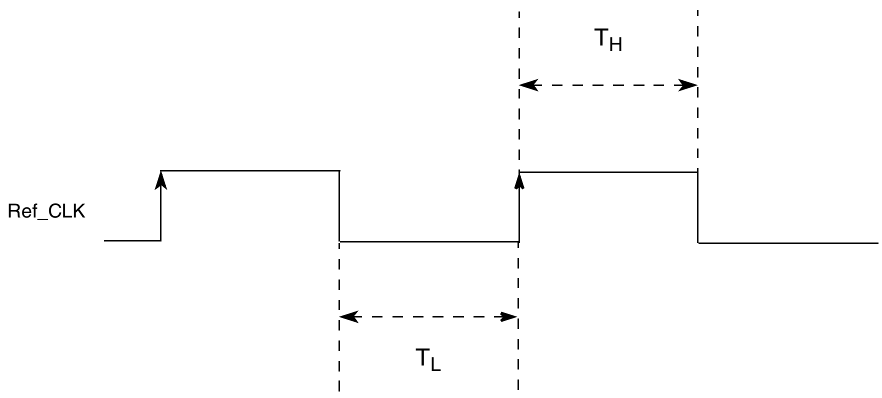

Figure 49. Reference Clock Timing Waveform

— The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. See the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range

— When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.

— This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1V above SnGND (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800mV with the common mode voltage at 400mV.

— If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SnGND (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.

- The input amplitude requirement

— This requirement is described in detail in the following sections.

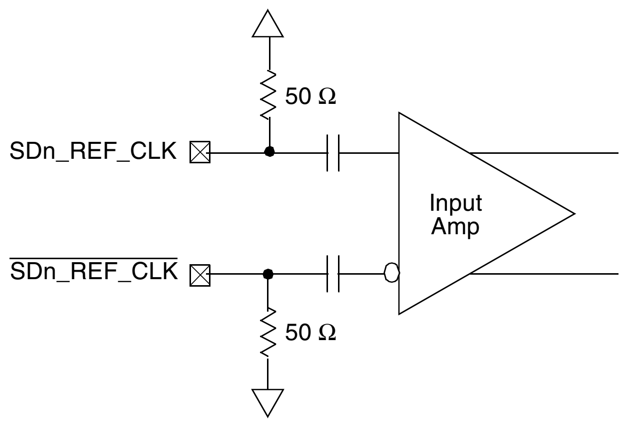

Figure 58. Receiver of SerDes Reference Clocks

Table 71. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.
$T_{TX\text{-}EYE}$	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX\text{-}CM\text{-}ACp} = RMS(\lvert V_{TXD+} + V_{TXD-}\rvert/2 - V_{TX\text{-}CM\text{-}DC})$ $V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ See Note 2
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$\lvert V_{TX\text{-}CM\text{-}DC\ (during\ L0)} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ (During\ Electrical\ Idle)}\rvert <= 100$ mV $V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [L0] $V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [Electrical Idle] See Note 2.
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-}\rvert <= 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+}\rvert$ $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}IDLE\text{-}DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX\text{-}IDLE\text{-}DIFFp} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-}\rvert <= 20$ mV See Note 2.
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX\text{-}DC\text{-}CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

2.21.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 69 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

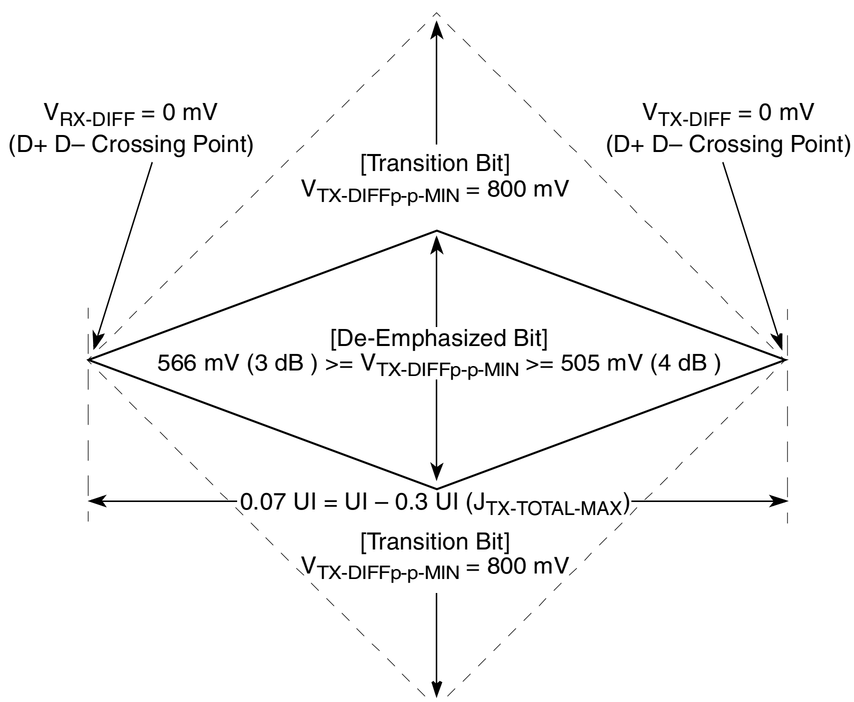

Figure 69. Minimum Transmitter Timing and Voltage Output Compliance Specifications

2.23.1 Clock Ranges

This table provides the clocking specifications for the processor cores and Table 74 provides the clocking specifications for the memory bus.

Table 73. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	600 MHz		800 MHz		1000 MHz		1250 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	600	600	600	800	600	1000	600	1250	MHz	1, 2
CCB frequency	400	400	400	400	333	400	333	500		
DDR Data Rate	400	400	400	400	400	400	400	500		

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," Section 2.23.3, "e500 Core PLL Ratio,"and Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. This table provides the clocking specifications for the memory bus.

Table 74. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	600, 800, 1000, 1250			
	Min	Max		
DDR Memory bus clock speed	200	250	MHz	1, 2, 3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," Section 2.23.3, "e500 Core PLL Ratio," and Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The Memory bus clock refers to the chip's memory controllers' MCK[0:5] and $\overline{\text{MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 2.23.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, “CCB/SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, “e500 Core PLL Ratio.”
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, “DDR/DDRCLK PLL Ratio.”

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

5. Capacitors may not be present on all devices
6. Caution must be taken not to short exposed metal capacitor pads on package top.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

6 Product Documentation

The following documents are required for a complete description of the chip and are needed to design properly with the part.

- *MPC8536E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8536ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)

7 Document Revision History

This table provides a revision history for this hardware specification.

Table 85. Document Revision History

Revision	Date	Substantive Change(s)
5	09/2011	• Removed PVDD from Table 1, "Pinout Listing."
4	06/2011	• In Table 1, "Pinout Listing," updated the power supply for TSEC3 pins to TVDD. • Updated Table 56, "eSDHC AC Timing Specifications." • In Section 4.3, "Part Numbering," added an extra bin (1250/500/667) to support DDR3.
3	11/2010	• In Table 1, "Pinout Listing," added the following note: "For systems that boot from Local Bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required..." In addition, updated footnote 26 and added footnote 29 to PCI1_AD. • Updated Table 21 • Updated Figure 25, "RGMII and RTBI AC Timing and Multiplexing Diagrams." • In Table 44, "MII Management DC Electrical Characteristics," changed the Voh/Vol values for MDIO/MDC. • Added Note 6 regarding USB*n*_DIR pin to Table 47, "USB General Timing Parameters6." • In Table 64, "I2C AC Electrical Specifications," updated footnote 2. • In Table 82, , Table 83, , Table 84, added the Revision Level A for Rev 1.2
2	09/2009	**Note:** • In Section 1, "Pin Assignments and Reset States,"updated the first sentence of the note to say, "The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration." • In Table 40, "SGMII DC Receiver Electrical Characteristics," changed LSTSAB to LSTSA and LSTSEF to LSTSE for Note 4. • Updated Die value and Bump/Underfill value in Table 84 **Note:** Updated Figure 81, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA," and its notes.
1	09/2009	• In Table 3, "Recommended Operating Conditions," for $V_{DD\_CORE,}$ removed 1.1 ± 55 mV. • In Table 5, "Power Dissipation 5," remove note 5. • In Table 5, "Power Dissipation 5," changed an "—"' to "0."
0	08/2009	• Initial public release.

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