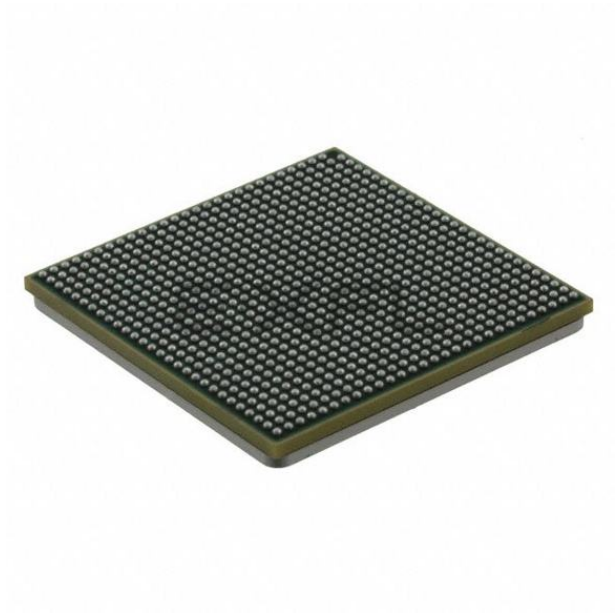

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535eavtanga

1.1 Pin Map

See Table 1 for the MPC8535E pinout, which is a subset of the MPC8536E.

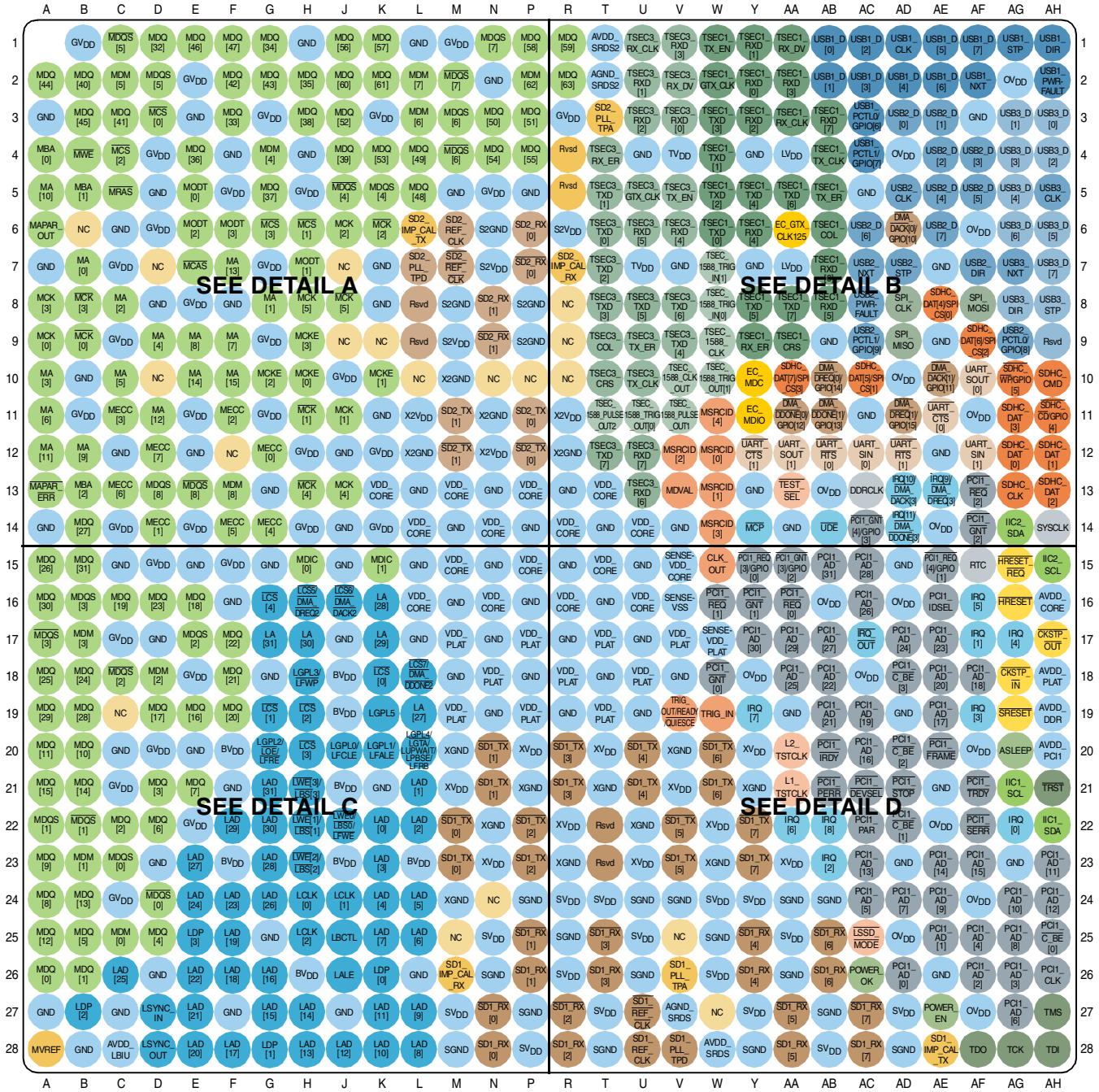


Figure 2. Chip Pin Map Bottom View

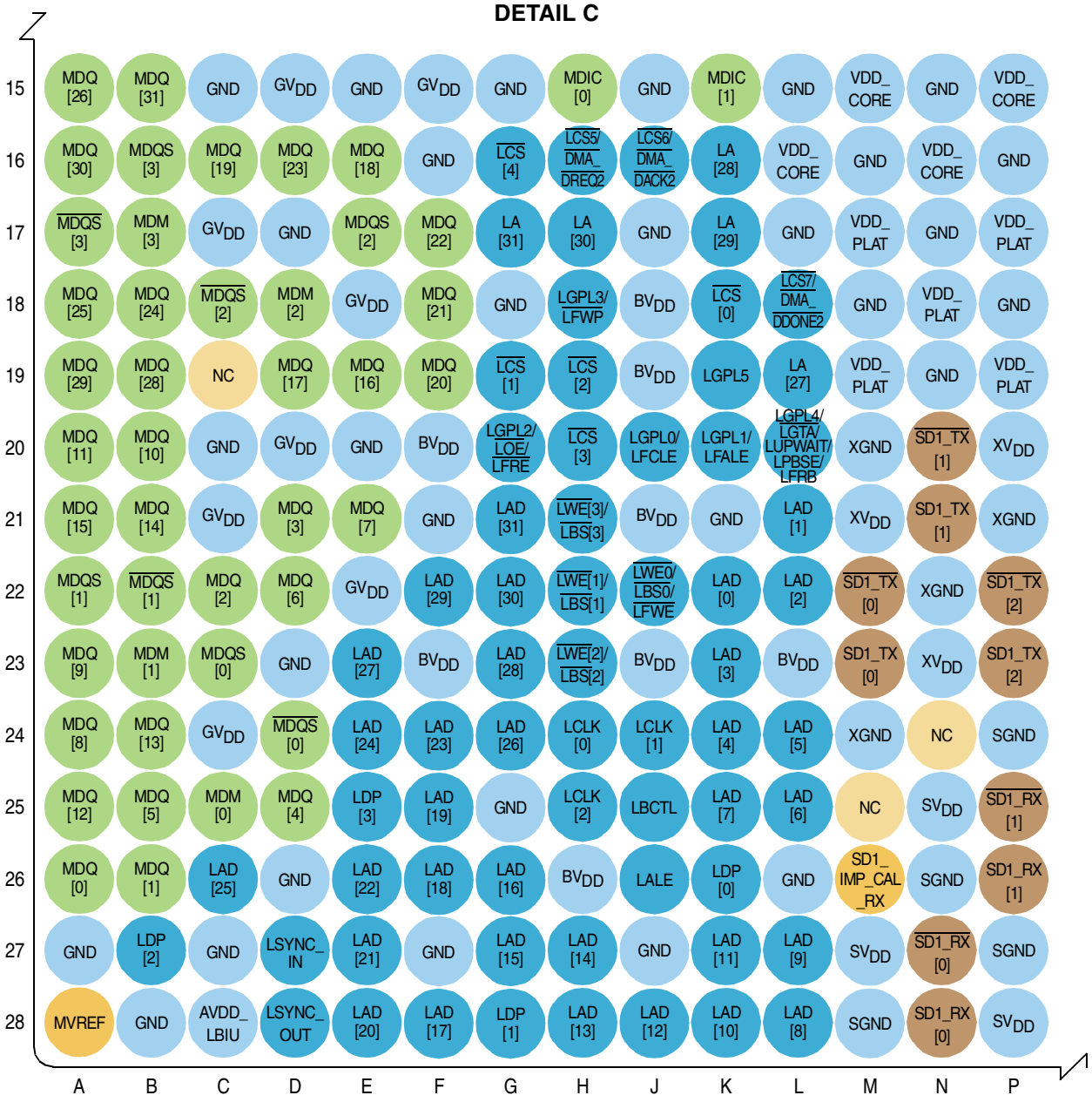


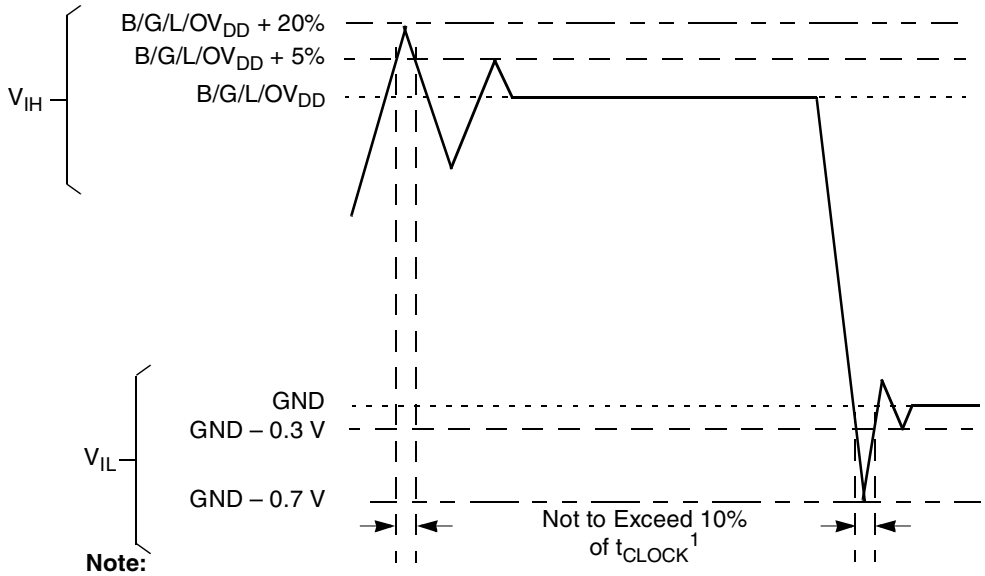
Figure 5. Chip Pin Map Detail C

This table provides the pin-out listing for the 783 FC-PBGA package.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
PCI					
PCI1_AD[31:0]	Muxed Address / data	AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26	I/O	OV_{DD}	—
$\overline{\text{PCI1\_C\_BE[3:0]}}$	Command/Byte Enable	AD18, AD20,AD22, AH25	I/O	OV_{DD}	29
PCI1_PAR	Parity	AC22	I/O	OV_{DD}	29
$\overline{\text{PCI1\_FRAME}}$	Frame	AE20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_TRDY}}$	Target Ready	AF21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_IRDY}}$	Initiator Ready	AB20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_STOP}}$	Stop	AD21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_DEVSEL}}$	Device Select	AC21	I/O	OV_{DD}	2,29
PCI1_IDSEL	Init Device Select	AE16	I	OV_{DD}	29
$\overline{\text{PCI1\_PERR}}$	Parity Error	AB21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_SERR}}$	System Error	AF22	I/O	OV_{DD}	2,4,29
$\overline{\text{PCI1\_REQ}}$[4:3]/GPIO[1:0]	Request	AE15,Y15	I	OV_{DD}	—
$\overline{\text{PCI1\_REQ}}$[2:1]	Request	AF13,W16	I	OV_{DD}	29
$\overline{\text{PCI1\_REQ}}$[0]	Request	AA16	I/O	OV_{DD}	29
$\overline{\text{PCI1\_GNT}}$[4:3]/GPIO[3:2]	Grant	AC14, AA15	O	OV_{DD}	
$\overline{\text{PCI1\_GNT}}$[2:1]	Grant	AF14,Y16	O	OV_{DD}	5,9,25,29
$\overline{\text{PCI1\_GNT}}$[0]	Grant	W18	I/O	OV_{DD}	29
PCI1_CLK	PCI Clock	AH26	I	OV_{DD}	29

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For eLBC, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI1_CLK or SYSCLK.

2. With the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 7. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The core voltage must always be provided at nominal 1.0 V . (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.3 Power Characteristics

The estimated power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III chips is shown in the following table.

Table 5. Power Dissipation [5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	600	400	400	1.0	1.0	105 /90	—	4.1/3.3	—	4.7/3.7	1, 3, 8
Thermal (W)							—	3.7/2.9	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.5	—	1.5	—	1, 2
Doze (W)							1.2	1.9	1.4	1.9	1
Nap (W)							0.8	1.5	1.4	1.9	1
Sleep (W)							0.8	1.5	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	6
Maximum (A)	800	400	400	1.0	1.0	105 / 90	—	4.5/3.7	—	4.7/3.7	1, 3, 8
Thermal (W)							—	3.9/3.1	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.7	—	1.5	—	1, 2
Doze (W)							1.3	2.1	1.4	1.9	1
Nap (W)							0.8	1.5	1.4	1.9	1
Sleep (W)							0.8	1.5	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	1,6
Maximum (A)	1000	400	400	1.0	1.0	105 / 90	—	4.8/4.0	—	4.7/3.7	1, 3, 8
Thermal (W)							—	4.1/3.3	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.9	—	1.5	—	1, 2
Doze (W)							1.4	2.2	1.4	1.9	1
Nap (W)							0.8	1.6	1.4	1.9	1
Sleep (W)							0.8	1.6	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	1, 6

2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

2.8.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.8.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	2
Maximum baud rate	CCB clock/16	baud	2,3
Oversample rate	16	—	4

Notes:

2. CCB clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

This figure shows the GMII transmit AC timing diagram.

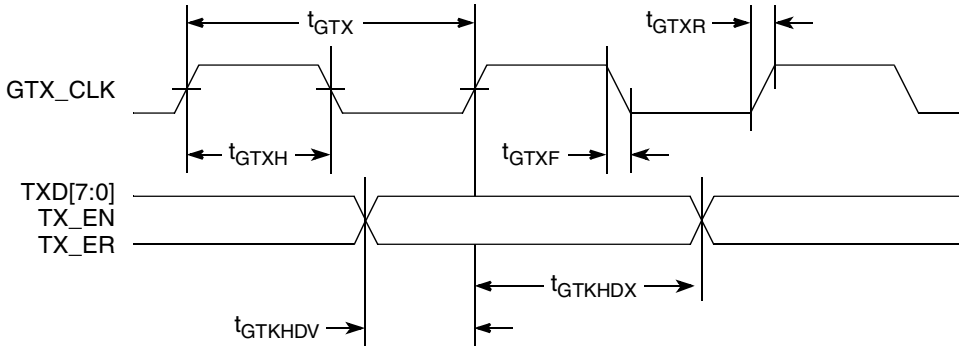


Figure 16. GMII Transmit AC Timing Diagram

2.9.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

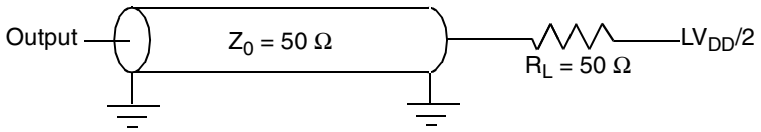


Figure 17. eTSEC AC Test Load

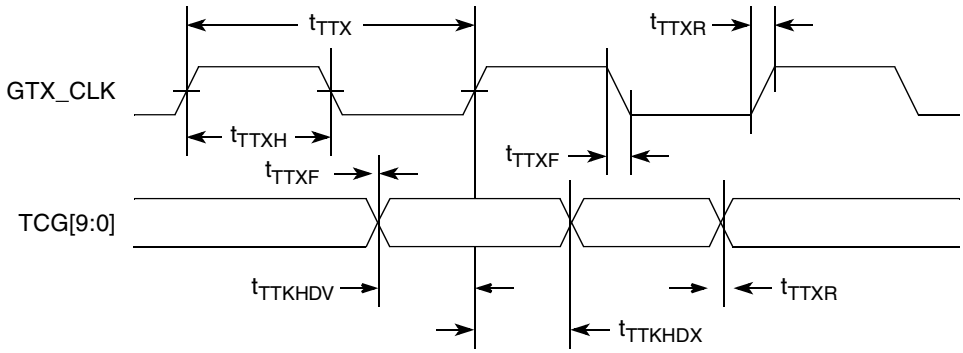


Figure 22. TBI Transmit AC Timing Diagram

2.9.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition[2]	Symbol [1]	Min	Typ	Max	Unit
Clock period for TBI Receive Clock 0, 1	t_{TRX}	—	16.0	—	ns
Skew for TBI Receive Clock 0, 1	t_{SKTRX}	7.5	—	8.5	ns
Duty cycle for TBI Receive Clock 0, 1	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1	t_{TRDXKH}	1.5	—	—	ns
Clock rise time (20%-80%) for TBI Receive Clock 0, 1	t_{TRXR}	0.7	—	2.4	ns
Clock fall time (80%-20%) for TBI Receive Clock 0, 1	t_{TRXF}	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. The signals “TBI Receive Clock 0” and “TBI Receive Clock 1” refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

A timing diagram for TBI receive appears in the following figure.

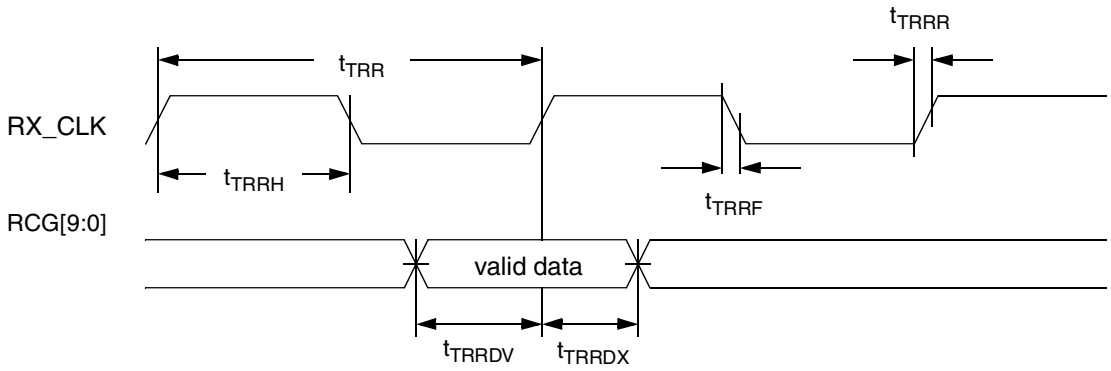


Figure 24. TBI Single-Clock Mode Receive AC Timing Diagram

2.9.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT_RX}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000BASE-T[4]	t_{RGTH}/t_{RGT}	45	—	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transition to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

2.9.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

The following tables describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) as depicted in Figure 30.

Table 39. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	$X2V_{DD}$	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$X2V_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$X2V_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Notes:

1. This will not align to DC-coupled SGMII. $X2V_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of the chip’s SerDes 2 control register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
   - 5.The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $X2V_{DD\text{-}Typ}$=1.0V, no common mode offset variation (VOS =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

2.9.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 31 shows the SGMII Receiver Input Compliance Mask eye diagram.

Table 42. SGMII Receive AC Timing Specifications

At recommended operating conditions with $X2V_{DD}$ = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the chip transmitter outputs.

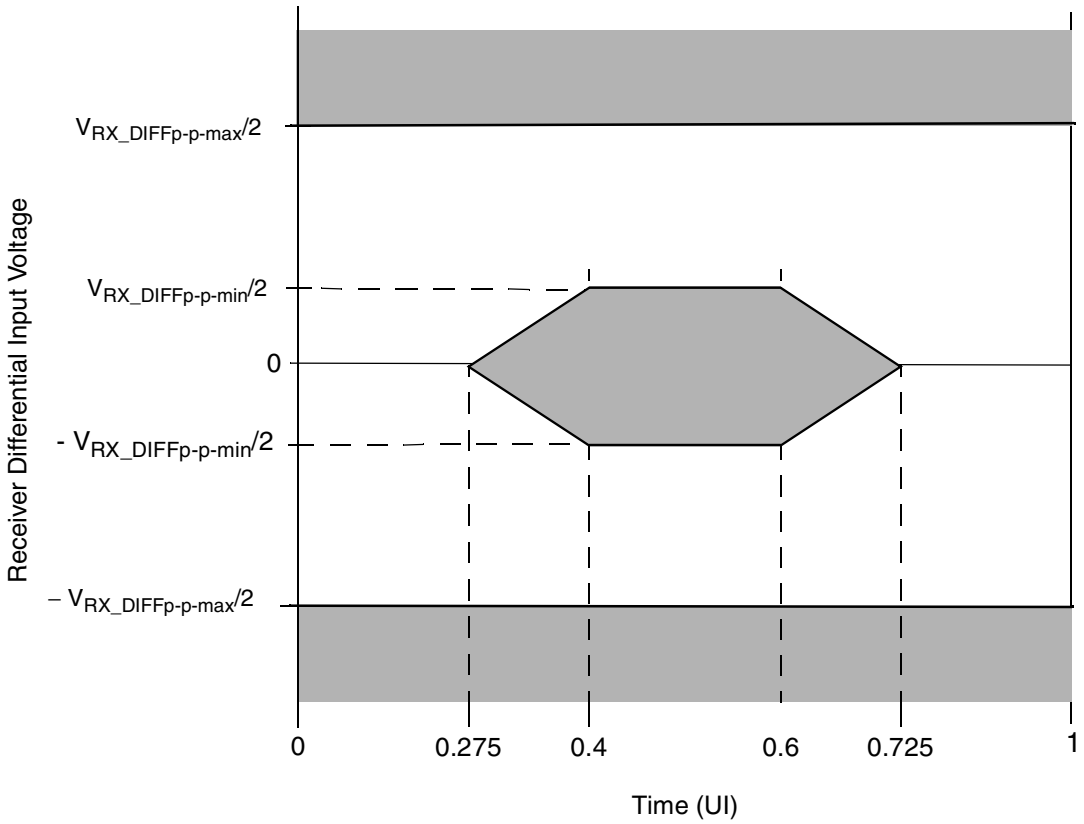


Figure 31. SGMII Receiver Input Compliance Mask

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDIO to EC_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
EC_MDC rise time	t_{MDCR}	—	—	10	ns	—
EC_MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. t_{CLKplb_clk} is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time t_{MDKHDX}. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

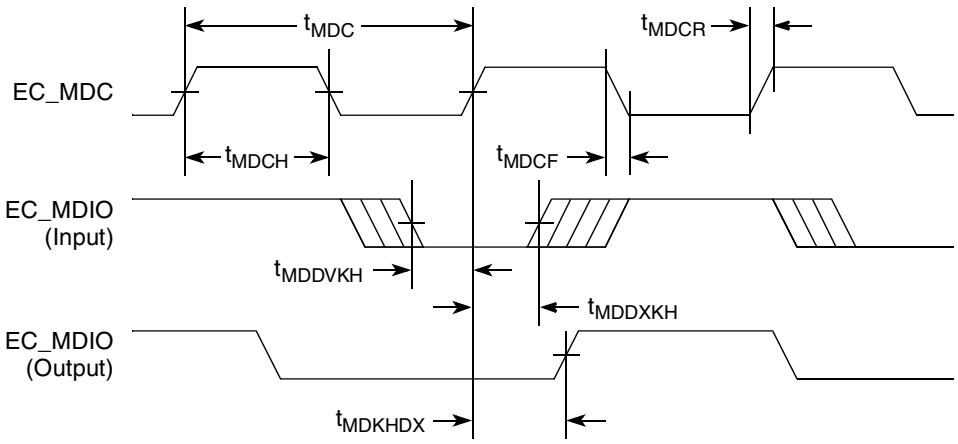


Figure 35. MII Management Interface Timing Diagram

2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

This figures provide the AC test load and signals for the USB, respectively.

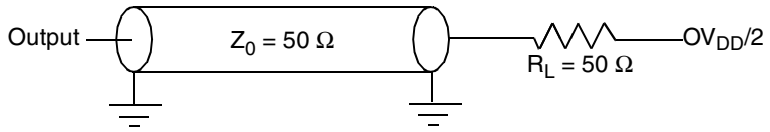


Figure 36. USB AC Test Load

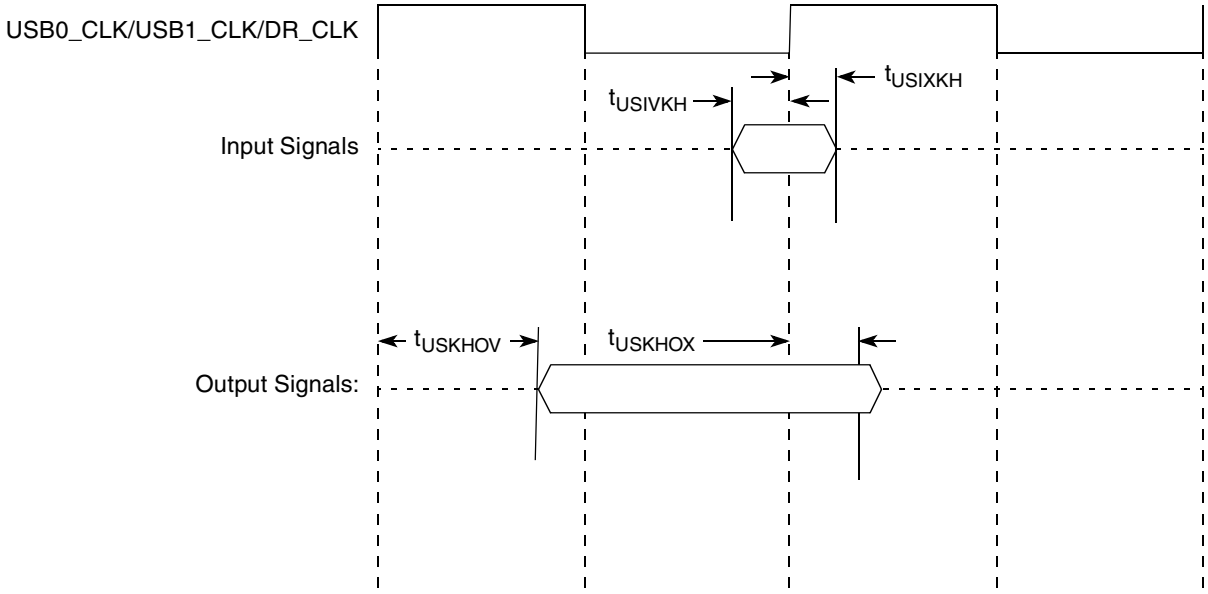


Figure 37. USB Signals

Table 53. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC) (continued)

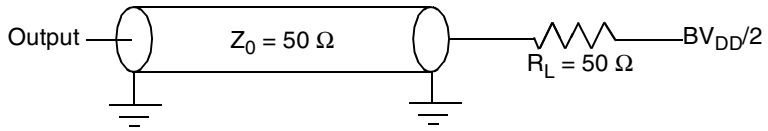
Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	—	$t_{LBKHOX2}$	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	—	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	—	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This figure provides the AC test load for the local bus.

Figure 38. Local Bus AC Test Load



This figure provides the AC test load for TDO and the boundary-scan outputs.

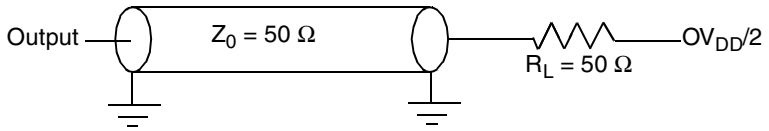


Figure 45. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

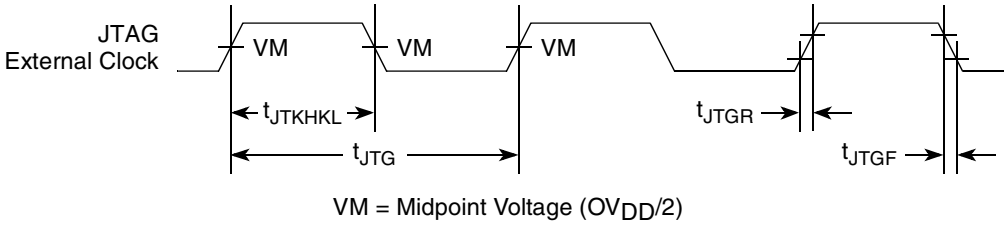


Figure 46. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

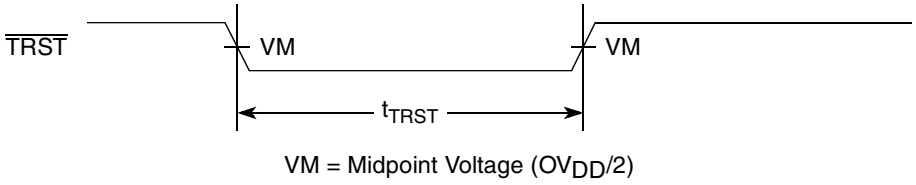


Figure 47. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

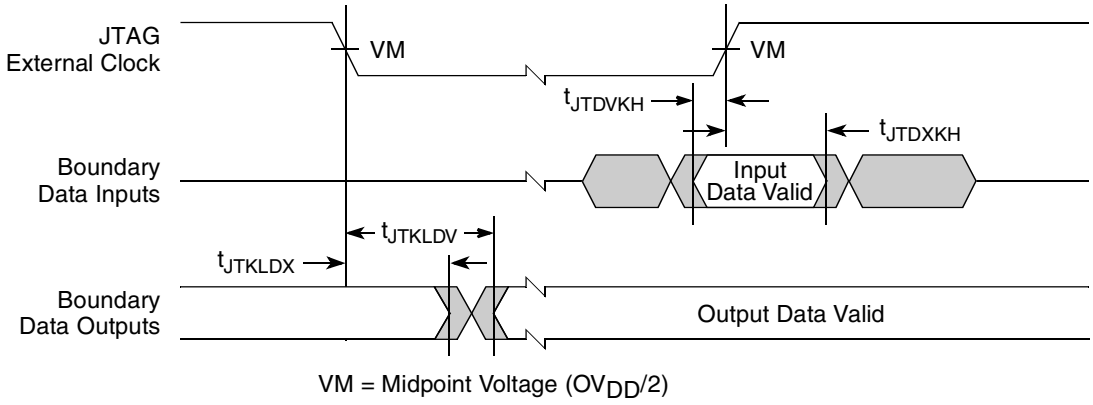


Figure 48. Boundary-Scan Timing Diagram

2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with chip's SerDes reference clock input's DC requirement.

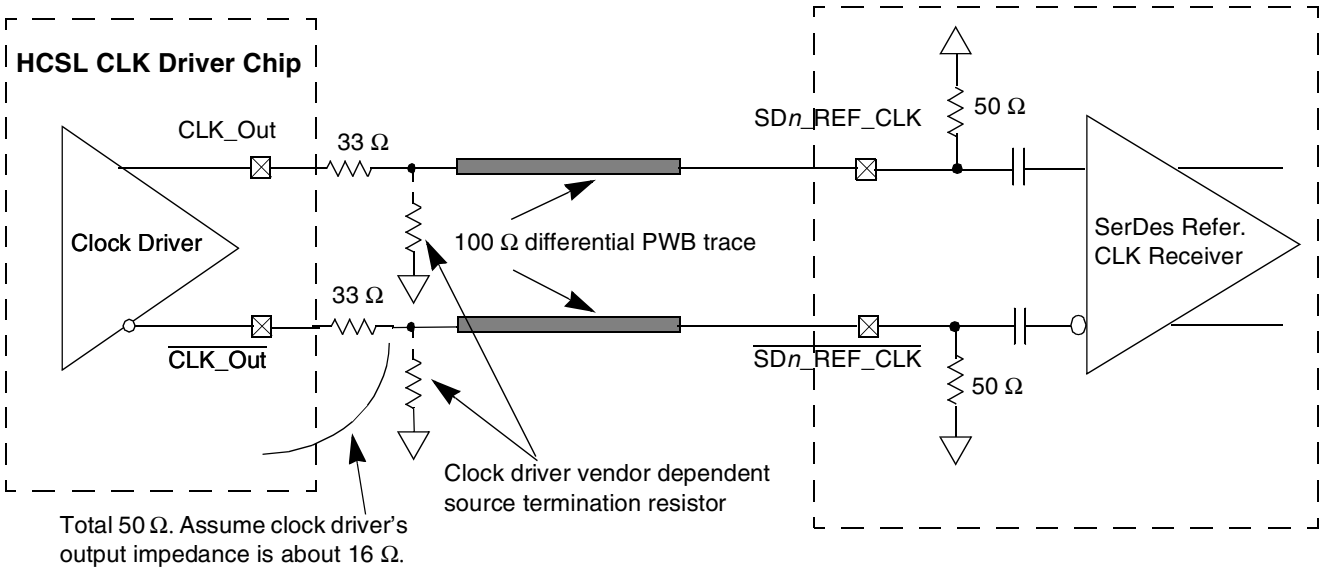


Figure 62. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the chip's SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

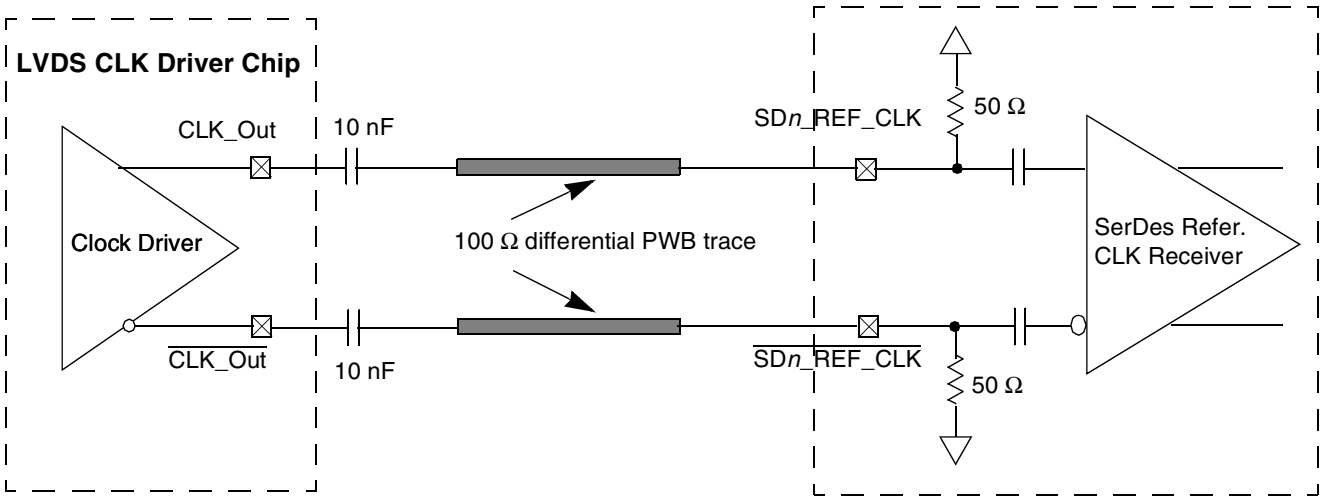


Figure 63. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Table 77. DDR Clock Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	cfg_ddr_pll[0:2]	000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

2.23.6 Frequency Options

2.23.6.1 SYSCLK to Platform Frequency Options

This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 78. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)						
3						333	400
4				333	400	444	
5			333	415	500		
6			400	500			
8		333					
10	333	417					
12	400	500					

2.24 Thermal

This section describes the thermal specifications of the chip.

2.24.1 Thermal Characteristics

This table provides the package thermal characteristics.

Table 79. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	18	°C/W	1, 2

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

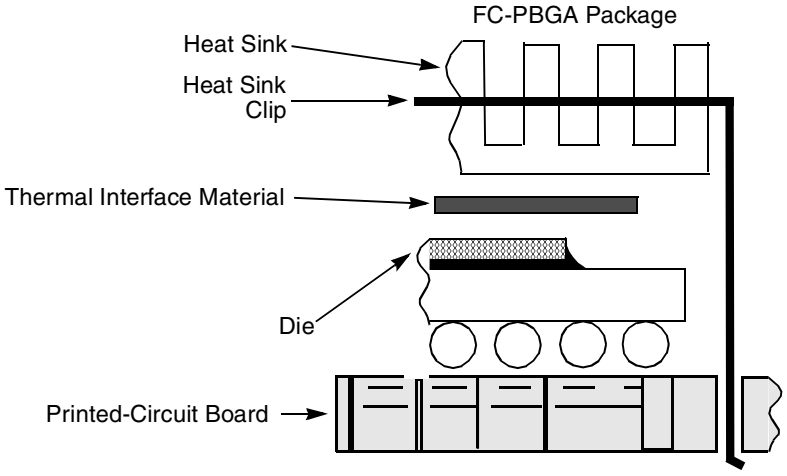


Figure 73. Package Exploded Cross-Sectional View with Several Heat Sink Options

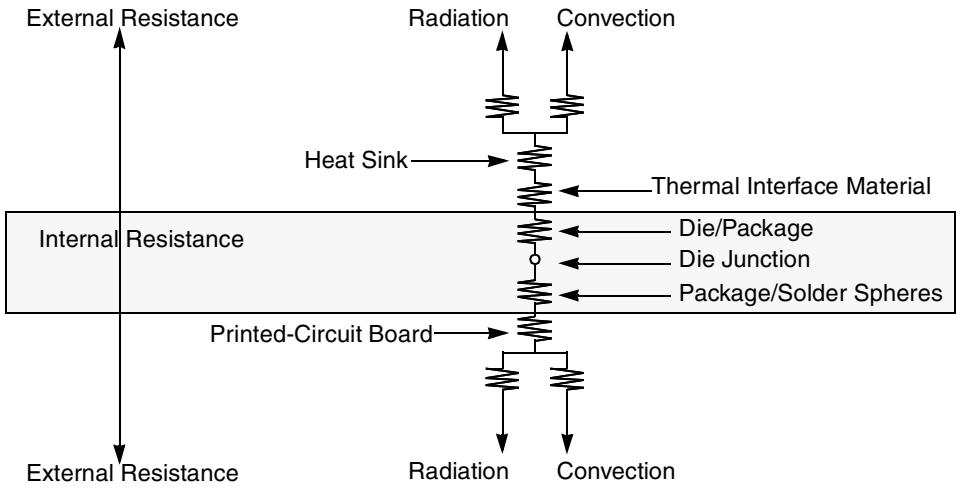
The system board designer can choose between several types of heat sinks to place on the chip. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the chip to function in various environments.

2.24.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 70, the intrinsic internal conduction thermal resistance paths are as follows:

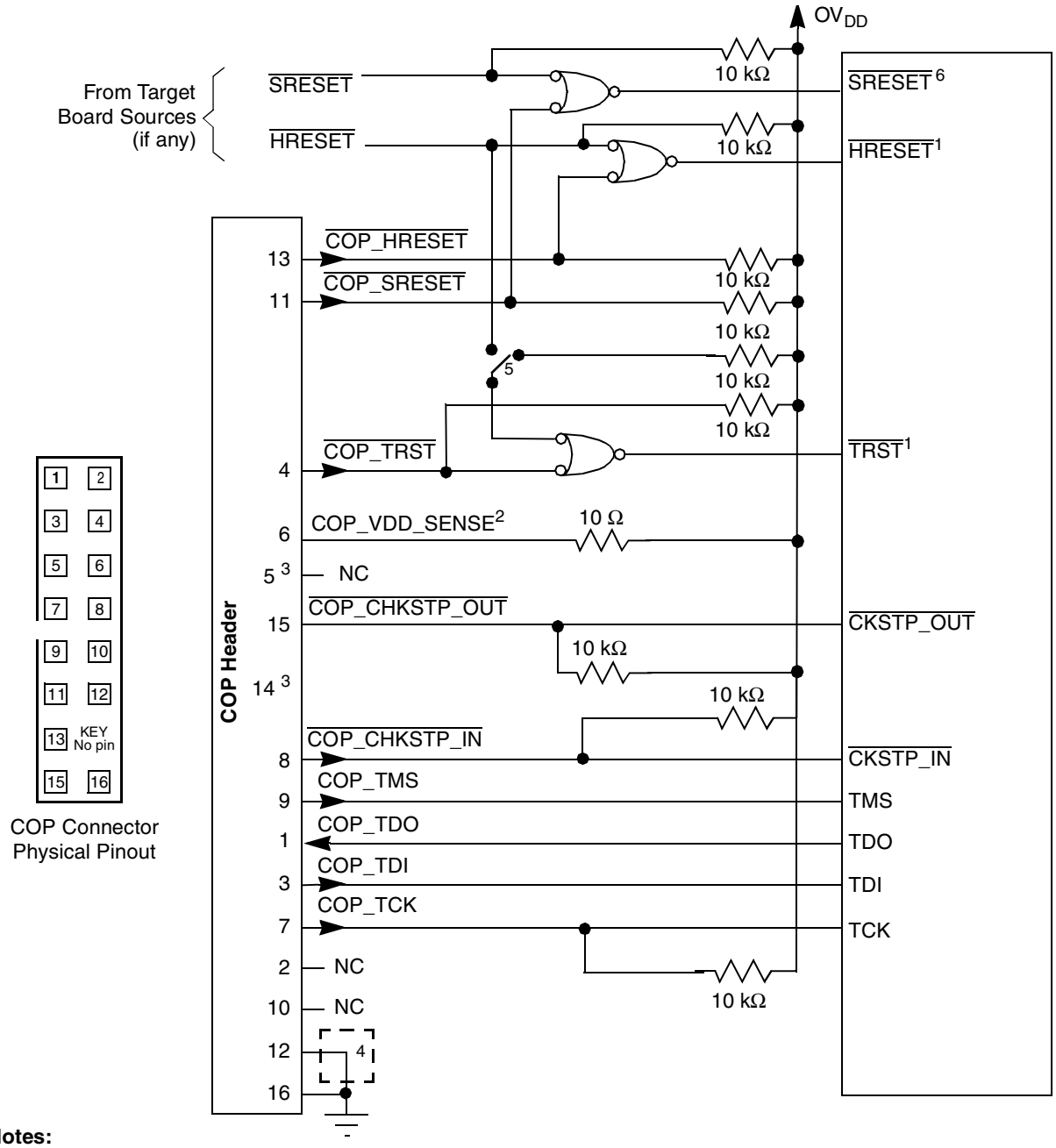
- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 78. JTAG Interface Connection