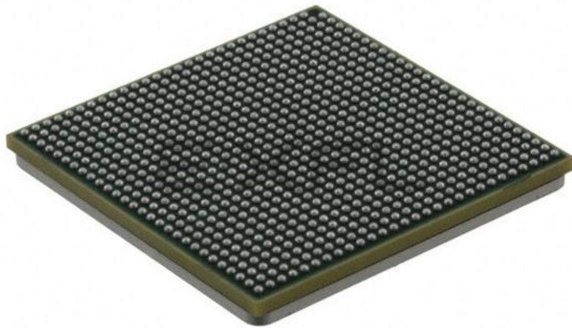

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8535ebvtanga

This figure shows the major functional units within the chip.

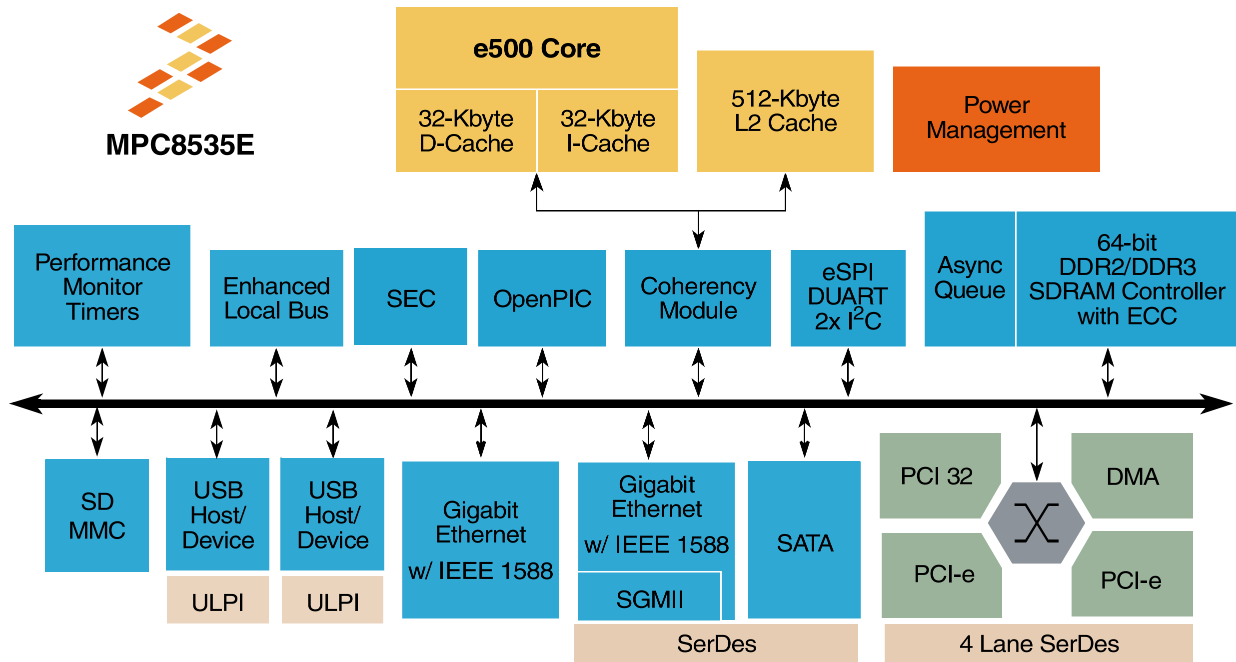

Figure 1. Chip Block Diagram

1 Pin Assignments and Reset States

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ[0:63]	Data	A26,B26,C22,D21,D25, B25,D22,E21,A24,A23, B20,A20,A25,B24,B21, A21,E19,D19,E16,C16, F19,F18,F17,D16,B18, A18,A15,B14,B19,A19, A16,B15,D1,F3,G1,H2, E4,G5,H3,J4,B2,C3,F2, G2,A2,B3,E1,F1,L5,L4, N3,P3,J3,K4,N4,P4,J1, K1,P1,R1,J2,K2,P2,R2	I/O	GV_{DD}	—
MECC[0:7]	Error Correcting Code	G12,D14,F11,C11, G14,F14,C13,D12	I/O	GV_{DD}	—
$\overline{\text{MAPAR_ERR}}$	Address Parity Error	A13	I	GV_{DD}	—
MAPAR_OUT	Address Parity Out	A6	O	GV_{DD}	—
MDM[0:8]	Data Mask	C25,B23,D18,B17,G4, C2,L3,L2,F13	O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	Data Strobe	D24,B22,C18,A17,J5, C1,M4,M2,E13	I/O	GV_{DD}	—
MDQS[0:8]	Data Strobe	C23,A22,E17,B16,K5, D2,M3,N1,D13	I/O	GV_{DD}	—
MA[0:15]	Address	B7,G8,C8,A10,D9,C10, A11,F9,E9,B12,A5, A12,D11,F7,E10,F10	O	GV_{DD}	—
MBA[0:2]	Bank Select	A4,B5,B13	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	B4	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	C5	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	E7	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	Chip Select	D3,H6,C4,G6	O	GV_{DD}	—
MCKE[0:3]	Clock Enable	H10,K10,G10,H9	O	GV_{DD}	11
MCK[0:5]	Differential Clock 3 Pairs / DIMM	A9,J11,J6,A8,J13,H8	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	Differential Clock 3 Pairs / DIMM	B9,H11,K6,B8,H13,J8	O	GV_{DD}	—
MODT[0:3]	On Die Termination	E5,H7,E6,F6	O	GV_{DD}	—
MDIC[0:1]	Calibration	H15,K15	I/O	GV_{DD}	26
Local Bus Controller Interface					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_CLK	Transmit clock In	U10	I	TV_{DD}	—
TSEC3_GTX_CLK	Transmit clock Out	U5	O	TV_{DD}	—
TSEC3_CRS	Carrier sense	T10	I/O	TV_{DD}	17
TSEC3_COL	Collision detect	T9	I	TV_{DD}	—
TSEC3_RXD[7:0]	Receive data	U12,U13,U6,V6,V1,U3, U2,V3	I	TV_{DD}	—
TSEC3_RX_DV	Receive data valid	V2	I	TV_{DD}	—
TSEC3_RX_ER	Receive data error	T4	I	TV_{DD}	—
TSEC3_RX_CLK	Receive clock	U1	I	TV_{DD}	—
IEEE 1588					
TSEC_1588_CLK	Clock In	W9	I	LV_{DD}	29
TSEC_1588_TRIG_IN[0:1]	Trigger In	W8,W7	I	LV_{DD}	29
TSEC_1588_TRIG_OUT[0:1]	Trigger Out	U11,W10	O	LV_{DD}	5,9,29
TSEC_1588_CLK_OUT	Clock Out	V10	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT1	Pulse Out1	V11	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT2	Pulse Out2	T11	O	LV_{DD}	5,9,29
eSDHC					
SDHC_CMD	Command line	AH10	I/O	OV_{DD}	29
$\overline{\text{SDHC_CD}}$/GPIO[4]	Card detection	AH11	I	OV_{DD}	—
SDHC_DAT[0:3]	Data line	AG12,AH12,AH13, AG11	I/O	OV_{DD}	29
SDHC_DAT[4:7] / SPI_CS[0:3]	8-bit MMC Data line / SPI chip select	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
SDHC_CLK	SD/MMC/SDIO clock	AG13	I/O	OV_{DD}	29
$\overline{\text{SDHC_WP}}$/GPIO[5]	Card write protection	AG10	I	OV_{DD}	1, 32
eSPI					
SPI_MOSI	Master Out Slave In	AF8	I/O	OV_{DD}	29
SPI_MISO	Master In Slave Out	AD9	I	OV_{DD}	29
SPI_CLK	eSPI clock	AD8	I/O	OV_{DD}	29
SPI_CS[0:3] / SDHC_DAT[4:7]	eSPI chip select / SDHC 8-bit MMC data	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
DUART					
$\overline{\text{UART_CTS}}$[0:1]	Clear to send	AE11,Y12	I	OV_{DD}	29
$\overline{\text{UART_RTS}}$[0:1]	Ready to send	AB12,AD12	O	OV_{DD}	29
UART_SIN[0:1]	Receive data	AC12,AF12	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	–0.3 to 1.21	V	—
Platform supply voltage		V_{DD_PLAT}	–0.3 to 1.1	V	—
PLL core supply voltage		AV_{DD_CORE}	–0.3 to 1.21	V	—
PLL other supply voltage		AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers		SV_{DD}, $S2V_{DD}$	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}, $X2V_{DD}$	–0.3 to 1.1	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface		–0.3 to 1.65		
Three-speed Ethernet I/O		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	2
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	2
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	^0C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.
2. The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	1.0 ± 50 mV	V	—
Platform supply voltage		V_{DD_PLAT}	1.0 ± 50 mV	V	—
PLL core supply voltage		AV_{DD_CORE}	1.0 ± 50 mV	V	2
PLL other supply voltage		AV_{DD}	1.0 ± 50 mV	V	2
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}	1.0 ± 50 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V ± 90 mV	V	3
	DDR3 SDRAM Interface		1.5 V ± 75 mV		
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	5
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	3.3 V ± 165 mV	V	4
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 and DDR3 SDRAM Interface reference	MV_{REF}	$GV_{DD}/2 \pm 1\%$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	5
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	4
Operating Temperature range	Commercial	T_A T_J	T_A= 0 (min) to T_J= 90(max)	°C	6
	Industrial standard temperature range		T_A= 0 (min) to T_J= 105 (max)		
	Extended temperature range		T_A= -40 (min) to T_J= 105 (max)		

Notes:

2. This voltage is the input to the filter discussed in Section 3.2.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
3. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	3
DDR3 signal	20 40 (half strength mode)	GV_{DD} = 1.5 V	2
TSEC signals	42	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I^2C	150	OV_{DD} = 3.3 V	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI1_GNT1}}$ signal at reset.
3. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min)

2.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper chip operation. These requirements are as follows for power up:

1. V_{DD_PLAT}, V_{DD_CORE} (if POWER_EN is not used to control V_{DD_CORE}), AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD},$S2V_{DD}$, TV_{DD}, XV_{DD} and $X2V_{DD}$
2. [Wait for POWER_EN to assert], then V_{DD_CORE} (if POWER_EN is used to control V_{DD_CORE})
3. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD platform supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the chip.

During the Deep Sleep state, the VDD core supply is removed. But all other power supplies remain applied. Therefore, there is no requirement to apply the VDD core supply before any other power rails when the silicon waking from Deep Sleep.

Table 17. DDR3 SDRAM Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606MHz and 667MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
667 MHz	—	–240	240	—	3
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} =+/-(T/4 - abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR2 and DDR3 frequency is 667MHz.

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

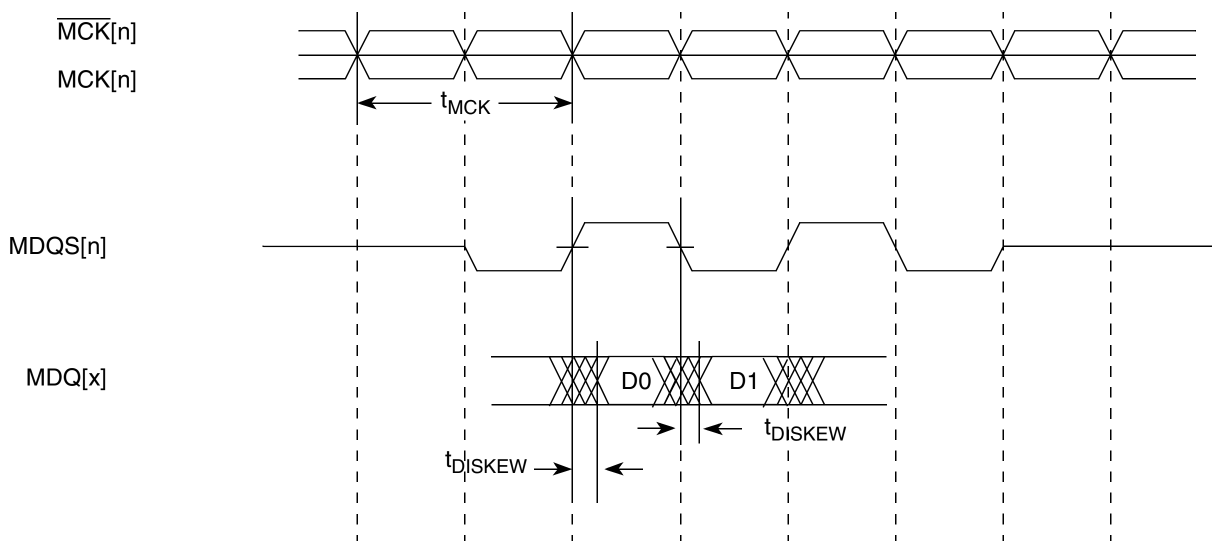

Figure 8. DDR SDRAM Input Timing Diagram

This figure provides the AC test load for the DDR bus.

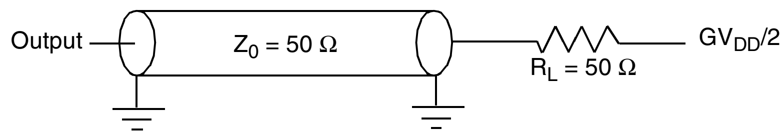

Figure 11. DDR AC Test Load

2.7 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the chip.

2.7.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the chip eSPI.

Table 20. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

2.7.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

Table 21. SPI AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_MOSI output—Master data hold time	t_{NIKHOX}	0.5	—	ns	3
	t_{NIKHOX}	4.0			4
SPI_MOSI output—Master data delay	t_{NIKHOV}	—	6.0	ns	3
	t_{NIKHOV}		7.4		4
SPI_CS outputs—Master data hold time	$t_{NIKHOX2}$	0	—	ns	—

The IEEE 1588 AC timing specifications are in the following table.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	T_{TX_CLK}*7	ns	1
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2*$t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK_MAX}$	—	—	ns	2

Note:

1. When TMR_CTRL[CKSEL]=00, the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in the Table above. The maximum value of $t_{T1588CLK}$ is defined in terms of T_{TX_CLK}, which is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running.
   When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.
   See the *MPC8536E PowerQUICC III Integrated Communications Processor Reference Manual* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

2.10 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals EC_MDIO (management data input/output) and EC_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in Section 2.9, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management”

This figures provide the AC test load and signals for the USB, respectively.

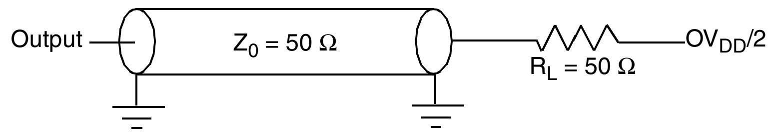

Figure 36. USB AC Test Load

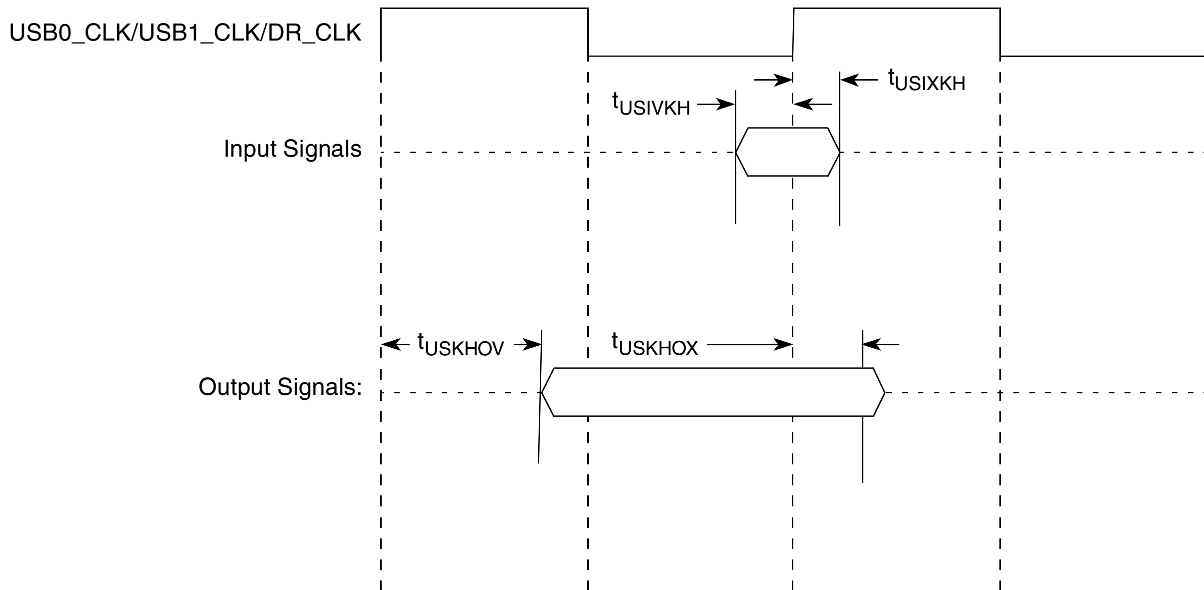

Figure 37. USB Signals

2.12 enhanced Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

2.12.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 48. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	1.9	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN}[1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 49. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN}[1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC) (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V DC.

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	1.9	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.8	—	ns	3

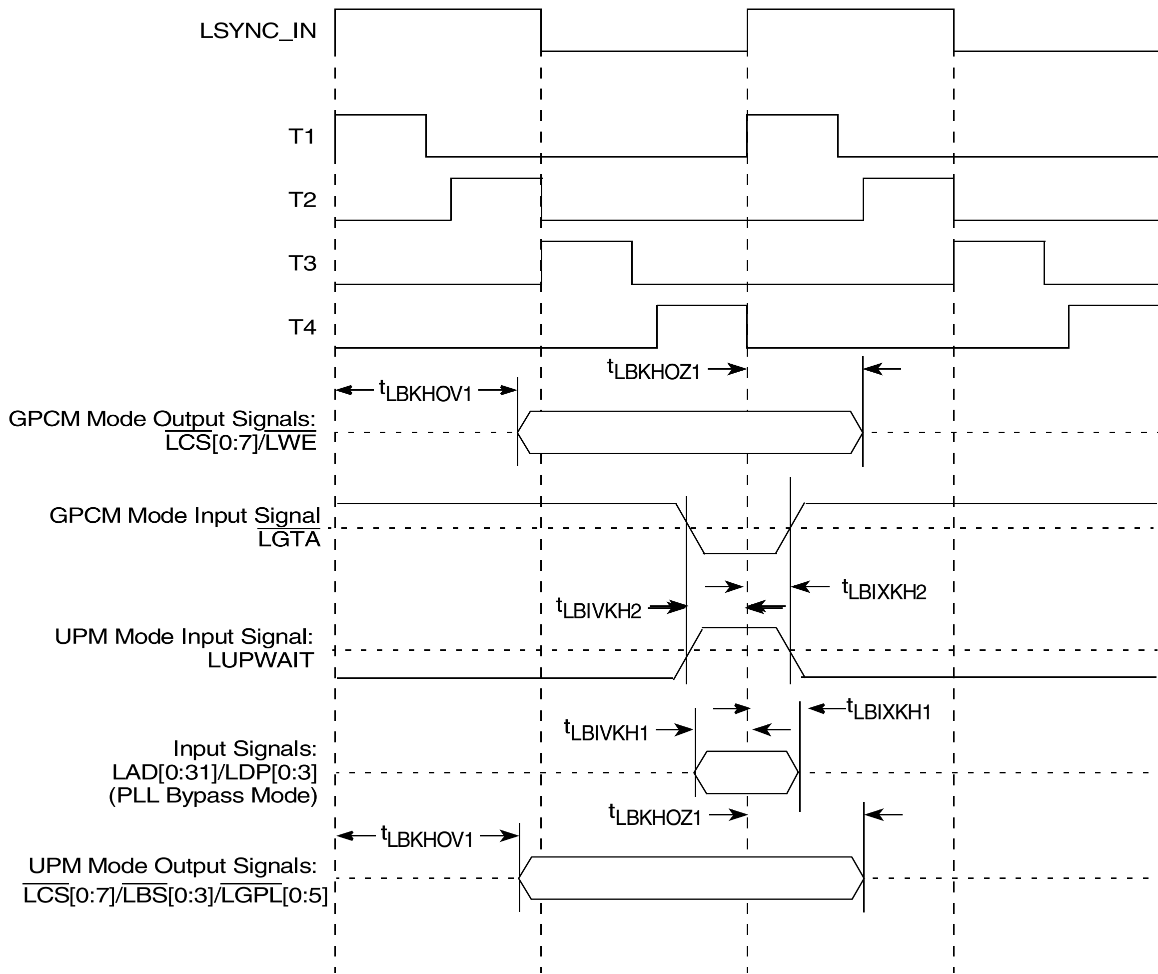

Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 * OVDD	OVDD+0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.25 * OVDD	V	—
Input/Output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—
Output high voltage	V_{OH}	I_{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	—

This figure provides the AC test load for TDO and the boundary-scan outputs.

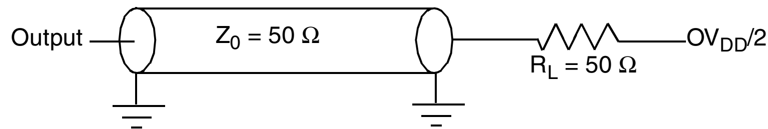

Figure 45. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

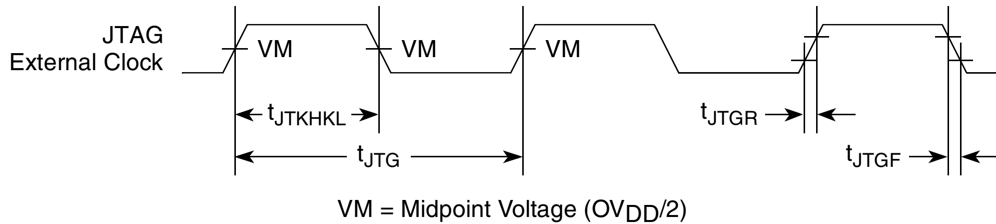

Figure 46. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

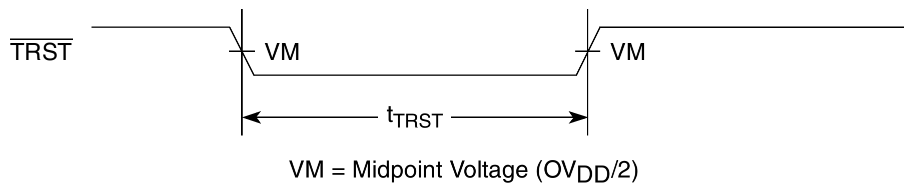

Figure 47. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

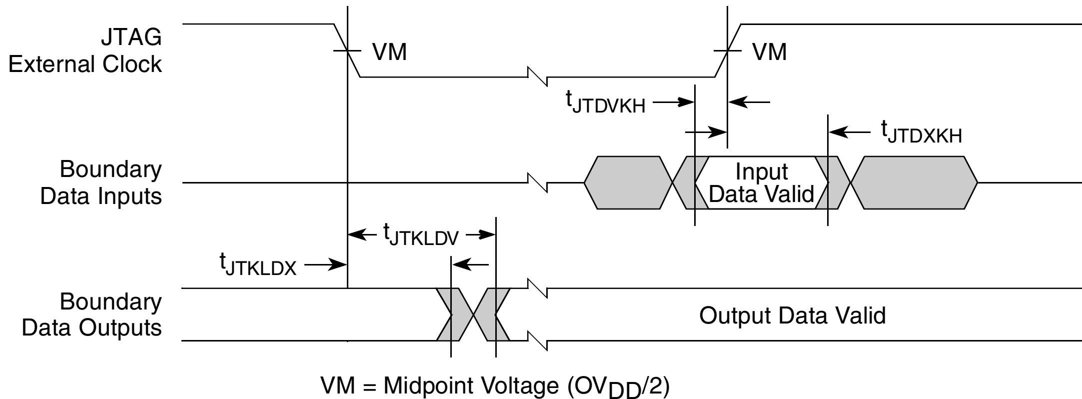

Figure 48. Boundary-Scan Timing Diagram

2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

2.21.1 DC Requirements for PCI Express SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$

For more information, see Section 2.20.2, “SerDes Reference Clocks.”

2.21.2 AC Requirements for PCI Express SerDes Clocks

This table lists AC requirements.

Table 70. SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	1,2,3

Notes:
1. Tj at BER of 10E-6 86 ps Max.
2. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 42 ps.
3. Limits from “PCI Express CEM Rev 2.0” and measured per “PCI Express Rj, D, and Bit Error Rates”.

2.21.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

2.21.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this chip. For further details as well as the specifications of the transport and data link layer, please use the PCI Express Base Specification. REV. 1.0a document.

2.21.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 71. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2.

2.21.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 72. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.175	—	1.200	V	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ See Note 2.
$T_{RX\text{-}EYE}$	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER} = 1 - T_{RX\text{-}EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX\text{-}CM\text{-}ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX\text{-}CM\text{-}ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 + V_{RX\text{-}CM\text{-}DC}$ $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{RX\text{-}D+} + V_{RX\text{-}D-}\rvert/2$ See Note 2
$RL_{RX\text{-}DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and –300 mV, respectively. See Note 4
$RL_{RX\text{-}CM}$	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
$Z_{RX\text{-}DC}$	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX\text{-}DIFFp\text{-}p} < V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$) must be recognized no longer than $T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERING}$ to signal an unexpected idle condition.

2.23.1 Clock Ranges

This table provides the clocking specifications for the processor cores and Table 74 provides the clocking specifications for the memory bus.

Table 73. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	600 MHz		800 MHz		1000 MHz		1250 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	600	600	600	800	600	1000	600	1250	MHz	1, 2
CCB frequency	400	400	400	400	333	400	333	500		
DDR Data Rate	400	400	400	400	400	400	400	500		

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," Section 2.23.3, "e500 Core PLL Ratio,"and Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. This table provides the clocking specifications for the memory bus.

Table 74. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	600, 800, 1000, 1250			
	Min	Max		
DDR Memory bus clock speed	200	250	MHz	1, 2, 3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," Section 2.23.3, "e500 Core PLL Ratio," and Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The Memory bus clock refers to the chip's memory controllers' MCK[0:5] and $\overline{\text{MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 2.23.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, "CCB/SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, "e500 Core PLL Ratio."
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, "DDR/DDRCLK PLL Ratio."

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

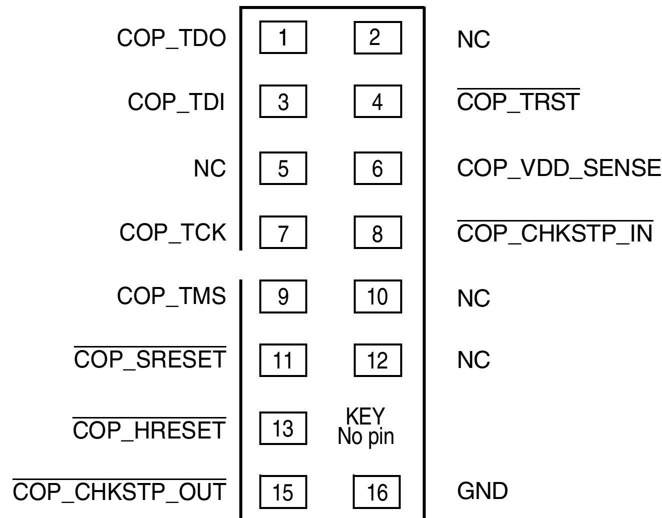

Figure 79. COP Connector Physical Pinout

3.11 Guidelines for High-Speed Interface Termination

3.11.1 SerDes1 Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins. There are several reserved pins that need to be either left floating or connected to XGND. See SerDes1 in Table 1 for details.

The following pins must be left unconnected (float):

- SD1_TX[7:4]
- $\overline{\text{SD1_TX[7:4]}}$
- Reserved pins T22, T23

The following pins must be connected to XGND:

- SD1_RX[7:4]
- $\overline{\text{SD1_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1_REF_CLK}}$

The POR configuration pin cfg_io_ports[0:2] on TSEC3_TXD[6:3] can be used to power down SerDes 1 block for power saving. Note that both SVDD and XVDD must remain powered.

3.11.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:4]
- $\overline{\text{SD1_TX[7:4]}}$
- Reserved pins: T22, T23