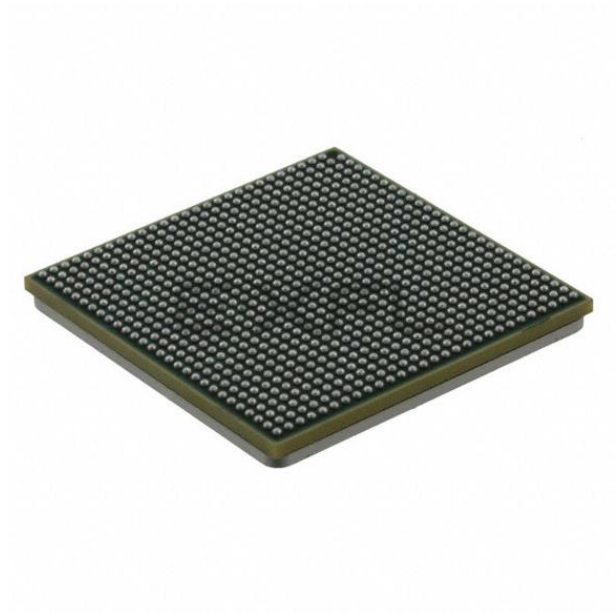

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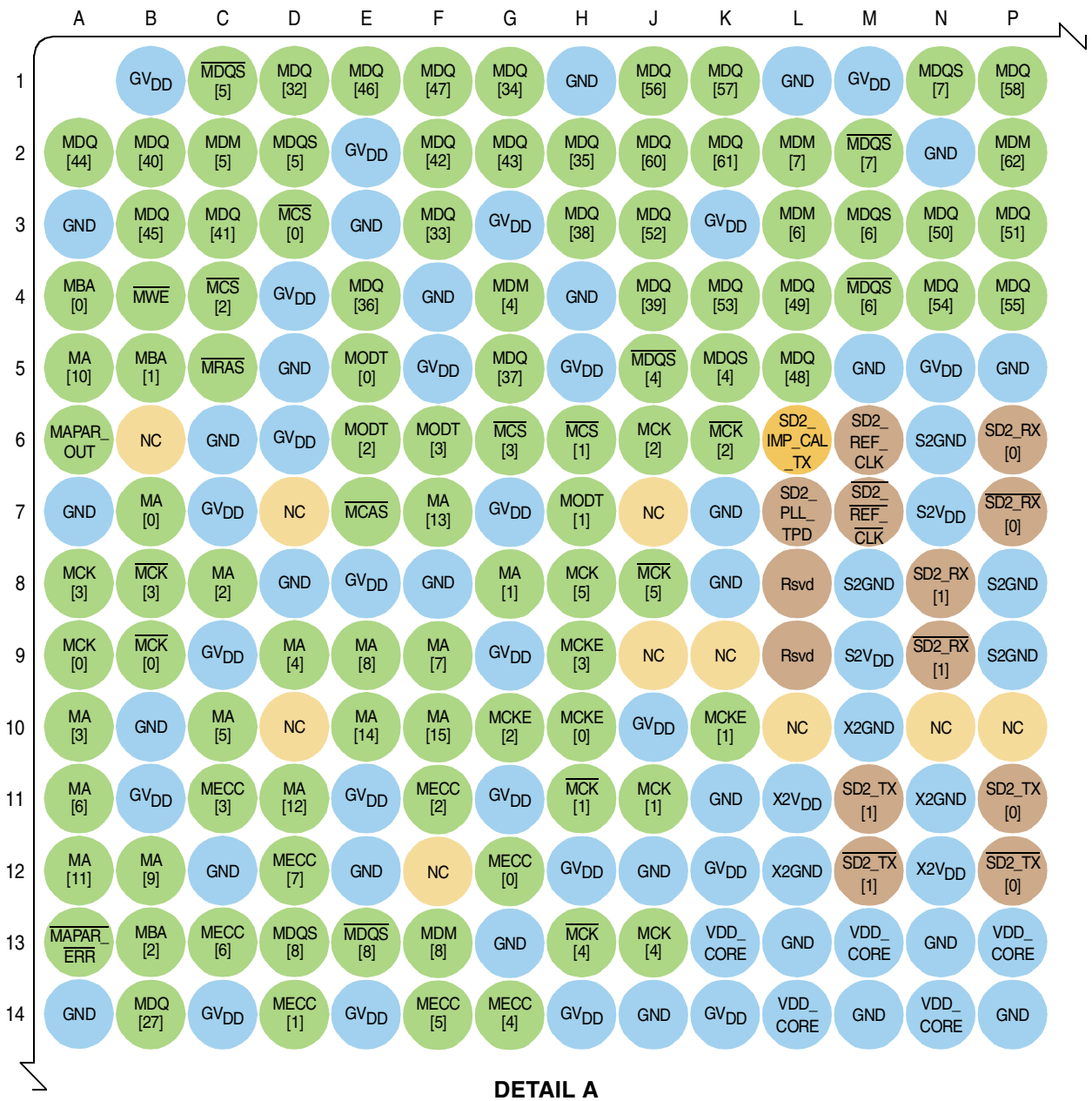
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8535ecvtakga



DETAIL A

Figure 3. Chip Pin Map Detail A

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ[0:63]	Data	A26,B26,C22,D21,D25, B25,D22,E21,A24,A23, B20,A20,A25,B24,B21, A21,E19,D19,E16,C16, F19,F18,F17,D16,B18, A18,A15,B14,B19,A19, A16,B15,D1,F3,G1,H2, E4,G5,H3,J4,B2,C3,F2, G2,A2,B3,E1,F1,L5,L4, N3,P3,J3,K4,N4,P4,J1, K1,P1,R1,J2,K2,P2,R2	I/O	GV_{DD}	—
MECC[0:7]	Error Correcting Code	G12,D14,F11,C11, G14,F14,C13,D12	I/O	GV_{DD}	—
$\overline{\text{MAPAR\_ERR}}$	Address Parity Error	A13	I	GV_{DD}	—
MAPAR_OUT	Address Parity Out	A6	O	GV_{DD}	—
MDM[0:8]	Data Mask	C25,B23,D18,B17,G4, C2,L3,L2,F13	O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	Data Strobe	D24,B22,C18,A17,J5, C1,M4,M2,E13	I/O	GV_{DD}	—
MDQS[0:8]	Data Strobe	C23,A22,E17,B16,K5, D2,M3,N1,D13	I/O	GV_{DD}	—
MA[0:15]	Address	B7,G8,C8,A10,D9,C10, A11,F9,E9,B12,A5, A12,D11,F7,E10,F10	O	GV_{DD}	—
MBA[0:2]	Bank Select	A4,B5,B13	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	B4	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	C5	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	E7	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	Chip Select	D3,H6,C4,G6	O	GV_{DD}	—
MCKE[0:3]	Clock Enable	H10,K10,G10,H9	O	GV_{DD}	11
MCK[0:5]	Differential Clock 3 Pairs / DIMM	A9,J11,J6,A8,J13,H8	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	Differential Clock 3 Pairs / DIMM	B9,H11,K6,B8,H13,J8	O	GV_{DD}	—
MODT[0:3]	On Die Termination	E5,H7,E6,F6	O	GV_{DD}	—
MDIC[0:1]	Calibration	H15,K15	I/O	GV_{DD}	26
Local Bus Controller Interface					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	Muxed data / address	K22,L21,L22,K23,K24, L24,L25,K25,L28,L27, K28,K27,J28,H28,H27, G27,G26,F28,F26,F25, E28,E27,E26,F24,E24, C26,G24,E23,G23,F22, G22,G21	I/O	BV_{DD}	5,9,29
LDP[0:3]	Data parity	K26,G28,B27,E25	I/O	BV_{DD}	29
LA[27]	Burst address	L19	O	BV_{DD}	5,9,29
LA[28:31]	Port address	K16,K17,H17,G17	O	BV_{DD}	5,7,9,29
$\overline{\text{LCS}}$[0:4]	Chip selects	K18,G19,H19,H20,G16	O	BV_{DD}	29
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	Chips selects / DMA Request	H16	I/O	BV_{DD}	1,29
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	Chips selects / DMA Ack	J16	O	BV_{DD}	1,29
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	Chips selects / DMA Done	L18	O	BV_{DD}	1,29
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$	Write enable / Byte select	J22	O	BV_{DD}	5,9,29
$\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$	Write enable / Byte select	H22,H23,H21	O	BV_{DD}	5,9,29
LBCTL	Buffer control	J25	O	BV_{DD}	5,8,9,29
LALE	Address latch enable	J26	O	BV_{DD}	5,8,9,29
LGPL0/LFCLE	UPM general purpose line 0 / FLash command latch enable	J20	O	BV_{DD}	5,9,29
LGPL1/LFALE	UPM general purpose line 1 / Flash address latch enable	K20	O	BV_{DD}	5,9,29
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM general purpose line 2 / Output enable/Flash read enable	G20	O	BV_{DD}	5,8,9,29
LGPL3/$\overline{\text{LFWP}}$	UPM general purpose line 3 / Flash write protect	H18	O	BV_{DD}	5,9,29
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT /LPBSE/LFRB	UPM general purpose line 4 / Target Ack/Wait/SDRAM parity byte select/Flash Ready-busy	L20	I/O	BV_{DD}	29, 35
LGPL5	UPM general purpose line 5 / Amux	K19	O	BV_{DD}	5,9,29
LCLK[0:2]	Local bus clock	H24,J24,H25	O	BV_{DD}	29
LSYNC_IN	Synchronization	D27	I	BV_{DD}	29
LSYNC_OUT	Local bus DLL	D28	O	BV_{DD}	29
DMA					
$\overline{\text{DMA\_DACK}}$[0:1] /GPIO[10:11]	DMA Acknowledge	AD6,AE10	O	OV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Programmable Interrupt Controller					
$\overline{\text{MCP}}$	Machine check processor	Y14	I	OV_{DD}	—
$\overline{\text{UDE}}$	Unconditional debug event	AB14	I	OV_{DD}	—
IRQ[0:8]	External interrupts	AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ[3]}}$	External interrupt/DMA request	AE13	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK[3]}}$	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE[3]}}$	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	Interrupt output	AC17	O	OV_{DD}	2,4
Ethernet Management Interface					
EC_MDC	Management data clock	Y10	O	OV_{DD}	5,9,22
EC_MDIO	Management data In/Out	Y11	I/O	OV_{DD}	—
Gigabit Reference Clock					
EC_GTX_CLK125	Reference clock	AA6	I	LV_{DD}	31
Three-Speed Ethernet Controller (Gigabit Ethernet 1)					
TSEC1_TXD[7:0]	Transmit data	AA8,AA5,Y8,Y5,W3, W5,W4,W6	O	LV_{DD}	5,9,22
TSEC1_TX_EN	Transmit Enable	W1	O	LV_{DD}	23
TSEC1_TX_ER	Transmit Error	AB5	O	LV_{DD}	5,9
TSEC1_TX_CLK	Transmit clock In	AB4	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit clock Out	W2	O	LV_{DD}	—
TSEC1_CRS	Carrier sense	AA9	I/O	LV_{DD}	17
TSEC1_COL	Collision detect	AB6	I	LV_{DD}	—
TSEC1_RXD[7:0]	Receive data	AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2	I	LV_{DD}	—
TSEC1_RX_DV	Receive data valid	AA1	I	LV_{DD}	—
TSEC1_RX_ER	Receive data error	Y9	I	LV_{DD}	—
TSEC1_RX_CLK	Receive clock	AA3	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)					
TSEC3_TXD[7:0]	Transmit data	T12,V8,U8,V9,T8,T7, T5,T6	O	TV_{DD}	5,9,22
TSEC3_TX_EN	Transmit Enable	V5	O	TV_{DD}	23
TSEC3_TX_ER	Transmit Error	U9	O	TV_{DD}	5,9

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
UART_SOUT[0:1]	Transmit data	AF10,AA12	O	OV_{DD}	5,9,22, 10,29
I^2C interface					
IIC1_SCL	Serial clock	AG21	I/O	OV_{DD}	4,21,29
IIC1_SDA	Serial data	AH22	I/O	OV_{DD}	4,21,29
IIC2_SCL	Serial clock	AH15	I/O	OV_{DD}	4,21,29
IIC2_SDA	Serial data	AG14	I/O	OV_{DD}	4,21,29
SerDes1(x4)					
SD1_TX[7:4]	Transmit Data (+)	Y23,W21,V23,U21	O	XV_{DD}	—
$\overline{\text{SD1\_TX}}$[7:4]	Transmit Data(-)	Y22,W20,V22,U20	O	XV_{DD}	—
SD1_RX[7:4]	Receive Data(+)	AC28,AB26,AA28,Y26	I	XV_{DD}	—
$\overline{\text{SD1\_RX}}$[7:4]	Receive Data(–)	AC27,AB25,AA27,Y25	I	XV_{DD}	—
Reserved	—	R21,P23,N21,M23, R20,P22,N20,M22	—	—	18
Reserved	—	T26,R28,P26,N28, T25,R27,P25,N27	—	—	33
SD1_PLL_TPD	PLL test point Digital	V28	O	XV_{DD}	18
SD1_REF_CLK	PLL Reference clock	U28	I	XV_{DD}	—
$\overline{\text{SD1\_REF\_CLK}}$	PLL Reference clock complement	U27	I	XV_{DD}	—
Reserved	—	T22	—	—	18
Reserved	—	T23	—	—	18
SerDes2(x1)					
SD2_TX[0]	Transmit data(+)	P11	O	$X2V_{DD}$	—
$\overline{\text{SD2\_TX[0]}}$	Transmit data(-)	P12	O	$X2V_{DD}$	—
SD2_RX[0]	Receive data(+)	P6	I	$X2V_{DD}$	—
$\overline{\text{SD2\_RX[0]}}$	Receive data(-)	P7	I	$X2V_{DD}$	—
Reserved	—	M11,M12	—	—	18
Reserved	—	N8, N9	—	—	34
SD2_PLL_TPD	PLL test point Digital	L7	O	$X2V_{DD}$	18
SD2_REF_CLK	PLL Reference clock	M6	I	$X2V_{DD}$	—
$\overline{\text{SD2\_REF\_CLK}}$	PLL Reference clock complement	M7	I	$X2V_{DD}$	—
Reserved	—	L8	—	$X2V_{DD}$	18
Reserved	—	L9	—	$X2V_{DD}$	18

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
General-Purpose Input/Output					
GPIO[0:1]/PCI1_REQ[3:4]	GPIO/PCI request	Y15,AE15	I/O	OV_{DD}	—
GPIO[2:3]/PCI1_GNT[3:4]	GPIO/PCI grant	AA15,AC14	I/O	OV_{DD}	—
GPIO[4]/SDHC_CD	GPIO/SDHC card detection	AH11	I/O	OV_{DD}	—
GPIO[5]/SDHC_WP	GPIO/SDHC write protection	AG10	I/O	OV_{DD}	32
GPIO[6]/USB1_PCTL0	GPIO/USB1 PCTL0	AC3	I/O	OV_{DD}	—
GPIO[7]/USB1_PCTL1	GPIO/USB1 PCTL1	AC4	I/O	OV_{DD}	—
GPIO[8]/USB2_PCTL0	GPIO/USB2 PCTL0	AG9	I/O	OV_{DD}	—
GPIO[9]/USB2_PCTL1	GPIO/USB2 PCTL1	AC9	I/O	OV_{DD}	—
GPIO[10:11] /DMA_DACK[0:1]	GPIO/DMA Ack	AD6,AE10	I/O	OV_{DD}	—
GPIO[12:13] /DMA_DDONE[0:1]	GPIO/DMA done	AA11,AB11	I/O	OV_{DD}	—
GPIO[14:15] /DMA_DREQ[0:1]	GPIO/DMA request	AB10,AD11	I/O	OV_{DD}	—
System Control					
HRESET	Hard reset	AG16	I	OV_{DD}	—
HRESET_REQ	Hard reset - request	AG15	O	OV_{DD}	22
SRESET	Soft reset	AG19	I	OV_{DD}	—
CKSTP_IN	CheckStop in	AG18	I	OV_{DD}	—
CKSTP_OUT	CheckStop Output	AH17	O	OV_{DD}	2,4
Debug					
TRIG_IN	Trigger in	W19	I	OV_{DD}	—
TRIG_OUT/READY /QUIESCE	Trigger out/Ready/Quiesce	V19	O	OV_{DD}	22
MSRCID[0:1]	Memory debug source port ID	W12,W13	O	OV_{DD}	6,9
MSRCID[2:4]	Memory debug source port ID	V12, W14,W11	O	OV_{DD}	6,9,22
MDVAL	Memory debug data valid	V13	O	OV_{DD}	6,22
CLK_OUT	Clock Out	W15	O	OV_{DD}	11
Clock					
RTC	Real time clock	AF15	I	OV_{DD}	—
SYSCLK	System clock / PCI clock	AH14	I	OV_{DD}	—
DDRCLK	DDR clock	AC13	I	OV_{DD}	30
JTAG					

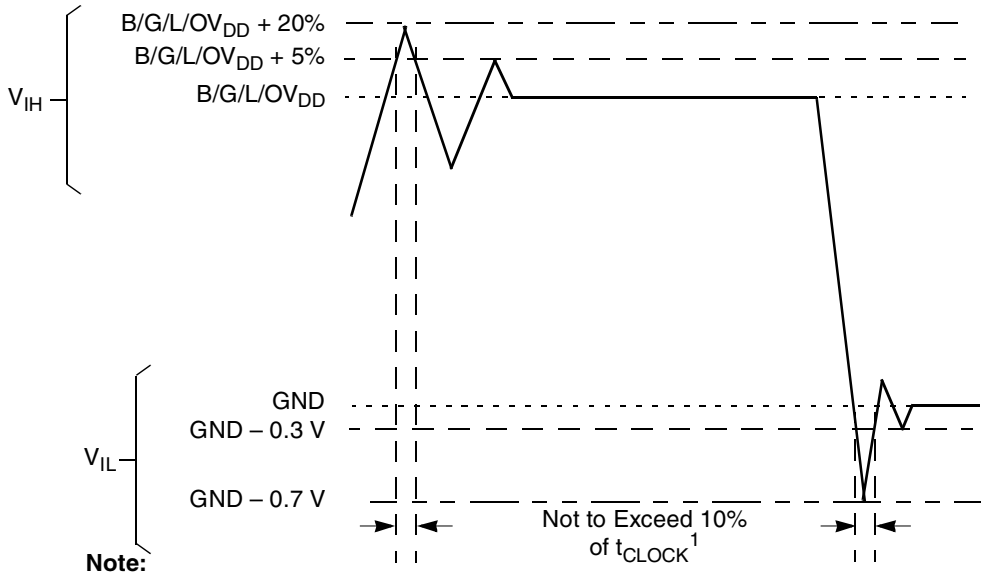
Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	1.0 ± 50 mV	V	—
Platform supply voltage		V_{DD_PLAT}	1.0 ± 50 mV	V	—
PLL core supply voltage		AV_{DD_CORE}	1.0 ± 50 mV	V	2
PLL other supply voltage		AV_{DD}	1.0 ± 50 mV	V	2
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}	1.0 ± 50 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V ± 90 mV	V	3
	DDR3 SDRAM Interface		1.5 V ± 75 mV		
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	5
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	3.3 V ± 165 mV	V	4
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 and DDR3 SDRAM Interface reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	5
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	4
Operating Temperature range	Commercial	T_A T_J	T_A= 0 (min) to T_J= 90(max)	°C	6
	Industrial standard temperature range		T_A= 0 (min) to T_J= 105 (max)		
	Extended temperature range		T_A= -40 (min) to T_J= 105 (max)		

Notes:

2. This voltage is the input to the filter discussed in Section 3.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
3. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For eLBC, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI1_CLK or SYSCLK.

2. With the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 7. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The core voltage must always be provided at nominal 1.0 V . (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

Table 5. Power Dissipation (continued)[5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	1250	500	500	1.0	1.0	105 / 90	—	5.3/4.4	—	5.0/4.0	1, 3, 8
Thermal (W)							—	4.4/3.6	—	5.0/4.0	1, 4, 8
Typical (W)						65	2.2		1.7		1
Doze (W)							1.6	2.4	1.5	2.1	1
Nap (W)							0.8	1.6	1.5	2.1	1
Sleep (W)							0.8	1.6	1.1	1.7	1
Deep Sleep (W)						35	0	0	0.6	1.2	1, 6

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 ^{0}C, for Industrial Tier is 105 ^{0}C.
9. Platform power is the power supplied to all the V_{DD_PLAT} pins.

See Section 2.23.6.1, "SYSCLK to Platform Frequency Options," for the full range of CCB frequencies that the chip supports.

Table 21. SPI AC Timing Specifications[1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_CS outputs—Master data delay	$t_{NIKHOV2}$	—	6.0	ns	—
SPI inputs—Master data input setup time	t_{NIIVKH}	5	—	ns	—
SPI inputs—Master data input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. SPCOM[RxDelay] is set to 0.
4. SPCOM[RxDelay] is set to 1.

This figure provides the AC test load for the SPI.

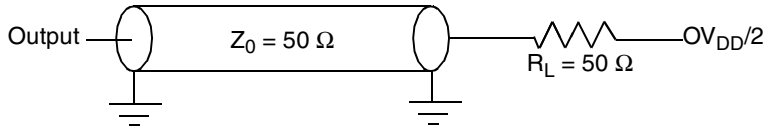
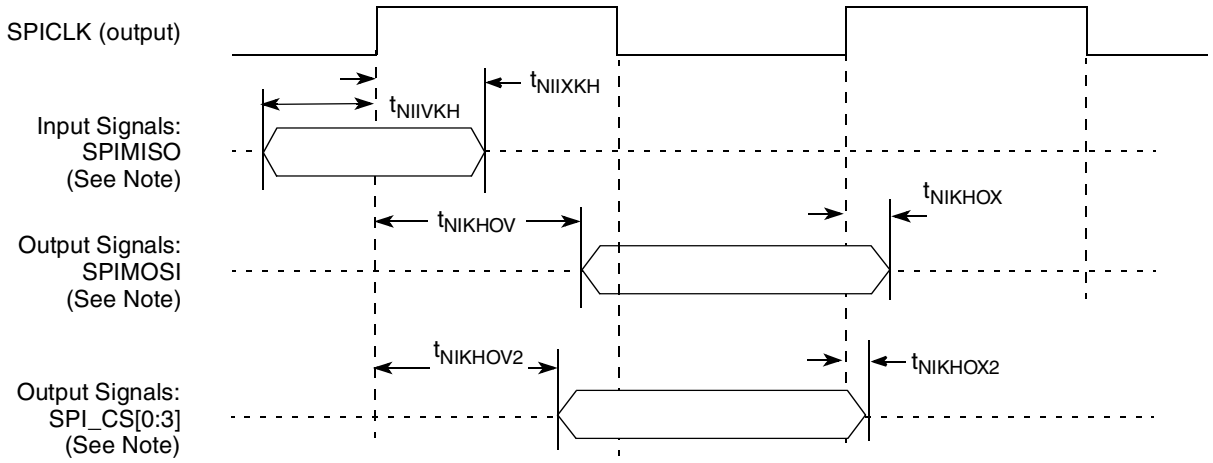


Figure 12. SPI AC Test Load

This figure represents the AC timing from Table 21. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on SPI.

Figure 13. SPI AC Timing in Master mode (Internal Clock) Diagram

Table 36. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

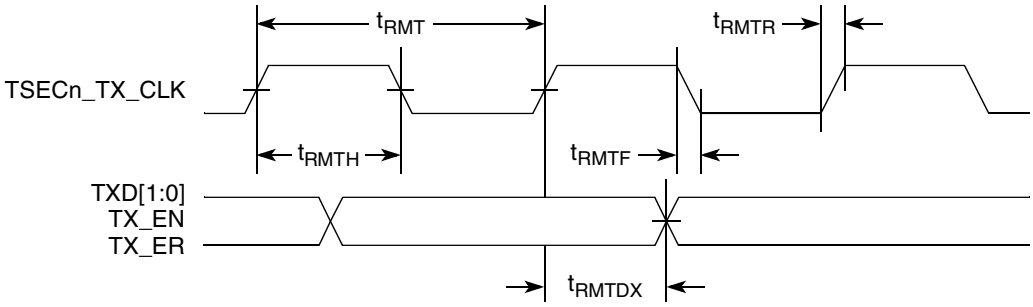


Figure 26. RMII Transmit AC Timing Diagram

2.9.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_RX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_RX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns

The IEEE 1588 AC timing specifications are in the following table.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	T_{TX_CLK}*7	ns	1
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2*$t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. When TMR_CTRL[CKSEL]=00, the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in the Table above. The maximum value of $t_{T1588CLK}$ is defined in terms of T_{TX_CLK}, which is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running.
   When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.
   See the *MPC8536E PowerQUICC III Integrated Communications Processor Reference Manual* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

2.10 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals EC_MDIO (management data input/output) and EC_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in Section 2.9, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management”

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC) (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	—	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	—	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	—	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 53. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.9	—	ns	3

Table 54. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	0.5	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	0.5	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.5	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	—	2.2	ns	4,8
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	—	2.2	ns	4,8
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.1	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.1	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. These timing parameters for PLL bypass mode are defined in the opposite direction of the PLL enabled output hold timing parameters.

Table 68. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Failing time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 22, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.

This figure provides the AC test load for PCI.

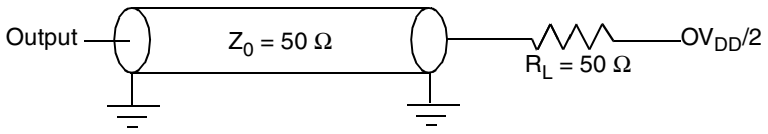


Figure 54. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

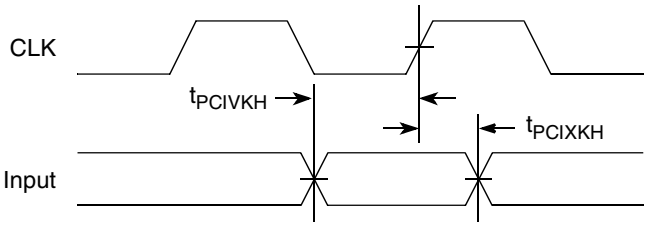


Figure 55. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

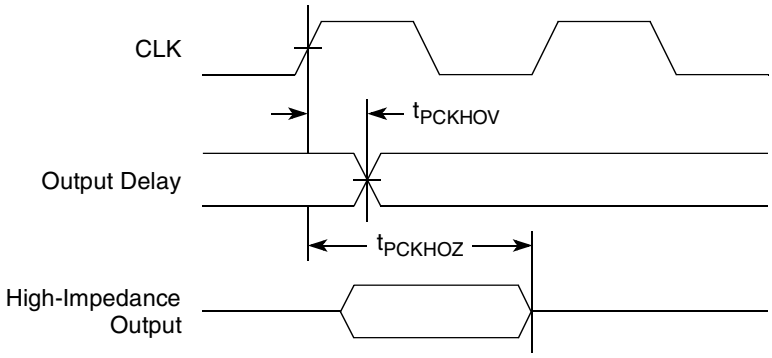


Figure 56. PCI Output AC Timing Measurement Condition

2.20 High-Speed Serial Interfaces

This chip features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for SGMII or SATA.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 57 shows how the signals are defined. For illustration purposes, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn\_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn\_TX}}$, SDn_RX and $\overline{\text{SDn\_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: V_{SDn_TX} - $V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: V_{SDn_RX} - $V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A - B| Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential

2.23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in the following table:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 75. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	Reserved	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

2.23.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in this table.

Table 76. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

2.23.4 DDR/DDRCLK PLL Ratio

The DDR memory controller complex can be synchronous with, or asynchronous to, the CCB, depending on configuration.

The following table describes the clock ratio between the DDR memory controller complex and the DDR/DDRCLK PLL reference clock, DDRCLK, which is not the memory bus clock.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for the DDR controller to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 77 reflects the DDR data rate to DDRCLK ratio, since the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Table 77. DDR Clock Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	cfg_ddr_pll[0:2]	000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

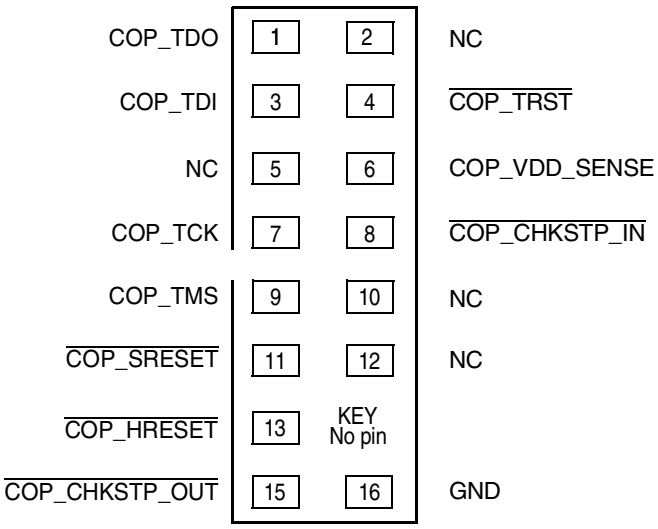


Figure 79. COP Connector Physical Pinout

3.11 Guidelines for High-Speed Interface Termination

3.11.1 SerDes1 Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins. There are several reserved pins that need to be either left floating or connected to XGND. See SerDes1 in Table 1 for details.

The following pins must be left unconnected (float):

- SD1_TX[7:4]
- $\overline{\text{SD1\_TX[7:4]}}$
- Reserved pins T22, T23

The following pins must be connected to XGND:

- SD1_RX[7:4]
- $\overline{\text{SD1\_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

The POR configuration pin cfg_io_ports[0:2] on TSEC3_TXD[6:3] can be used to power down SerDes 1 block for power saving. Note that both SVDD and XVDD must remain powered.

3.11.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:4]
- $\overline{\text{SD1\_TX[7:4]}}$
- Reserved pins: T22, T23

4.1 Part Numbers Fully Addressed by this Document

This table shows the part numbering nomenclature.

Table 82. Part Numbering Nomenclature

MPC	*nnnn*	*E*	*C*	*VT*	*AA*	*X*	*R*
Product Code	**Part Identifier**	**Security Engine**	**Tiers and Temperature Range**	**Package [1]**	**Processor Frequency [2]**	**DDR Frequency [3]**	**Revision Level**
MPC	8536 8535	E = included	• A = Commercial tier standard temperature range (0° to 90°C) • B or Blank = industrial tier standard temperature range (0° to 105°C) • C = Industrial tier extended temperature range (–40° to 105°C)	• VT = FC-PBGA • (Pb-free) • PX = plastic standard	• AK = 600 MHz • AN = 800 MHz • AQ = 1000 MHz • AT = 1250 MHz • AU = 1333 MHz • AV = 1500 MHz	• G = 400 MHz • H = 500 MHz • J = 533 MHz • L = 667 MHz	• Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0190, 0x803F0191) • A = Ver. 1.2 (SVR = 0x803F0192)
		Blank = not included					• Blank = Ver. 1.0 or 1.1 (SVR = 0x80370190, 0x80370191) • A = Ver. 1.2 (SVR = 0x80370192)

Notes:

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.