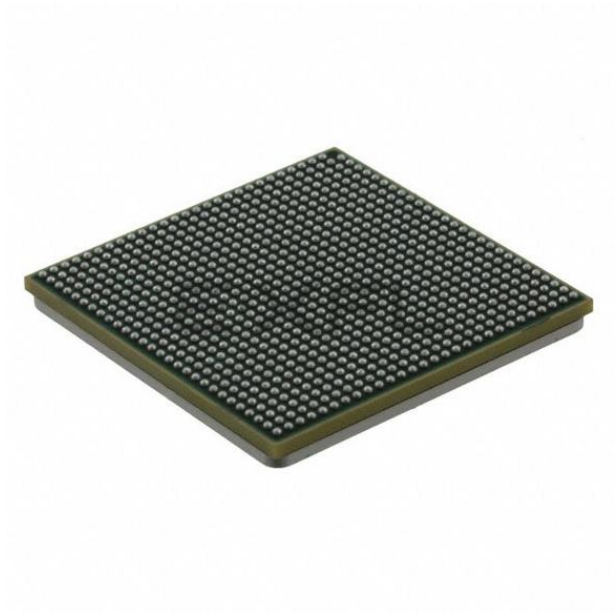

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | SATA 3Gbps (1) |
| USB | USB 2.0 (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535ecvtaqga |

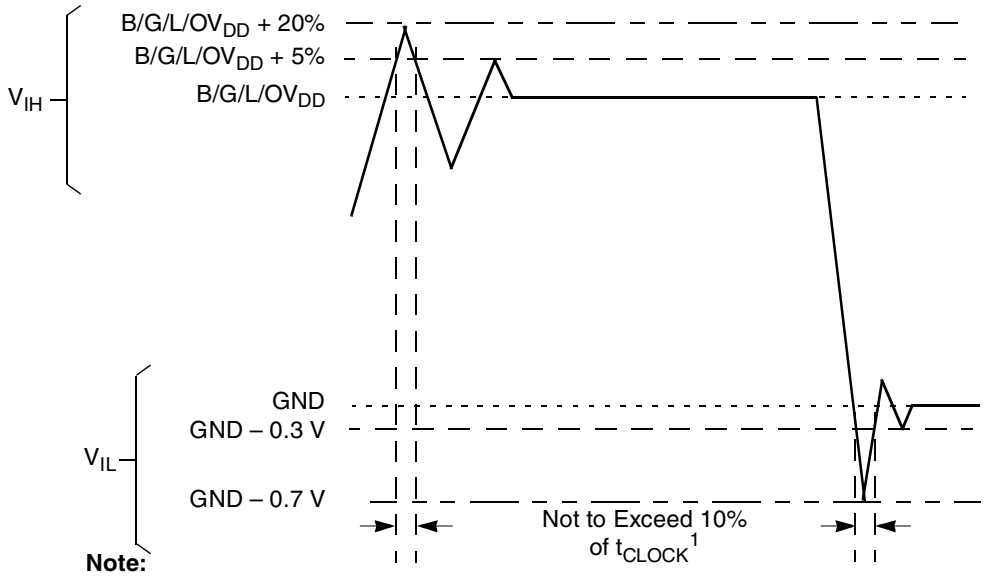
**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| LAD[0:31] | Muxed data / address | K22,L21,L22,K23,K24, L24,L25,K25,L28,L27, K28,K27,J28,H28,H27, G27,G26,F28,F26,F25, E28,E27,E26,F24,E24, C26,G24,E23,G23,F22, G22,G21 | I/O | $BV_{DD}$ | 5,9,29 |
| LDP[0:3] | Data parity | K26,G28,B27,E25 | I/O | $BV_{DD}$ | 29 |
| LA[27] | Burst address | L19 | O | $BV_{DD}$ | 5,9,29 |
| LA[28:31] | Port address | K16,K17,H17,G17 | O | $BV_{DD}$ | 5,7,9,29 |
| $\overline{\text{LCS}}$[0:4] | Chip selects | K18,G19,H19,H20,G16 | O | $BV_{DD}$ | 29 |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$ | Chips selects / DMA Request | H16 | I/O | $BV_{DD}$ | 1,29 |
| $\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$ | Chips selects / DMA Ack | J16 | O | $BV_{DD}$ | 1,29 |
| $\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$ | Chips selects / DMA Done | L18 | O | $BV_{DD}$ | 1,29 |
| $\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$ | Write enable / Byte select | J22 | O | $BV_{DD}$ | 5,9,29 |
| $\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$ | Write enable / Byte select | H22,H23,H21 | O | $BV_{DD}$ | 5,9,29 |
| LBCTL | Buffer control | J25 | O | $BV_{DD}$ | 5,8,9,29 |
| LALE | Address latch enable | J26 | O | $BV_{DD}$ | 5,8,9,29 |
| LGPL0/LFCLE | UPM general purpose line 0 / FLash command latch enable | J20 | O | $BV_{DD}$ | 5,9,29 |
| LGPL1/LFALE | UPM general purpose line 1 / Flash address latch enable | K20 | O | $BV_{DD}$ | 5,9,29 |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | UPM general purpose line 2 / Output enable/Flash read enable | G20 | O | $BV_{DD}$ | 5,8,9,29 |
| LGPL3/$\overline{\text{LFWP}}$ | UPM general purpose line 3 / Flash write protect | H18 | O | $BV_{DD}$ | 5,9,29 |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT /LPBSE/LFRB | UPM general purpose line 4 / Target Ack/Wait/SDRAM parity byte select/Flash Ready-busy | L20 | I/O | $BV_{DD}$ | 29, 35 |
| LGPL5 | UPM general purpose line 5 / Amux | K19 | O | $BV_{DD}$ | 5,9,29 |
| LCLK[0:2] | Local bus clock | H24,J24,H25 | O | $BV_{DD}$ | 29 |
| LSYNC_IN | Synchronization | D27 | I | $BV_{DD}$ | 29 |
| LSYNC_OUT | Local bus DLL | D28 | O | $BV_{DD}$ | 29 |
| DMA | | | | | |
| $\overline{\text{DMA\_DACK}}$[0:1] /GPIO[10:11] | DMA Acknowledge | AD6,AE10 | O | $OV_{DD}$ | — |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SGND | SerDes 1 Transceiver core logic GND (xcorevss) | M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28 | — | — | — |
| X2GND | SerDes 2 Transceiver pad GND (xpadvss) | R12,M10,N11,L12 | — | — | — |
| S2GND | SerDes 2 Transceiver core logic GND (xcorevss) | P8,P9,N6,M8 | — | — | — |
| AGND_SRDS | SerDes 1 PLL GND | V27 | — | — | — |
| AGND_SRDS2 | SerDes 2 PLL GND | T2 | — | — | — |
| SENSEVSS | GND Sensing | V16 | — | — | 13 |
| **Analog Signals** | | | | | |
| MVREF | SSTL2 reference voltage | A28 | Reference voltage for DDR | GVDD/2 | — |
| SD1_IMP_CAL_RX | Rx impedance calibration | M26 | — | 200Ω (±1%) to GND | — |
| SD1_IMP_CAL_TX | Tx impedance calibration | AE28 | — | 100Ω (±1%) to GND | — |
| SD1_PLL_TPA | PLL test point analog | V26 | — | AVDD_SRDS analog | 18 |
| SD2_IMP_CAL_RX | Rx impedance calibration | R7 | — | 200Ω (±1%) to GND | — |
| SD2_IMP_CAL_TX | Tx impedance calibration | L6 | — | 100Ω (±1%) to GND | — |
| SD2_PLL_TPA | PLL test point analog | T3 | — | AVDD_SRDS2 analog | 18 |
| Reserved | — | R4 | — | — | — |
| Reserved | — | R5 | — | — | — |
| **No Connect Pins** | | | | | |
| NC | — | C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9 | — | — | — |

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.




**Note:**

1. $t_{CLOCK}$ refers to the clock period associated with the respective interface:
   For $I^2C$ and JTAG, $t_{CLOCK}$ references SYSCLK.
   For DDR, $t_{CLOCK}$ references MCLK.
   For eTSEC, $t_{CLOCK}$ references EC_GTX_CLK125.
   For eLBC, $t_{CLOCK}$ references LCLK.
   For PCI, $t_{CLOCK}$ references PCI1_CLK or SYSCLK.

2. With the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

**Figure 7. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$**

The core voltage must always be provided at nominal 1.0 V . (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $OV_{DD}$ and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

**Table 5. Power Dissipation (continued)[5]**

| Power Mode | Core Frequency | CCB Frequency | DDR Frequency | $V_{DD}$ Platform | $V_{DD}$ Core | Junction Temperature | Core Power | | Platform Power[9] | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | (MHz) | (MHz) | (MHz) | (V) | (V) | (°C) | mean[7] | Max | mean[7] | Max | |
| Maximum (A) | 1250 | 500 | 500 | 1.0 | 1.0 | 105 / 90 | — | 5.3/4.4 | — | 5.0/4.0 | 1, 3, 8 |
| Thermal (W) | | | | | | | — | 4.4/3.6 | — | 5.0/4.0 | 1, 4, 8 |
| Typical (W) | | | | | | 65 | 2.2 | | 1.7 | | 1 |
| Doze (W) | | | | | | | 1.6 | 2.4 | 1.5 | 2.1 | 1 |
| Nap (W) | | | | | | | 0.8 | 1.6 | 1.5 | 2.1 | 1 |
| Sleep (W) | | | | | | | 0.8 | 1.6 | 1.1 | 1.7 | 1 |
| Deep Sleep (W) | | | | | | 35 | 0 | 0 | 0.6 | 1.2 | 1, 6 |

**Notes:**

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage ($V_{DD}$) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage ($V_{DD}$) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage ($V_{DD}$) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 $^0$C, for Industrial Tier is 105 $^0$C.
9. Platform power is the power supplied to all the $V_{DD\_PLAT}$ pins.

See Section 2.23.6.1, "SYSCLK to Platform Frequency Options," for the full range of CCB frequencies that the chip supports.

**Table 25. RGMII, RTBI, and FIFO DC Electrical Characteristics**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}/TV_{DD}$ | 2.37 | 2.63 | V | 1,2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –1.0 mA) | $V_{OH}$ | 2.00 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.70 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | µA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | µA | 3 |

**Note:**

1 $LV_{DD}$ supports eTSECs 1.

2 $TV_{DD}$ supports eTSECs 3.

3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1 and Table 2.

## 2.9.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

### 2.9.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 2.4.6, "Platform to FIFO Restrictions."

A summary of the FIFO AC specifications appears in the following tables.

**Table 26. FIFO Mode Transmit AC Timing Specification**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period[2] | $t_{FIT}$ | 6.0 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |

**Table 45. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with OVDD is 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_MDIO to EC_MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| EC_MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |
| EC_MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency ($f_{CCB}$). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC}$ = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency ($f_{CCB}$), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. $t_{CLKplb\_clk}$ is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid $t_{MDKHDV}$ is a function of clock period and max delay time $t_{MDKHDX}$. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

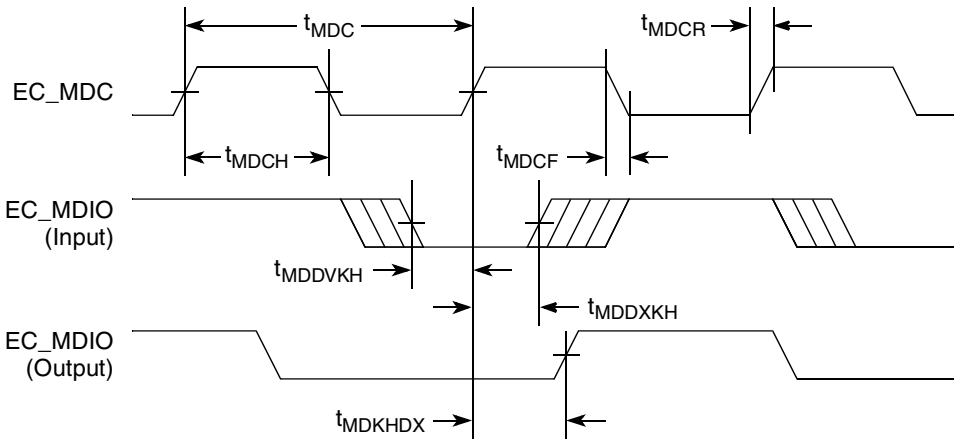



**Figure 35. MII Management Interface Timing Diagram**

## 2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 50. Local Bus DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage 1.8V | $BV_{DD}$ | — | 1.71 | 1.89 | V |
| High-level input voltage | $V_{IH}$ | — | 0.65*$BV_{DD}$ | 0.3+$BV_{DD}$ | V |
| Low-level input voltage | $V_{IL}$ | — | –0.3 | 0.35*$BV_{DD}$ | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | -15 | 10 | μA |
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = –100 μA | $BV_{DD}$ – 0.2 | — | V |
| | | $I_{OH}$ = –2 mA | $BV_{DD}$ – 0.45 | — | |
| Low-level output voltage | $V_{OL}$ | $I_{OH}$ = 100 μA | — | 0.2 | V |
| | | $I_{OH}$ = 2 mA | — | 0.45 | |

**Note:**

1. Note that the symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 2.12.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 3.3 V DC. For information about the frequency range of local bus see Section 2.23.1, “Clock Ranges.”

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.4 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.3 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.7 | — | ns | 3 |

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC) (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.7 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.5 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.5 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 2.5 V DC.

**Table 52. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | — | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | — | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 1.9 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.8 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | — | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | — | $t_{LBKHOV1}$ | — | 2.4 | ns | — |
| Local bus clock to data valid for LAD/LDP | — | $t_{LBKHOV2}$ | — | 2.5 | ns | 3 |
| Local bus clock to address valid for LAD | — | $t_{LBKHOV3}$ | — | 2.4 | ns | 3 |
| Local bus clock to LALE assertion | — | $t_{LBKHOV4}$ | — | 2.4 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | — | $t_{LBKHOX1}$ | 0.8 | — | ns | 3 |

**Table 52. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC) (continued)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | — | $t_{LBKHOX2}$ | 0.8 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | — | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | — | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 1.8 V DC.

**Table 53. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | — | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 2.4 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.9 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | — | $t_{LBOTOT}$ | 1.2 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | — | $t_{LBKHOV1}$ | — | 3.2 | ns | — |
| Local bus clock to data valid for LAD/LDP | — | $t_{LBKHOV2}$ | — | 3.2 | ns | 3 |
| Local bus clock to address valid for LAD | — | $t_{LBKHOV3}$ | — | 3.2 | ns | 3 |
| Local bus clock to LALE assertion | — | $t_{LBKHOV4}$ | — | 3.2 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | — | $t_{LBKHOX1}$ | 0.9 | — | ns | 3 |

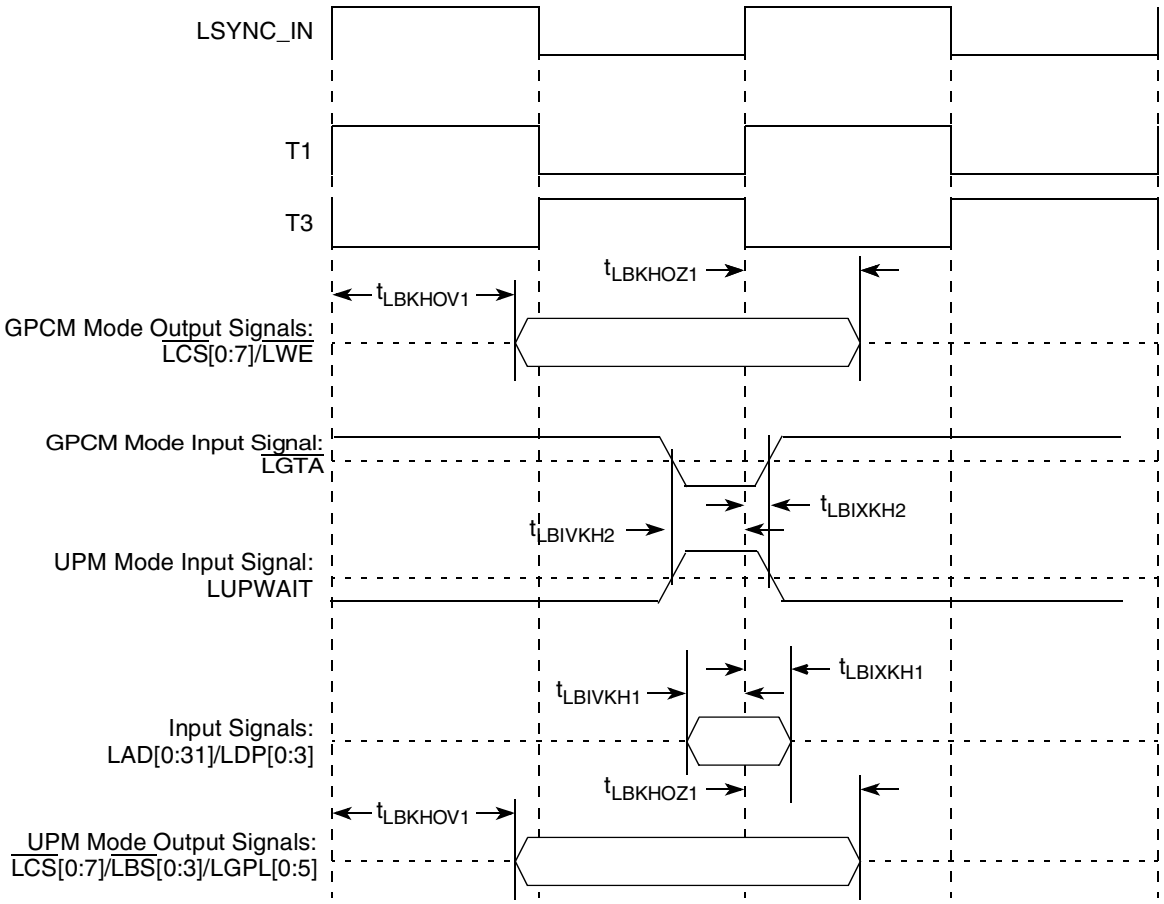



**Figure 41. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4(PLL Enabled)**

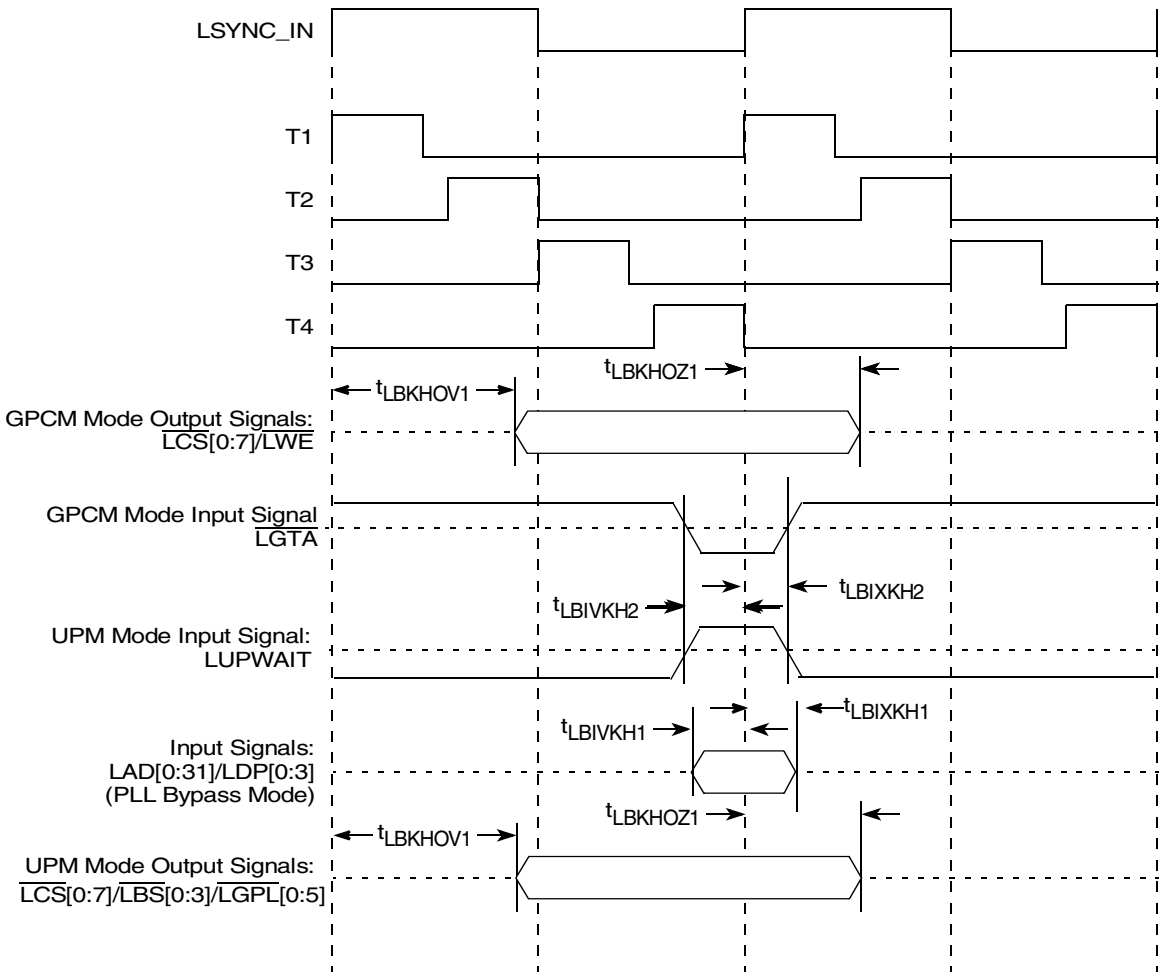



**Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)**

## 2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

### 2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

**Table 55. eSDHC interface DC Electrical Characteristics**

At recommended operating conditions (see Table 3)

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 0.625 * OVDD | OVDD+0.3 | V | — |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.25 * OVDD | V | — |
| Input/Output leakage current | $I_{IN}/I_{OZ}$ | — | –10 | 10 | uA | — |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -100 uA @OVDDmin | 0.75 * OVDD | — | V | — |

## 2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

**Table 59. Reference Clock Input Requirements**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SD2_REF_CLK/_B reference clock cycle time | $t_{CLK\_REF}$ | 100 | — | 150 | MHz | 1 |
| SD2_REF_CLK/_B frequency tolerance | $t_{CLK\_TOL}$ | –350 | 0 | +350 | ppm | — |
| SD_REF_CLK/_B rise/fall time (80%-20%) | $t_{CLK\_RISE}/t_{CLK\_FALL}$ | — | — | 1 | ns | — |
| SD_REF_CLK/_B duty cycle (@50% X2VDD) | $t_{CLK\_DUTY}$ | 45 | 50 | 55 | % | — |
| SD_REF_CLK/_B cycle to cycle clock jitter (period jitter) | $t_{CLK\_CJ}$ | — | — | 100 | ps | — |
| SD_REF_CLK/_B phase jitter (peak-to-peak) | $t_{CLK\_PJ}$ | –50 | — | +50 | ps | 2,3 |

**Note:**

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

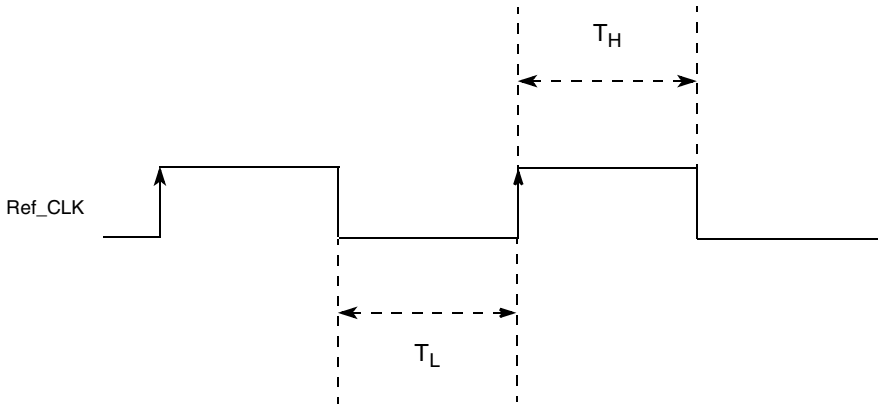



**Figure 49. Reference Clock Timing Waveform**

## 2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

### 2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

**Table 65. GPIO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | – 0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**

1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 66. GPIO Input and Output AC Timing Specifications[1]**

| Characteristic | Symbol [2] | Min | Unit | Notes |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 7.5 | ns | 3 |
| GPIO outputs—minimum pulse width | $t_{GTOWID}$ | 12 | ns | — |

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

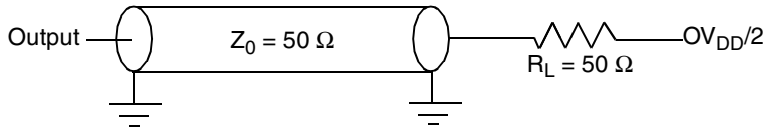



**Figure 53. GPIO AC Test Load**

This figure shows the PCI output AC timing conditions.

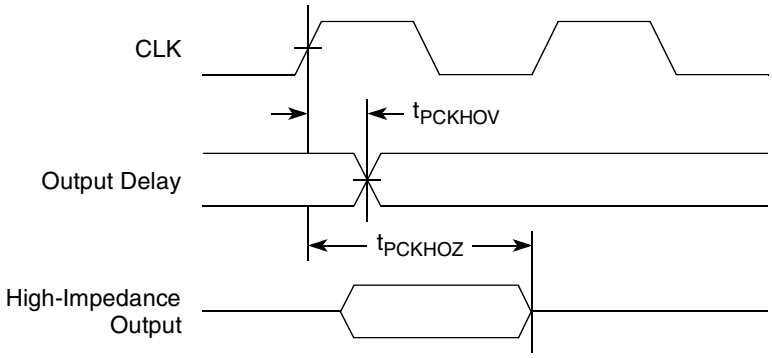



**Figure 56. PCI Output AC Timing Measurement Condition**

## 2.20 High-Speed Serial Interfaces

This chip features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for SGMII or SATA.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

### 2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 57 shows how the signals are defined. For illustration purposes, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn\_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn\_TX}}$, SDn_RX and $\overline{\text{SDn\_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**):

The Differential Output Voltage (or Swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX}$ - $V_{\overline{SDn\_TX}}$. The $V_{OD}$ value can be either positive or negative.

3. **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**):

The Differential Input Voltage (or Swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX}$ - $V_{\overline{SDn\_RX}}$. The $V_{ID}$ value can be either positive or negative.

4. **Differential Peak Voltage, $V_{DIFFp}$**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp}$ = |A - B| Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential

peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.

**6. Common Mode Voltage, $V_{cm}$**

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = V_{SDn\_TX} + V_{\overline{SDn\_TX}} = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

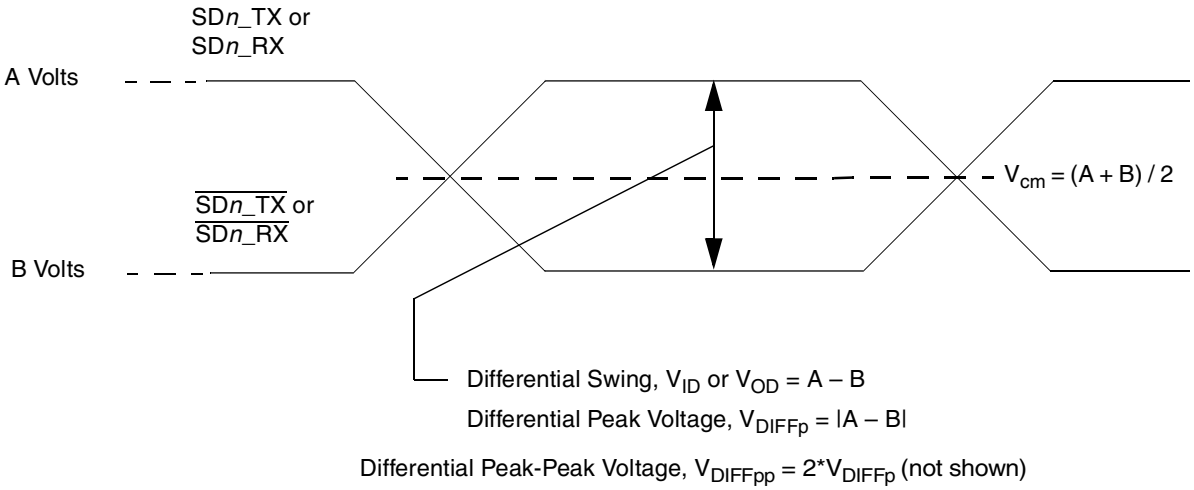



**Figure 57. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

## 2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks for PCI Express are SD1_REF_CLK and, $\overline{SD1\_REF\_CLK}$. The SerDes reference clocks for the SATA and SGMII interfaces are SD2_REF_CLK and, $\overline{SD2\_REF\_CLK}$.

The following sections describe the SerDes reference clock requirements and some application information.

### 2.20.2.1 SerDes Reference Clock Receiver Characteristics

Figure 58 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $X2V_{DD}$ are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SDn_REF_CLK and $\overline{SDn\_REF\_CLK}$ are internally AC-coupled differential inputs as shown in Figure 58. Each differential clock input (SD*n*_REF_CLK or $\overline{SDn\_REF\_CLK}$) has a 50-Ω termination to SGND (xcorevss) followed by on-chip AC-coupling.

— The external reference clock driver must be able to drive this termination.
— The SerDes reference clock input can be either differential or single-ended. See the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1V above SnGND (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800mV with the common mode voltage at 400mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SnGND (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

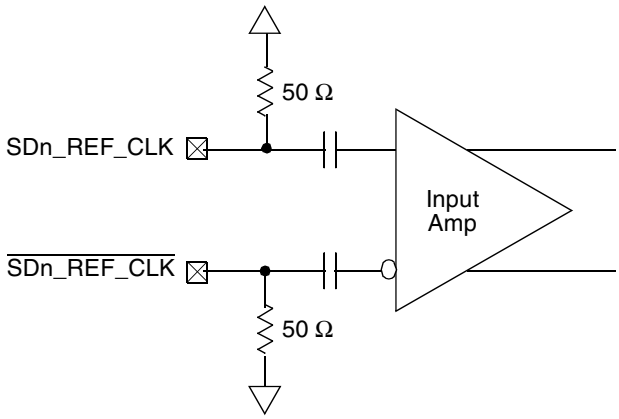



**Figure 58. Receiver of SerDes Reference Clocks**

## 2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

### 2.21.1 DC Requirements for PCI Express SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$

For more information, see Section 2.20.2, "SerDes Reference Clocks."

### 2.21.2 AC Requirements for PCI Express SerDes Clocks

This table lists AC requirements.

**Table 70. SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | 1,2,3 |

**Notes:**
1. Tj at BER of 10E-6 86 ps Max.
2. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 42 ps.
3. Limits from "PCI Express CEM Rev 2.0" and measured per "PCI Express Rj, D, and Bit Error Rates".

### 2.21.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

### 2.21.4 Physical Layer Specifications

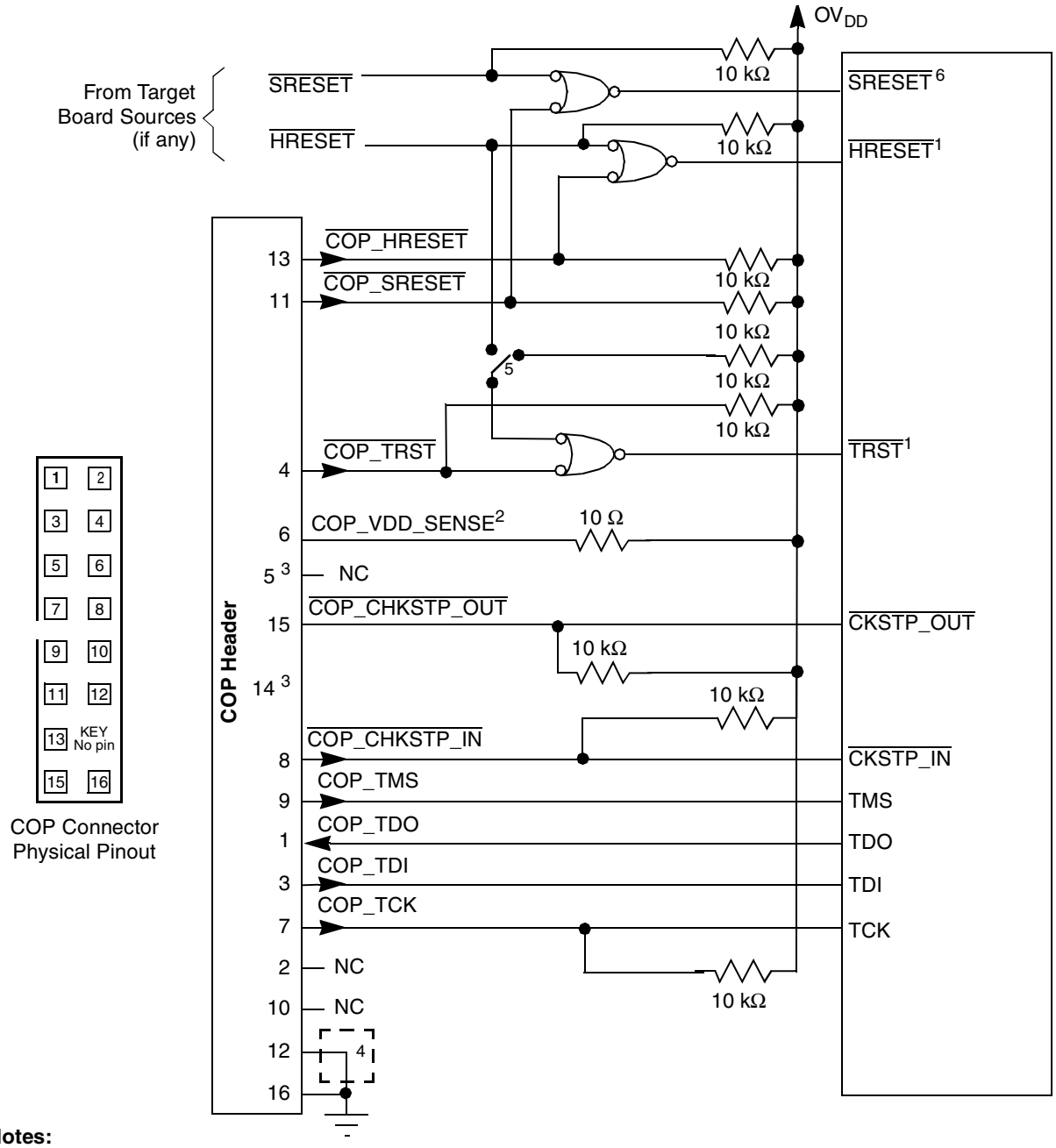
The following is a summary of the specifications for the physical layer of PCI Express on this chip. For further details as well as the specifications of the transport and data link layer, please use the PCI Express Base Specification. REV. 1.0a document.

#### 2.21.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 71. Differential Transmitter (TX) Output Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{TX\text{-}DIFFp\text{-}p}$ | Differential Peak-to-Peak Output Voltage | 0.8 | — | 1.2 | V | $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2. |




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

**Figure 78. JTAG Interface Connection**

# 5 Package Information

This section details package parameters, pin assignments, and dimensions.

## 5.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA) without a lid.

| | |
|---|---|
| Package outline | 29 mm × 29 mm |
| Interconnects | 783 |
| Pitch | 1 mm |
| Minimum module height | 2.23 mm |
| Maximum module height | 2.8 mm |
| Solder Balls | 96.5Sn/3.5Ag |
| Ball diameter (typical) | 0.6 mm |

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