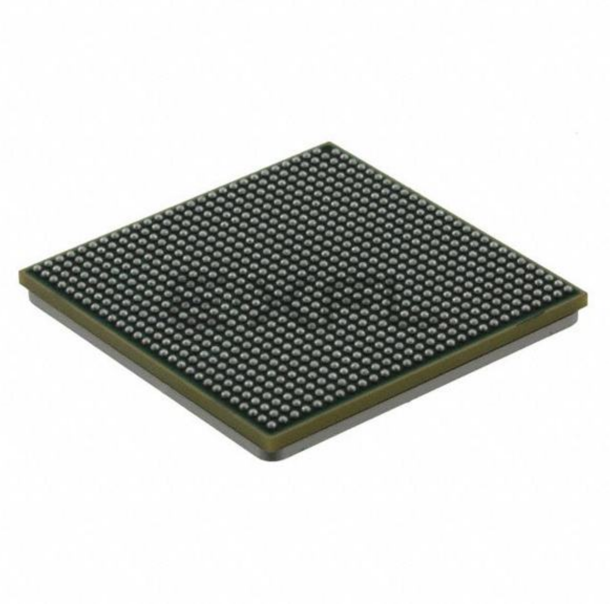

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.25GHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | SATA 3Gbps (1) |
| USB | USB 2.0 (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8535ecvtatha |

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**Table 5. Power Dissipation (continued)[5]**

| Power Mode | Core Frequency | CCB Frequency | DDR Frequency | $V_{DD}$ Platform | $V_{DD}$ Core | Junction Temperature | Core Power | | Platform Power[9] | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | (MHz) | (MHz) | (MHz) | (V) | (V) | (°C) | mean[7] | Max | mean[7] | Max | |
| Maximum (A) | 1250 | 500 | 500 | 1.0 | 1.0 | 105 / 90 | — | 5.3/4.4 | — | 5.0/4.0 | 1, 3, 8 |
| Thermal (W) | | | | | | | — | 4.4/3.6 | — | 5.0/4.0 | 1, 4, 8 |
| Typical (W) | | | | | | 65 | 2.2 | | 1.7 | | 1 |
| Doze (W) | | | | | | | 1.6 | 2.4 | 1.5 | 2.1 | 1 |
| Nap (W) | | | | | | | 0.8 | 1.6 | 1.5 | 2.1 | 1 |
| Sleep (W) | | | | | | | 0.8 | 1.6 | 1.1 | 1.7 | 1 |
| Deep Sleep (W) | | | | | | 35 | 0 | 0 | 0.6 | 1.2 | 1, 6 |

**Notes:**

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage ($V_{DD}$) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage ($V_{DD}$) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage ($V_{DD}$) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 $^{0}$C, for Industrial Tier is 105 $^{0}$C.
9. Platform power is the power supplied to all the $V_{DD\_PLAT}$ pins.

See Section 2.23.6.1, “SYSCLK to Platform Frequency Options,” for the full range of CCB frequencies that the chip supports.

This table provides the DDR capacitance when $GV_{DD}$(type) = 1.8 V.

**Table 14. DDR2 SDRAM Capacitance for $GV_{DD}$(typ)=1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1, 2 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1, 2 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.
2. This parameter is sampled. $GV_{DD}$ = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.175 V.

This table provides the current draw characteristics for $MV_{REF}$.

**Table 15. Current Draw Characteristics for $MV_{REF}$**

| Parameter/Condition | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Current draw for $MV_{REF}n$ | DDR2 SDRAM | $I_{MVREFn}$ | — | 1500 | μA | 1 |
| | DDR3 SDRAM | | | 1250 | | |

1.The voltage regulator for $MV_{REF}$ must be able to supply up to 1500 μA or 1250 uA current for DDR2 or DDR3 respectively.

## 2.6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM Controller interface. The DDR controller supports both DDR2 and DDR3 memories. Please note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 667 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this document.

### 2.6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

These tables provide the input AC timing specifications for the DDR controller.

**Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5%

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| AC input low voltage | 667 | $V_{ILAC}$ | — | $MV_{REF}$ – 0.20 | V |
| | <=533 | | — | $MV_{REF}$ – 0.25 | V |
| AC input high voltage | 667 | $V_{IHAC}$ | $MV_{REF}$ + 0.20 | — | V |
| | <=533 | | $MV_{REF}$ + 0.25 | — | V |

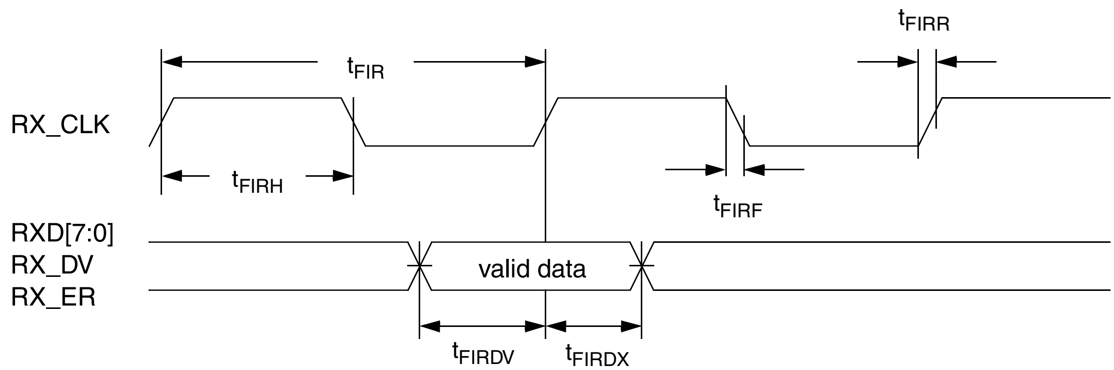



**Figure 15. FIFO Receive AC Timing Diagram**

### 2.9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

#### 2.9.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

**Table 28. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTK}$ | — | 8.0 | — | ns |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$[3] | 0.5 | — | 5.0 | ns |
| GTX_CLK data clock rise time (20%-80%) | $t_{GTXR}$ | — | — | 1.0 | ns |
| GTX_CLK data clock fall time (80%-20%) | $t_{GTXF}$ | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid tGTKHDV to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the GMII receive AC timing diagram.

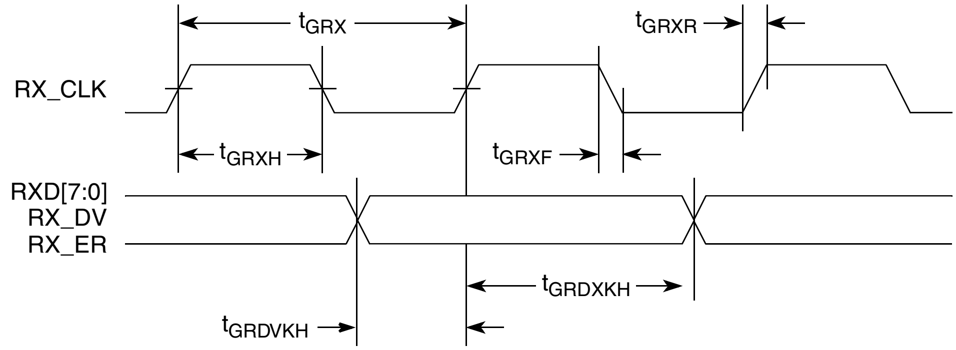



**Figure 18. GMII Receive AC Timing Diagram**

### 2.9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

#### 2.9.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

**Table 30. MII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$ | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise (20%-80%) | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%-20%) | $t_{MTXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

## 2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

**Table 44. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.13 | 3.47 | V |
| Output high voltage ($OV_{DD}$ = Min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.40 | $OV_{DD}$ + 0.3 | V |
| Output low voltage ($OV_{DD}$ =Min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | GND | 0.40 | V |
| Input high voltage | $V_{IH}$ | 2.0 | — | V |
| Input low voltage | $V_{IL}$ | — | 0.90 | V |
| Input high current ($OV_{DD}$ = Max, $V_{IN}$ [1] = 2.1 V) | $I_{IH}$ | — | 40 | μA |
| Input low current ($OV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA |

**Note:**

1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 45. MII Management AC Timing Specifications**

At recommended operating conditions with OVDD is 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_MDC frequency | $f_{MDC}$ | 0.74 | 2.5 | 8.3 | MHz | 2 |
| EC_MDC period | $t_{MDC}$ | 120 | 400 | 1350 | ns | — |
| EC_MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| EC_MDC to EC_MDIO delay | $t_{MDKHDX}$ | (16 * $t_{plb\_clk}$)-3 | — | (16 * $t_{plb\_clk}$)+3 | ns | 3,5,6 |
| EC_MDIO to EC_MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |

**Table 52. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC) (continued)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | — | $t_{LBKHOX2}$ | 0.8 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | — | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | — | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 1.8 V DC.

**Table 53. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | — | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 2.4 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.9 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | — | $t_{LBOTOT}$ | 1.2 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | — | $t_{LBKHOV1}$ | — | 3.2 | ns | — |
| Local bus clock to data valid for LAD/LDP | — | $t_{LBKHOV2}$ | — | 3.2 | ns | 3 |
| Local bus clock to address valid for LAD | — | $t_{LBKHOV3}$ | — | 3.2 | ns | 3 |
| Local bus clock to LALE assertion | — | $t_{LBKHOV4}$ | — | 3.2 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | — | $t_{LBKHOX1}$ | 0.9 | — | ns | 3 |

This figures show the local bus signals.

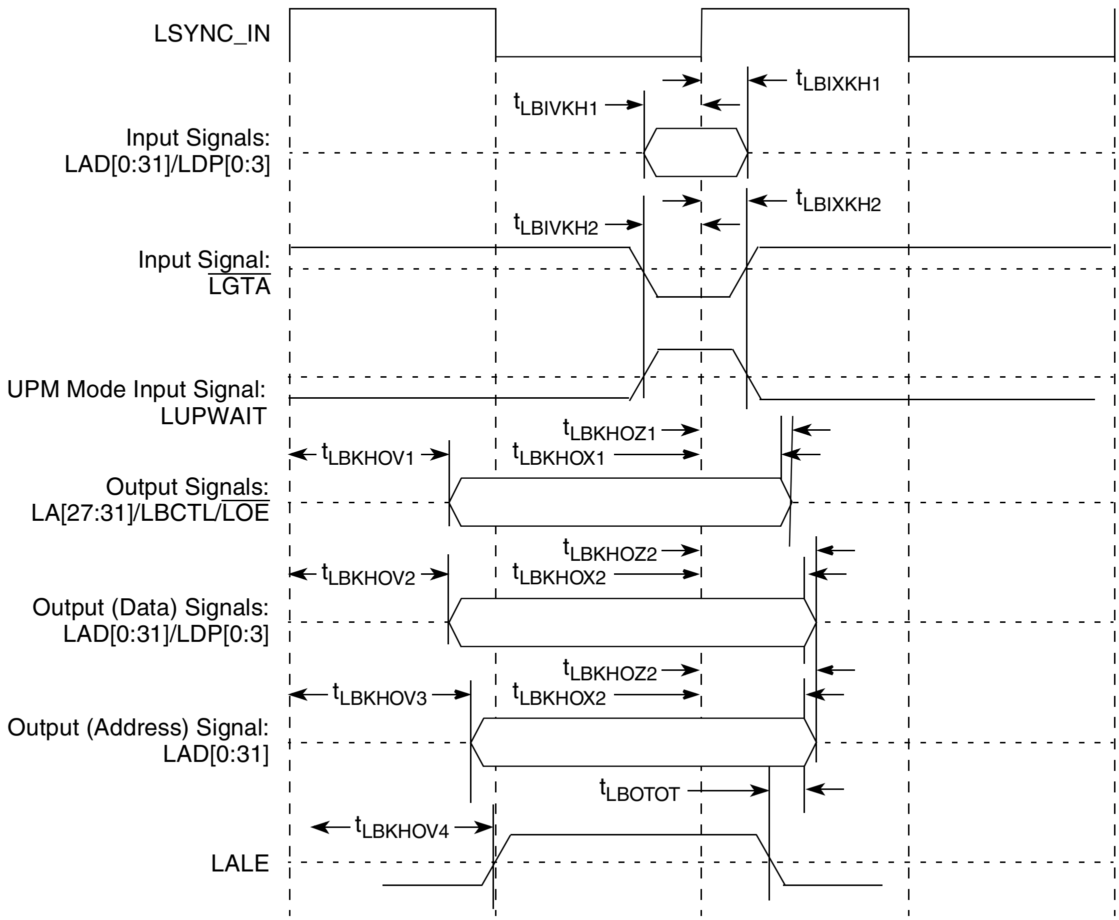



**Figure 39. Local Bus Signals, Non-Special Signals Only (PLL Enabled)**

## NOTE

In PLL bypass mode, some signals are launched and captured on the opposite edge of LCLK[n] to that used in PLL Enable Mode. In this mode, output signals are launched at the falling edge of the LCLK[n] and inputs signals are captured at the rising edge of LCLK[n] with the exception of LGTA/LUPWAIT (which is captured at the falling edge of the LCLK[n]).

This figure provides the eSDHC clock input timing diagram.

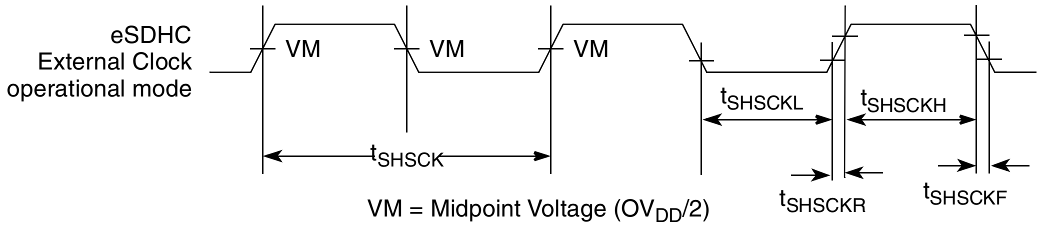



**Figure 43. eSDHC Clock Input Timing Diagram**

This figure provides the data and command input/output timing diagram.

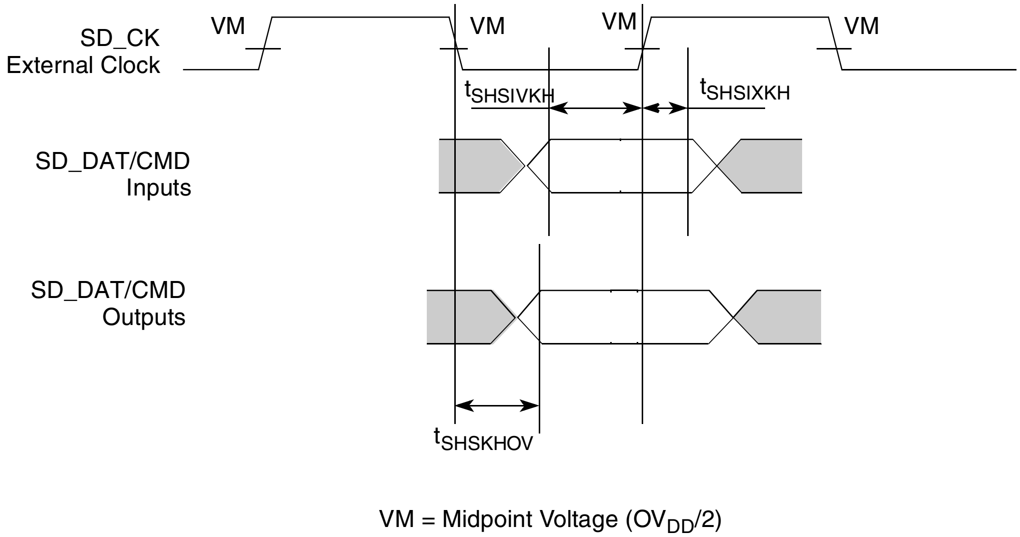



**Figure 44. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock**

# 2.14 Programmable Interrupt Controller (PIC)

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

# 2.15 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

## 2.15.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

**Table 57. JTAG DC Electrical Characteristics**

| Parameter | Symbol [1] | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | -0.3 | 0.8 | V |

This figure provides the AC test load for TDO and the boundary-scan outputs.

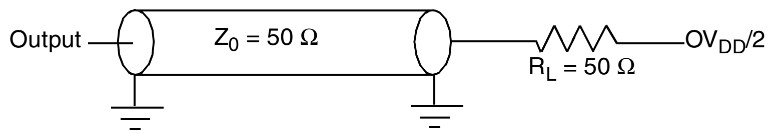



**Figure 45. AC Test Load for the JTAG Interface**

This figure provides the JTAG clock input timing diagram.

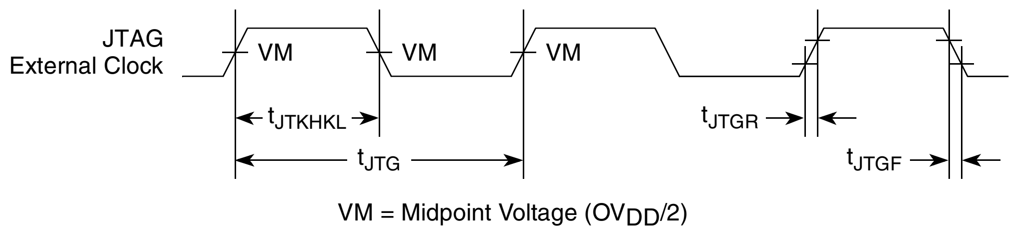



**Figure 46. JTAG Clock Input Timing Diagram**

This figure provides the $\overline{\text{TRST}}$ timing diagram.

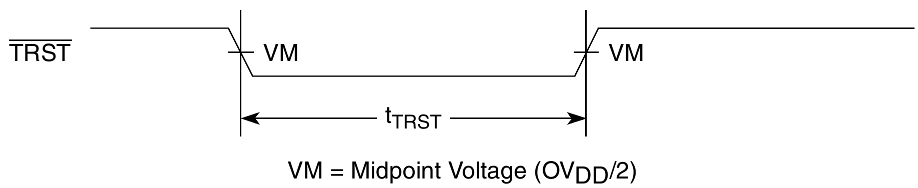



**Figure 47. $\overline{\text{TRST}}$ Timing Diagram**

This figure provides the boundary-scan timing diagram.

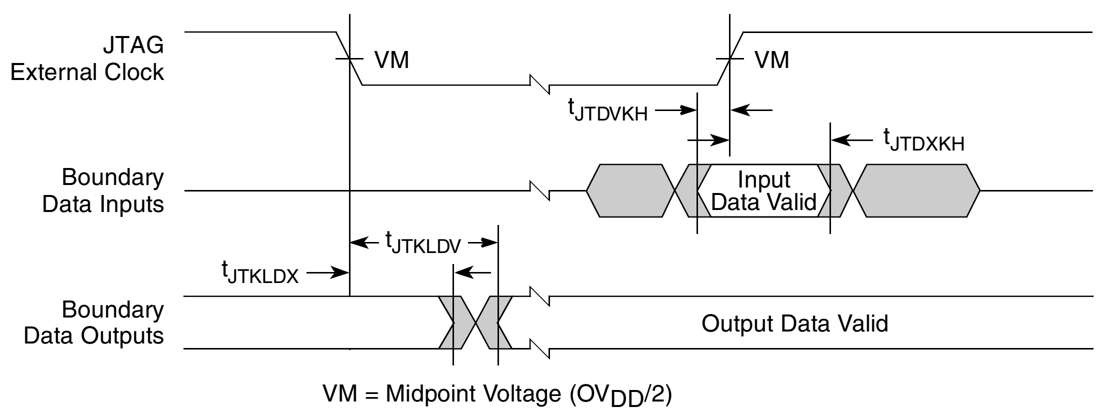



**Figure 48. Boundary-Scan Timing Diagram**

## 2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

**Table 64. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 63).

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | μs | — |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V | — |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V | — |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the chip acts as the I²C bus master while transmitting, the chip drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. For details of the I²C frequency calculation, refer to *Determining the I²C Frequency Divider Ratio for SCL* (AN2919). Note that the I²C Source Clock Frequency is half of the CCB clock frequency for the chip.
3. The maximum $t_{I2DVKH}$ has only to be met if the chip does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. $C_B$ = capacitance of one bus line in pF.

This figure provides the AC test load for the I²C.

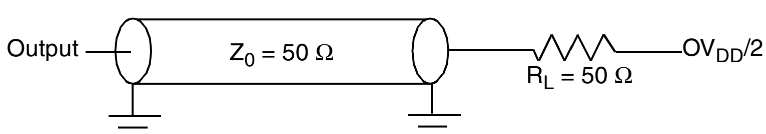



**Figure 51. I²C AC Test Load**

This figure shows the AC timing diagram for the I²C bus.

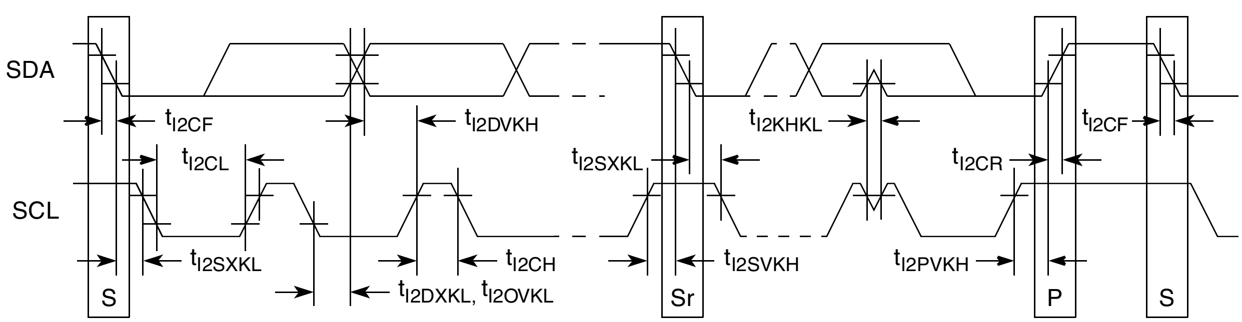



**Figure 52. I²C Bus AC Timing Diagram**

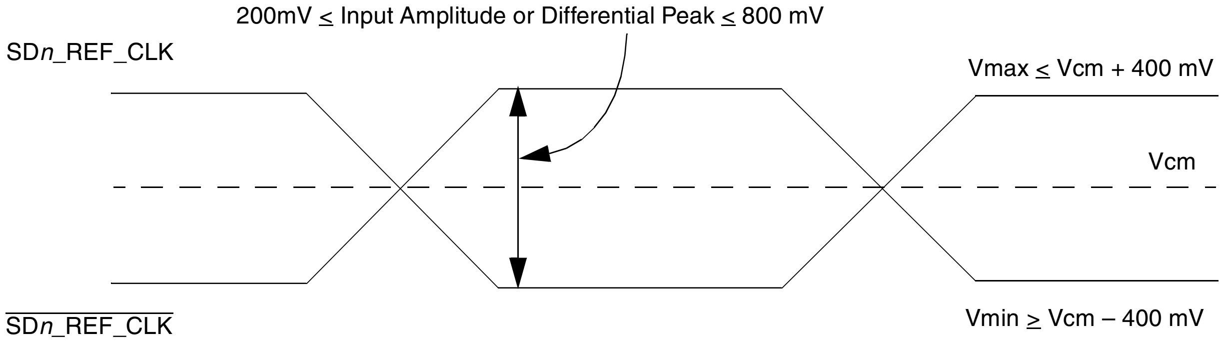



**Figure 60. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

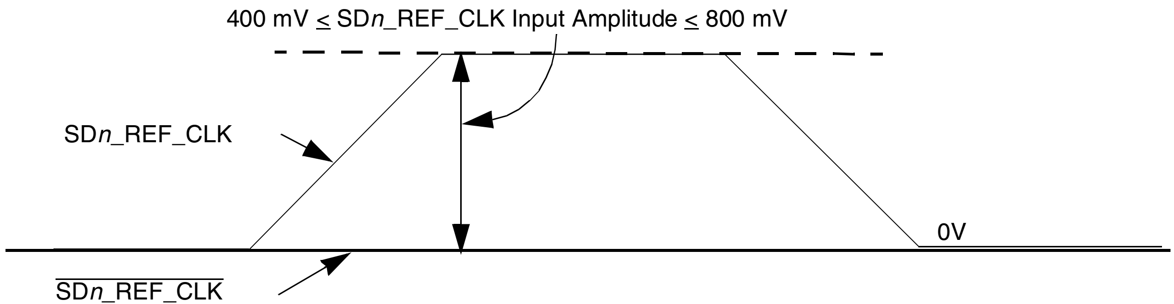



**Figure 61. Single-Ended Reference Clock Input DC Requirements**

### 2.20.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SnGND (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL (Low Voltage Positive Emitter-Coupled Logic) outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 62 to Figure 65 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the chip’s SerDes reference clock receiver requirement provided in this document.

### 2.21.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 69 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

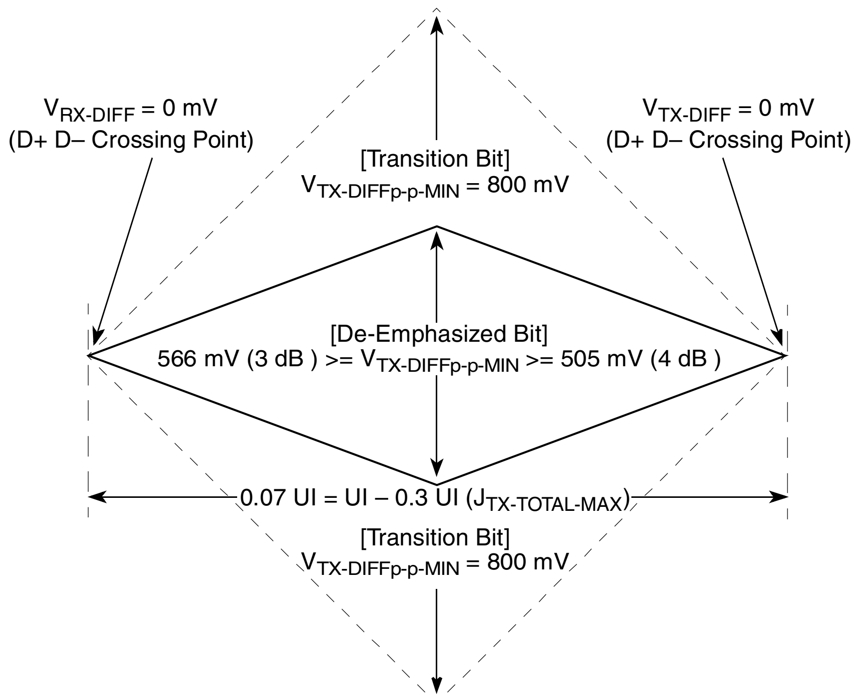



**Figure 69. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 77). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

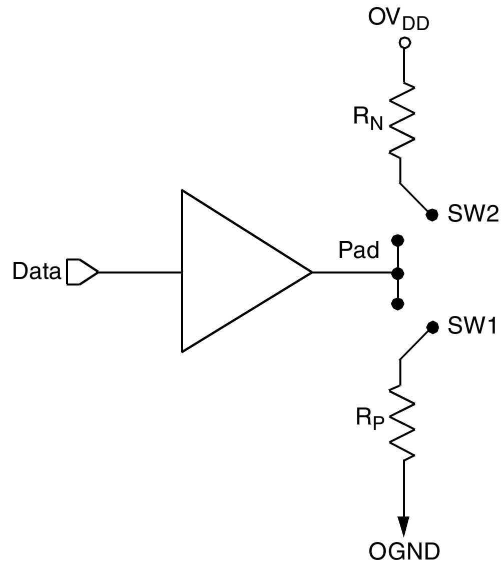



**Figure 77. Driver Impedance Measurement**

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 81. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 45 Target | 45 Target (cfg_pci_impd=1)<br>25 Target (cfg_pci_impd=0) | 18 Target (full strength mode)<br>36 Target (full strength mode) | $Z_0$ | Ω |
| $R_P$ | 45 Target | 45 Target (cfg_pci_impd=1)<br>25 Target (cfg_pci_impd=0) | 18 Target (full strength mode)<br>36 Target (full strength mode) | $Z_0$ | Ω |

**Note:** Nominal supply voltages. See Table 1.

## 3.9 Configuration Pin Muxing

The chip provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the chip into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 3.10 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredicatable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The chip requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 78 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 79, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

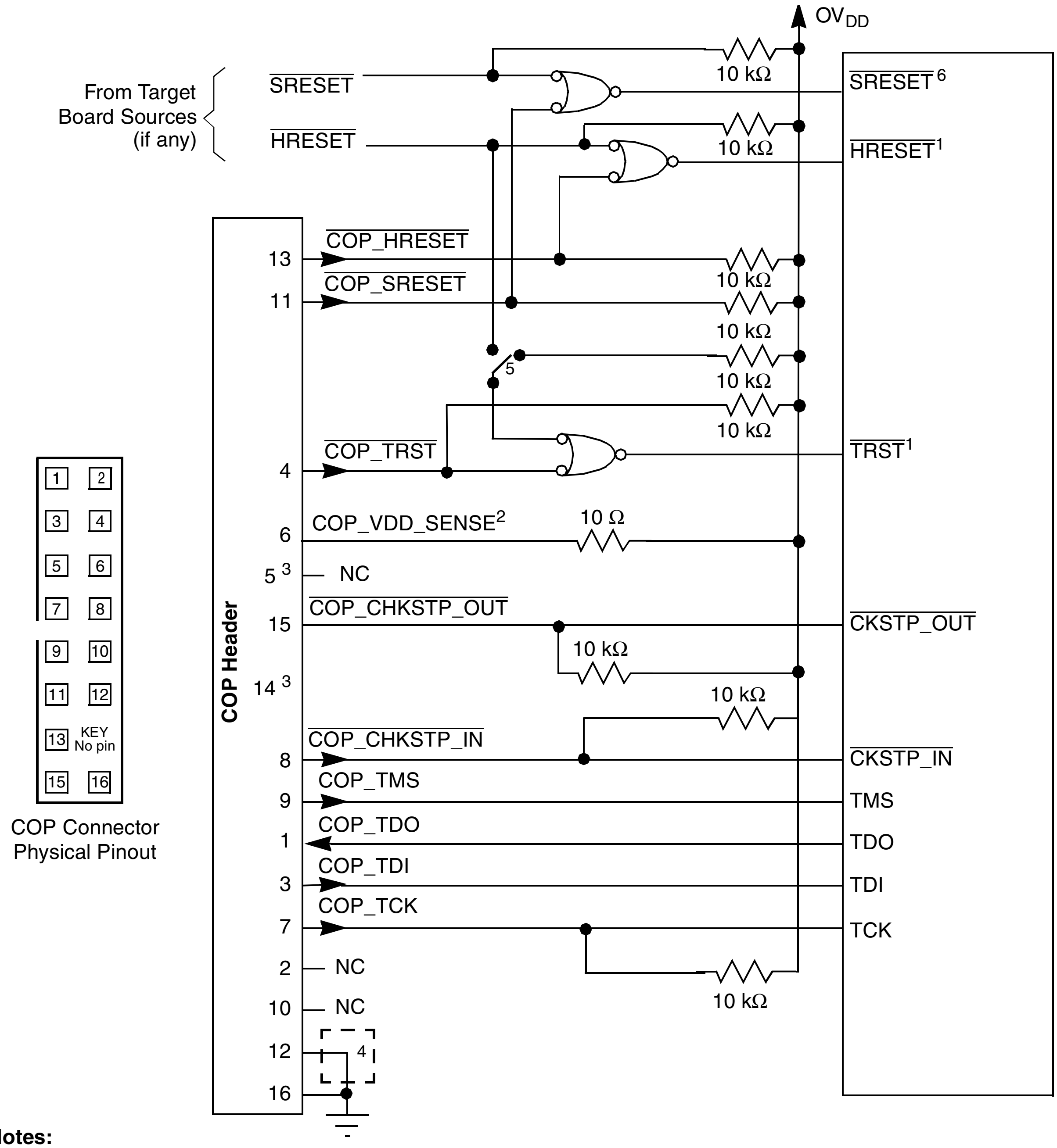
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 79 is common to all known emulators.

### 3.10.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 78. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

**Figure 78. JTAG Interface Connection**

## 4.1 Part Numbers Fully Addressed by this Document

This table shows the part numbering nomenclature.

**Table 82. Part Numbering Nomenclature**

| *MPC* | *nnnn* | *E* | *C* | *VT* | *AA* | *X* | *R* |
|---|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Security Engine** | **Tiers and Temperature Range** | **Package** [1] | **Processor Frequency** [2] | **DDR Frequency**[3] | **Revision Level** |
| MPC | 8536<br>8535 | E = included | • A = Commercial tier standard temperature range (0° to 90°C)<br>• B or Blank = industrial tier standard temperature range (0° to 105°C)<br>• C = Industrial tier extended temperature range (–40° to 105°C) | • VT = FC-PBGA<br>• (Pb-free)<br>• PX = plastic standard | • AK = 600 MHz<br>• AN = 800 MHz<br>• AQ = 1000 MHz<br>• AT = 1250 MHz<br>• AU = 1333 MHz<br>• AV = 1500 MHz | • G = 400 MHz<br>• H = 500 MHz<br>• J = 533 MHz<br>• L = 667 MHz | • Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0190, 0x803F0191)<br>• A = Ver. 1.2 (SVR = 0x803F0192) |
| | | Blank = not included | | | | | • Blank = Ver. 1.0 or 1.1 (SVR = 0x80370190, 0x80370191)<br>• A = Ver. 1.2 (SVR = 0x80370192) |

**Notes:**

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.

# 5 Package Information

This section details package parameters, pin assignments, and dimensions.

## 5.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA) without a lid.

| | |
|---|---|
| Package outline | 29 mm × 29 mm |
| Interconnects | 783 |
| Pitch | 1 mm |
| Minimum module height | 2.23 mm |
| Maximum module height | 2.8 mm |
| Solder Balls | 96.5Sn/3.5Ag |
| Ball diameter (typical) | 0.6 mm |

5. Capacitors may not be present on all devices
6. Caution must be taken not to short exposed metal capacitor pads on package top.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

# 6 Product Documentation

The following documents are required for a complete description of the chip and are needed to design properly with the part.

- *MPC8536E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8536ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)

# 7 Document Revision History

This table provides a revision history for this hardware specification.

**Table 85. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 5 | 09/2011 | • Removed PVDD from Table 1, "Pinout Listing." |
| 4 | 06/2011 | • In Table 1, "Pinout Listing," updated the power supply for TSEC3 pins to TVDD.<br>• Updated Table 56, "eSDHC AC Timing Specifications."<br>• In Section 4.3, "Part Numbering," added an extra bin (1250/500/667) to support DDR3. |
| 3 | 11/2010 | • In Table 1, "Pinout Listing," added the following note: "For systems that boot from Local Bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required..." In addition, updated footnote 26 and added footnote 29 to PCI1_AD.<br>• Updated Table 21<br>• Updated Figure 25, "RGMII and RTBI AC Timing and Multiplexing Diagrams."<br>• In Table 44, "MII Management DC Electrical Characteristics," changed the Voh/Vol values for MDIO/MDC.<br>• Added Note 6 regarding USB*n*_DIR pin to Table 47, "USB General Timing Parameters6."<br>• In Table 64, "I2C AC Electrical Specifications," updated footnote 2.<br>• In Table 82, , Table 83, , Table 84, added the Revision Level A for Rev 1.2 |
| 2 | 09/2009 | **Note:**<br>• In Section 1, "Pin Assignments and Reset States,"updated the first sentence of the note to say, "The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration."<br>• In Table 40, "SGMII DC Receiver Electrical Characteristics," changed LSTSAB to LSTSA and LSTSEF to LSTSE for Note 4.<br>• Updated Die value and Bump/Underfill value in Table 84<br>**Note:** Updated Figure 81, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA," and its notes. |
| 1 | 09/2009 | • In Table 3, "Recommended Operating Conditions," for $V_{DD\_CORE,}$ removed 1.1 ± 55 mV.<br>• In Table 5, "Power Dissipation 5," remove note 5.<br>• In Table 5, "Power Dissipation 5," changed an "—" to "0." |
| 0 | 08/2009 | • Initial public release. |

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