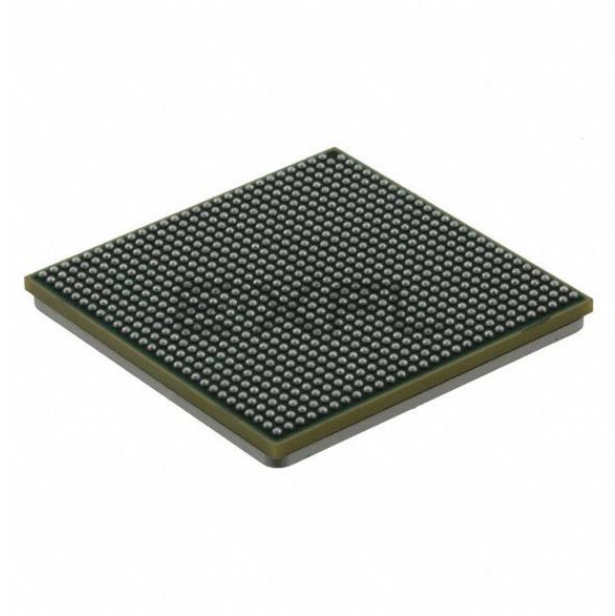

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8536avjanga

This figure shows the major functional units within the chip.

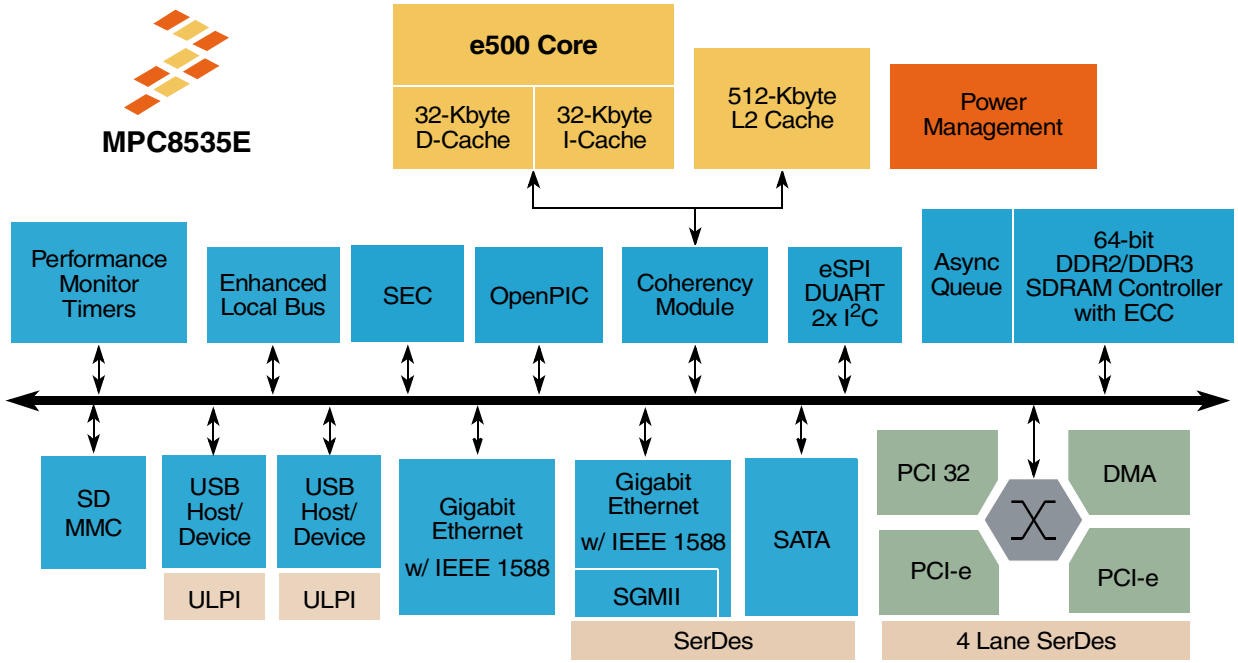


Figure 1. Chip Block Diagram

1 Pin Assignments and Reset States

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST\_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

Table 5. Power Dissipation (continued)[5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	1250	500	500	1.0	1.0	105 / 90	—	5.3/4.4	—	5.0/4.0	1, 3, 8
Thermal (W)							—	4.4/3.6	—	5.0/4.0	1, 4, 8
Typical (W)						65	2.2		1.7		1
Doze (W)							1.6	2.4	1.5	2.1	1
Nap (W)							0.8	1.6	1.5	2.1	1
Sleep (W)							0.8	1.6	1.1	1.7	1
Deep Sleep (W)						35	0	0	0.6	1.2	1, 6

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 ^{0}C, for Industrial Tier is 105 ^{0}C.
9. Platform power is the power supplied to all the V_{DD_PLAT} pins.

See Section 2.23.6.1, "SYSCLK to Platform Frequency Options," for the full range of CCB frequencies that the chip supports.

2.4 Input Clocks

2.4.1 System Clock Timing

This table provides the system clock (SYSCLK) AC timing specifications for the chip.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	—
SYSCLK jitter	—	—	—	+/-150	ps	3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," and Section 2.23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 KHz and 60 KHz on SYSCLK.

2.4.2 PCI Clock Timing

When the PCI controller is configured for asynchronous operation, the reference clock for the PCI controller is not the SYSCLK input, but instead the PCI_CLK. This table provides the PCI reference clock AC timing specifications for the chip.

Table 7. PCICLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCICLK frequency	f_{PCICLK}	33	—	66	MHz	—
PCICLK cycle time	t_{PCICLK}	15	—	30	ns	—
PCICLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	1
PCICLK duty cycle	t_{KHK}/t_{PCICLK}	40	—	60	%	—

Notes:
1. Rise and fall times for PCICLK are measured at 0.6 V and 2.7 V.

2.4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

This figure shows the GMII receive AC timing diagram.

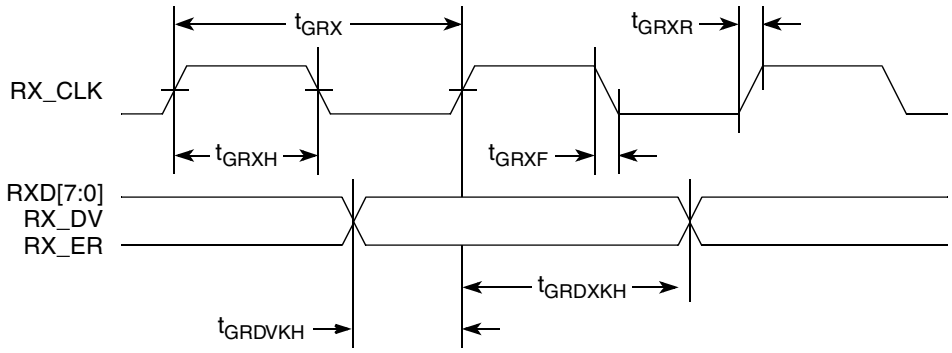


Figure 18. GMII Receive AC Timing Diagram

2.9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.9.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 30. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

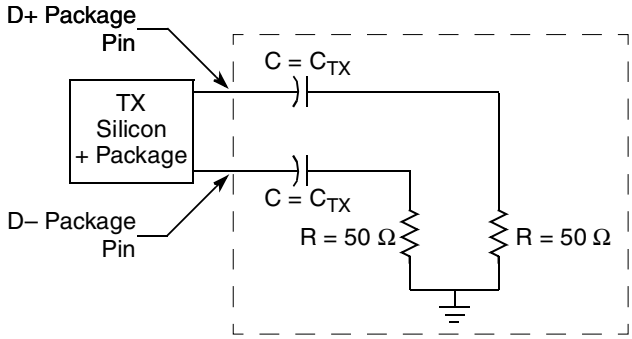


Figure 32. SGMII AC Test/Measurement Load

2.9.4 eTSEC IEEE 1588 AC Specifications

This figure shows the data and command output timing diagram.

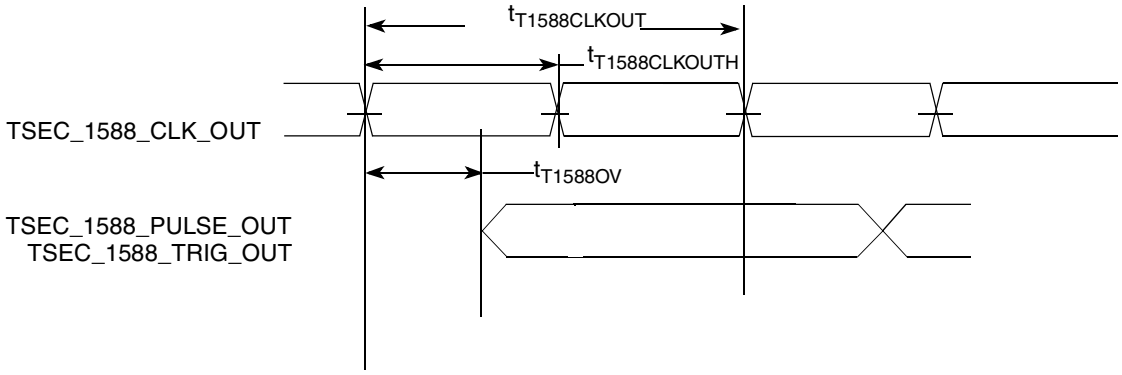


Figure 33. eTSEC IEEE 1588 Output AC timing

[1] The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

This figure provides the data and command input timing diagram.

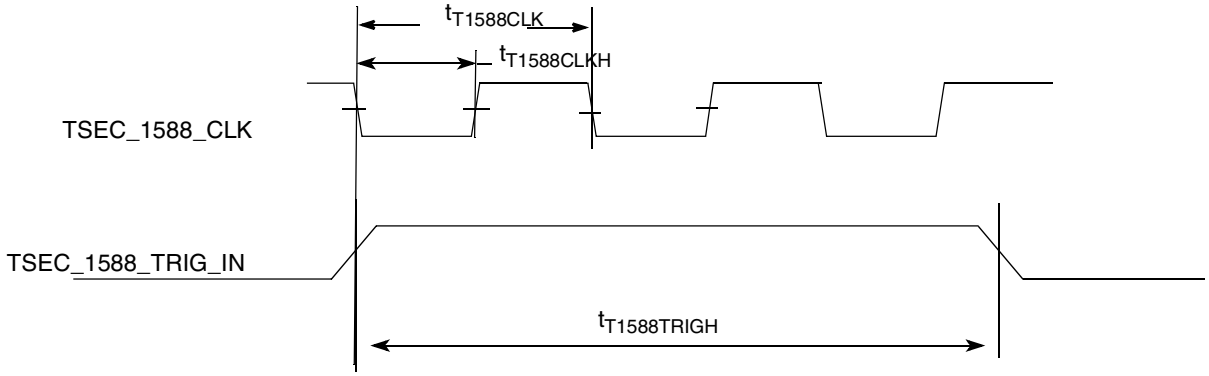


Figure 34. eTSEC IEEE 1588 Input AC timing

2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

Table 44. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.40	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDC frequency	f_{MDC}	0.74	2.5	8.3	MHz	2
EC_MDC period	t_{MDC}	120	400	1350	ns	—
EC_MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
EC_MDC to EC_MDIO delay	t_{MDKHDX}	(16 * t_{plb_clk})-3	—	(16 * t_{plb_clk})+3	ns	3,5,6
EC_MDIO to EC_MDC setup time	t_{MDDVKH}	5	—	—	ns	—

2.12 enhanced Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

2.12.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 48. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	1.9	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 49. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 50. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	—	1.71	1.89	V
High-level input voltage	V_{IH}	—	0.65*BV_{DD}	0.3+BV_{DD}	V
Low-level input voltage	V_{IL}	—	–0.3	0.35*BV_{DD}	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	-15	10	μA
High-level output voltage	V_{OH}	I_{OH} = –100 μA	BV_{DD} – 0.2	—	V
		I_{OH} = –2 mA	BV_{DD} – 0.45	—	
Low-level output voltage	V_{OL}	I_{OH} = 100 μA	—	0.2	V
		I_{OH} = 2 mA	—	0.45	

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

2.12.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V DC. For information about the frequency range of local bus see Section 2.23.1, “Clock Ranges.”

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.4	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3

This figures show the local bus signals.

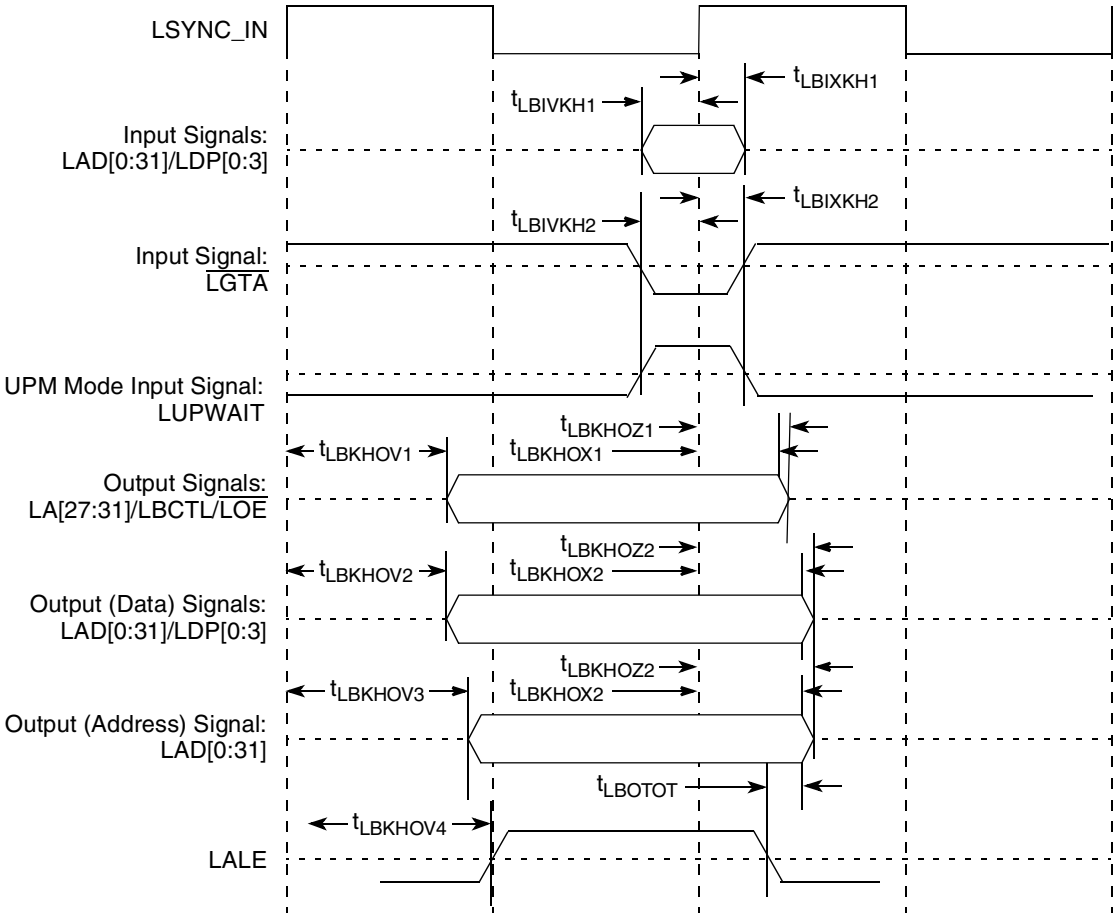


Figure 39. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

NOTE

In PLL bypass mode, some signals are launched and captured on the opposite edge of LCLK[n] to that used in PLL Enable Mode. In this mode, output signals are launched at the falling edge of the LCLK[n] and inputs signals are captured at the rising edge of LCLK[n] with the exception of LGTA/LUPWAIT (which is captured at the falling edge of the LCLK[n]).

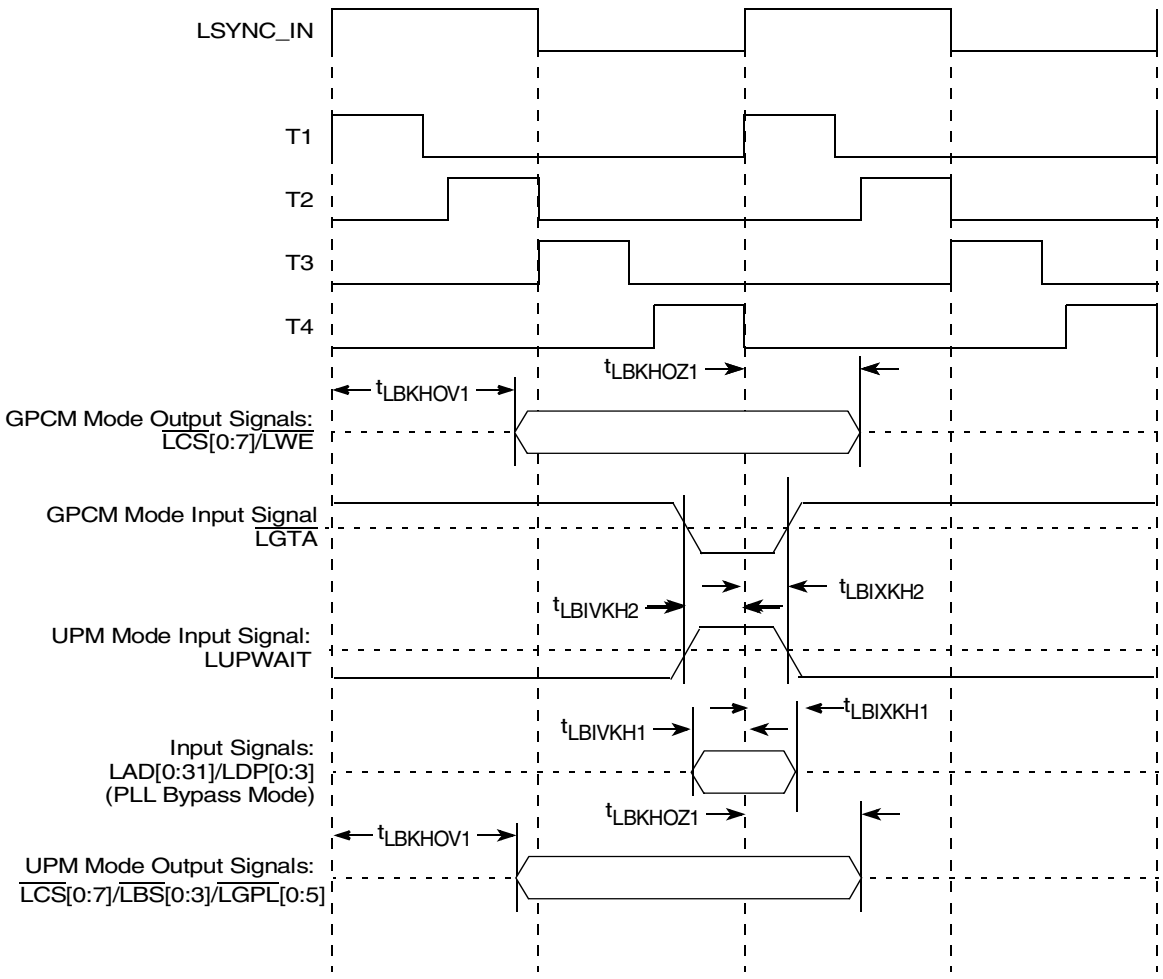


Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 * OVDD	OVDD+0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.25 * OVDD	V	—
Input/Output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—
Output high voltage	V_{OH}	I_{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	—

Table 55. eSDHC interface DC Electrical Characteristics (continued)

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output low voltage	V_{OL}	I_{OL} = 100uA @OVDDmin	—	0.125 * OVDD	V	—
Output high voltage	V_{OH}	I_{OH} = -100 uA	OV_{DD} - 0.2	—	—	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	—	2

Notes:

1. The min V_{IL} and V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.13.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in the following figure.

Table 56. eSDHC AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full speed/high speed mode MMC Full speed/high speed mode	f_{SHSCK}	 0	 25/50 20/52	MHz	2, 5
SD_CLK clock frequency - identification mode	f_{SIDCK}	0 100	400	KHz	3, 5
SD_CLK clock low time - High speed/Full speed mode	t_{SHSCKL}	7/10	—	ns	5
SD_CLK clock high time - High speed/Full speed mode	t_{SHSCKH}	7/10	—	ns	5
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	5
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	4,5,6
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	5,6
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	5,6

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52MHz for a MMC card.
3. 0 Hz means to stop the clock. The given minimum frequency range is for cases were a continuous clock is required.
4. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns.
5. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF
6. The parameter values apply to both full speed and high speed modes.

Table 57. JTAG DC Electrical Characteristics (continued)

Parameter	Symbol [1]	Min	Max	Unit
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

This table provides the JTAG AC timing specifications as defined in the following figures.

Table 58. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions (see Table 3).

Parameter	Symbol [1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times:	t_{JTDVKH}	4	—	ns	
Input hold times:	t_{JTDXKH}	10	—	ns	
Output Valid times:	t_{JTKLDV}	—	10	ns	3
Output hold times:	t_{JTKLDX}	0	—	ns	3

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3.) The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

Table 60. Differential Transmitter (TX) Output Characteristics (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
TX Common Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXCC11}	 — — — — — —	 — — — — — —	 5 5 2 2 1 1	 dB	 1, 2
TX Impedance Balance 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXDC11}	 — — — — — —	 — — — — — —	 30 20 10 10 4 4	 dB	 1, 2
Deterministic jitter 1.5G 3.0G	U_{SATA_TXDJ}	—	—	 0.18 0.14	 UI	—
Total Jitter 1.5G 3.0G	U_{SATA_TXTJ}	—	—	 0.42 0.32	 UI	—

Notes:
1. Only applies when operating in 3.0Gb data rate mode.
2. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
3. Only applies to Gen1i mode.

2.16.4 Out-of-Band (OOB) Electrical Characteristics

This table provides the Out-of-Band (OOB) electrical characteristics for the SATA interface of the chip.

Table 62. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	 mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	646.67	666.67	686.67	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTXWakeGap}$	—	160	—	UI	—
COMWAKE Gap Detection Windows	$T_{SATA\_OOBDetWakeGap}$	55	—	175	ns	—
COMINIT/ COMRESET Gap Detection Windows	$T_{SATA\_OOBDetCOMGap}$	175	—	525	ns	—

2.17 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interfaces of the chip.

2.17.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 63. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	OV_{DD}	3.13	3.47	V	—
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 65. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	7.5	ns	3
GPIO outputs—minimum pulse width	t_{GTOWID}	12	ns	—

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

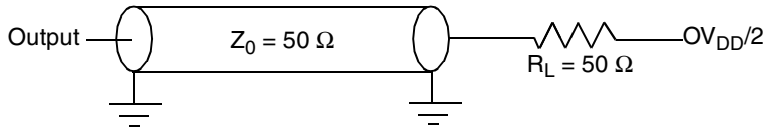


Figure 53. GPIO AC Test Load

— The external reference clock driver must be able to drive this termination.
— The SerDes reference clock input can be either differential or single-ended. See the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1V above SnGND (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800mV with the common mode voltage at 400mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SnGND (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

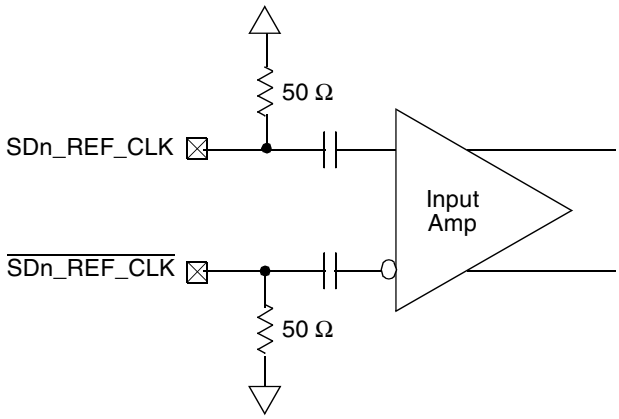


Figure 58. Receiver of SerDes Reference Clocks

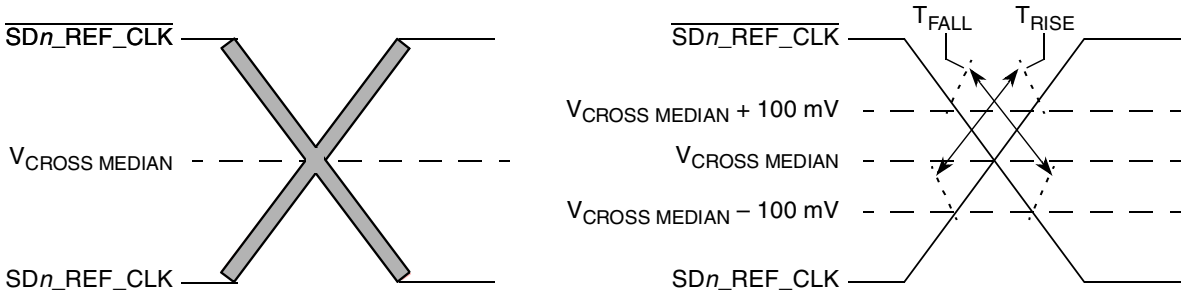


Figure 67. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 2.9.3.2, "AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK"
- Section 2.21.2, "AC Requirements for PCI Express SerDes Clocks"

2.20.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

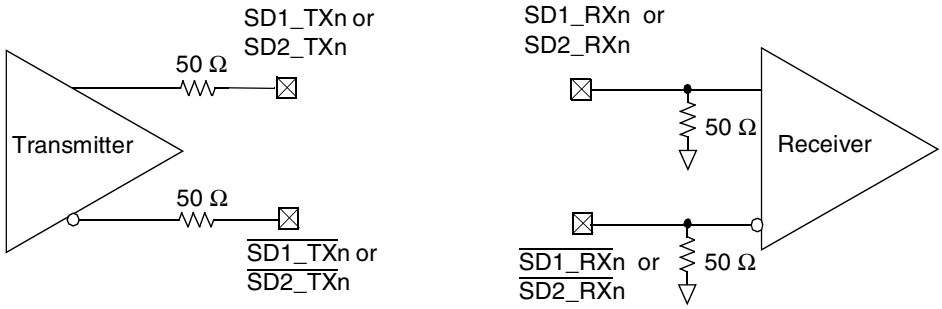


Figure 68. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SATA or SGMII) in this document based on the application usage:

- Section 2.9.3, "SGMII Interface Electrical Characteristics"
- Section 2.21, "PCI Express"
- Section 2.16, "Serial ATA (SATA)"

Please note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

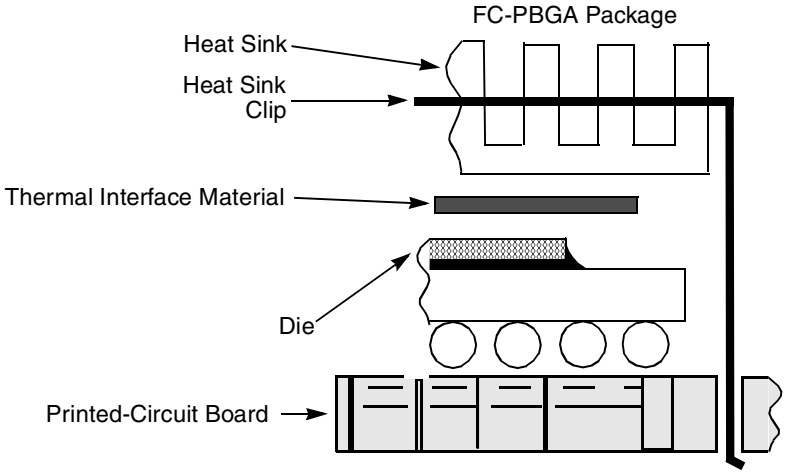


Figure 73. Package Exploded Cross-Sectional View with Several Heat Sink Options

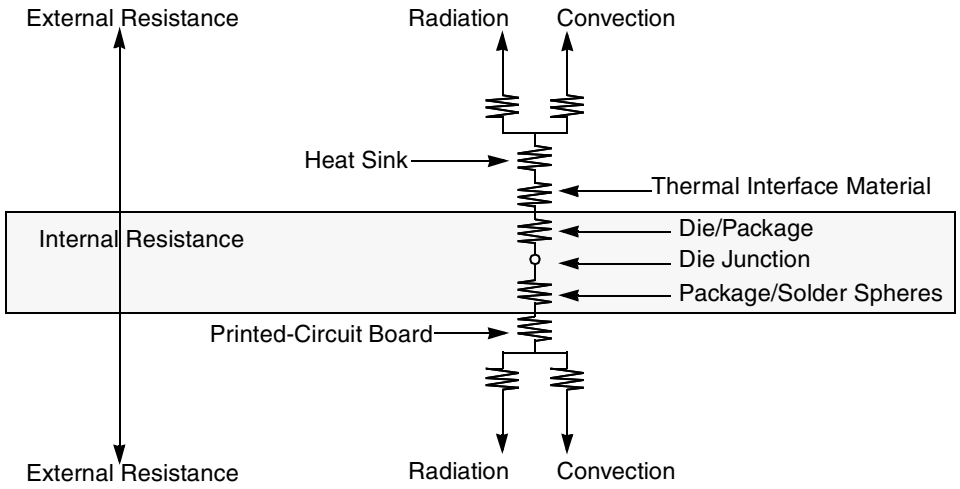
The system board designer can choose between several types of heat sinks to place on the chip. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the chip to function in various environments.

2.24.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 70, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values types and quantity of bulk capacitors.

3.5 SerDes Block Power Supply Decoupling Recommendations

he SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power (SnV_{DD} and XnV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the chip. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the chip as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (SnV_{DD} and XnV_{DD}) to the board ground plane on each side of the chip. This should be done for all SerDes supplies.
- Third, between the chip and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND pins of the chip.

3.7 Pull-Up and Pull-Down Resistor Requirements

The chip requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC1_TXD[3], $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The UART_SOUT[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. Please refer to the pinlist table (see Table 62) of the individual chip for more details.

See the PCI 2.2 specification for all pull-ups required for PCI.

3.8 Output Buffer DC Impedance

The chip drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).