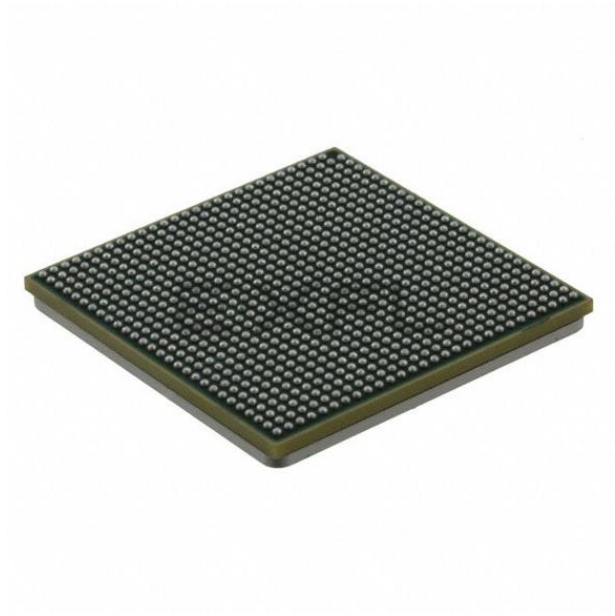

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8536avjaula

This table provides the pin-out listing for the 783 FC-PBGA package.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
PCI					
PCI1_AD[31:0]	Muxed Address / data	AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26	I/O	OV_{DD}	—
$\overline{\text{PCI1\_C\_BE[3:0]}}$	Command/Byte Enable	AD18, AD20,AD22, AH25	I/O	OV_{DD}	29
PCI1_PAR	Parity	AC22	I/O	OV_{DD}	29
$\overline{\text{PCI1\_FRAME}}$	Frame	AE20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_TRDY}}$	Target Ready	AF21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_IRDY}}$	Initiator Ready	AB20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_STOP}}$	Stop	AD21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_DEVSEL}}$	Device Select	AC21	I/O	OV_{DD}	2,29
PCI1_IDSEL	Init Device Select	AE16	I	OV_{DD}	29
$\overline{\text{PCI1\_PERR}}$	Parity Error	AB21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_SERR}}$	System Error	AF22	I/O	OV_{DD}	2,4,29
$\overline{\text{PCI1\_REQ}}$[4:3]/GPIO[1:0]	Request	AE15,Y15	I	OV_{DD}	—
$\overline{\text{PCI1\_REQ}}$[2:1]	Request	AF13,W16	I	OV_{DD}	29
$\overline{\text{PCI1\_REQ}}$[0]	Request	AA16	I/O	OV_{DD}	29
$\overline{\text{PCI1\_GNT}}$[4:3]/GPIO[3:2]	Grant	AC14, AA15	O	OV_{DD}	
$\overline{\text{PCI1\_GNT}}$[2:1]	Grant	AF14,Y16	O	OV_{DD}	5,9,25,29
$\overline{\text{PCI1\_GNT}}$[0]	Grant	W18	I/O	OV_{DD}	29
PCI1_CLK	PCI Clock	AH26	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
General-Purpose Input/Output					
GPIO[0:1]/PCI1_REQ[3:4]	GPIO/PCI request	Y15,AE15	I/O	OV_{DD}	—
GPIO[2:3]/PCI1_GNT[3:4]	GPIO/PCI grant	AA15,AC14	I/O	OV_{DD}	—
GPIO[4]/SDHC_CD	GPIO/SDHC card detection	AH11	I/O	OV_{DD}	—
GPIO[5]/SDHC_WP	GPIO/SDHC write protection	AG10	I/O	OV_{DD}	32
GPIO[6]/USB1_PCTL0	GPIO/USB1 PCTL0	AC3	I/O	OV_{DD}	—
GPIO[7]/USB1_PCTL1	GPIO/USB1 PCTL1	AC4	I/O	OV_{DD}	—
GPIO[8]/USB2_PCTL0	GPIO/USB2 PCTL0	AG9	I/O	OV_{DD}	—
GPIO[9]/USB2_PCTL1	GPIO/USB2 PCTL1	AC9	I/O	OV_{DD}	—
GPIO[10:11] /DMA_DACK[0:1]	GPIO/DMA Ack	AD6,AE10	I/O	OV_{DD}	—
GPIO[12:13] /DMA_DDONE[0:1]	GPIO/DMA done	AA11,AB11	I/O	OV_{DD}	—
GPIO[14:15] /DMA_DREQ[0:1]	GPIO/DMA request	AB10,AD11	I/O	OV_{DD}	—
System Control					
HRESET	Hard reset	AG16	I	OV_{DD}	—
HRESET_REQ	Hard reset - request	AG15	O	OV_{DD}	22
SRESET	Soft reset	AG19	I	OV_{DD}	—
CKSTP_IN	CheckStop in	AG18	I	OV_{DD}	—
CKSTP_OUT	CheckStop Output	AH17	O	OV_{DD}	2,4
Debug					
TRIG_IN	Trigger in	W19	I	OV_{DD}	—
TRIG_OUT/READY /QUIESCE	Trigger out/Ready/Quiesce	V19	O	OV_{DD}	22
MSRCID[0:1]	Memory debug source port ID	W12,W13	O	OV_{DD}	6,9
MSRCID[2:4]	Memory debug source port ID	V12, W14,W11	O	OV_{DD}	6,9,22
MDVAL	Memory debug data valid	V13	O	OV_{DD}	6,22
CLK_OUT	Clock Out	W15	O	OV_{DD}	11
Clock					
RTC	Real time clock	AF15	I	OV_{DD}	—
SYSCLK	System clock / PCI clock	AH14	I	OV_{DD}	—
DDRCLK	DDR clock	AC13	I	OV_{DD}	30
JTAG					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST\_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND	SerDes 1 Transceiver core logic GND (xcorevss)	M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28	—	—	—
X2GND	SerDes 2 Transceiver pad GND (xpadvss)	R12,M10,N11,L12	—	—	—
S2GND	SerDes 2 Transceiver core logic GND (xcorevss)	P8,P9,N6,M8	—	—	—
AGND_SRDS	SerDes 1 PLL GND	V27	—	—	—
AGND_SRDS2	SerDes 2 PLL GND	T2	—	—	—
SENSEVSS	GND Sensing	V16	—	—	13
Analog Signals					
MVREF	SSTL2 reference voltage	A28	Reference voltage for DDR	GVDD/2	—
SD1_IMP_CAL_RX	Rx impedance calibration	M26	—	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	Tx impedance calibration	AE28	—	100Ω (±1%) to GND	—
SD1_PLL_TPA	PLL test point analog	V26	—	AVDD_SRDS analog	18
SD2_IMP_CAL_RX	Rx impedance calibration	R7	—	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	Tx impedance calibration	L6	—	100Ω (±1%) to GND	—
SD2_PLL_TPA	PLL test point analog	T3	—	AVDD_SRDS2 analog	18
Reserved	—	R4	—	—	—
Reserved	—	R5	—	—	—
No Connect Pins					
NC	—	C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9	—	—	—

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	1.0 ± 50 mV	V	—
Platform supply voltage		V_{DD_PLAT}	1.0 ± 50 mV	V	—
PLL core supply voltage		AV_{DD_CORE}	1.0 ± 50 mV	V	2
PLL other supply voltage		AV_{DD}	1.0 ± 50 mV	V	2
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}	1.0 ± 50 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V ± 90 mV	V	3
	DDR3 SDRAM Interface		1.5 V ± 75 mV		
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	5
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	3.3 V ± 165 mV	V	4
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 and DDR3 SDRAM Interface reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	5
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	4
Operating Temperature range	Commercial	T_A T_J	T_A= 0 (min) to T_J= 90(max)	°C	6
	Industrial standard temperature range		T_A= 0 (min) to T_J= 105 (max)		
	Extended temperature range		T_A= -40 (min) to T_J= 105 (max)		

Notes:

2. This voltage is the input to the filter discussed in Section 3.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
3. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

2.9.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

The following tables describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) as depicted in Figure 30.

Table 39. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	$X2V_{DD}$	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$X2V_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$X2V_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Notes:

1. This will not align to DC-coupled SGMII. $X2V_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of the chip’s SerDes 2 control register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
   - 5.The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $X2V_{DD\text{-}Typ}$=1.0V, no common mode offset variation (VOS =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

2.9.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 31 shows the SGMII Receiver Input Compliance Mask eye diagram.

Table 42. SGMII Receive AC Timing Specifications

At recommended operating conditions with $X2V_{DD}$ = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the chip transmitter outputs.

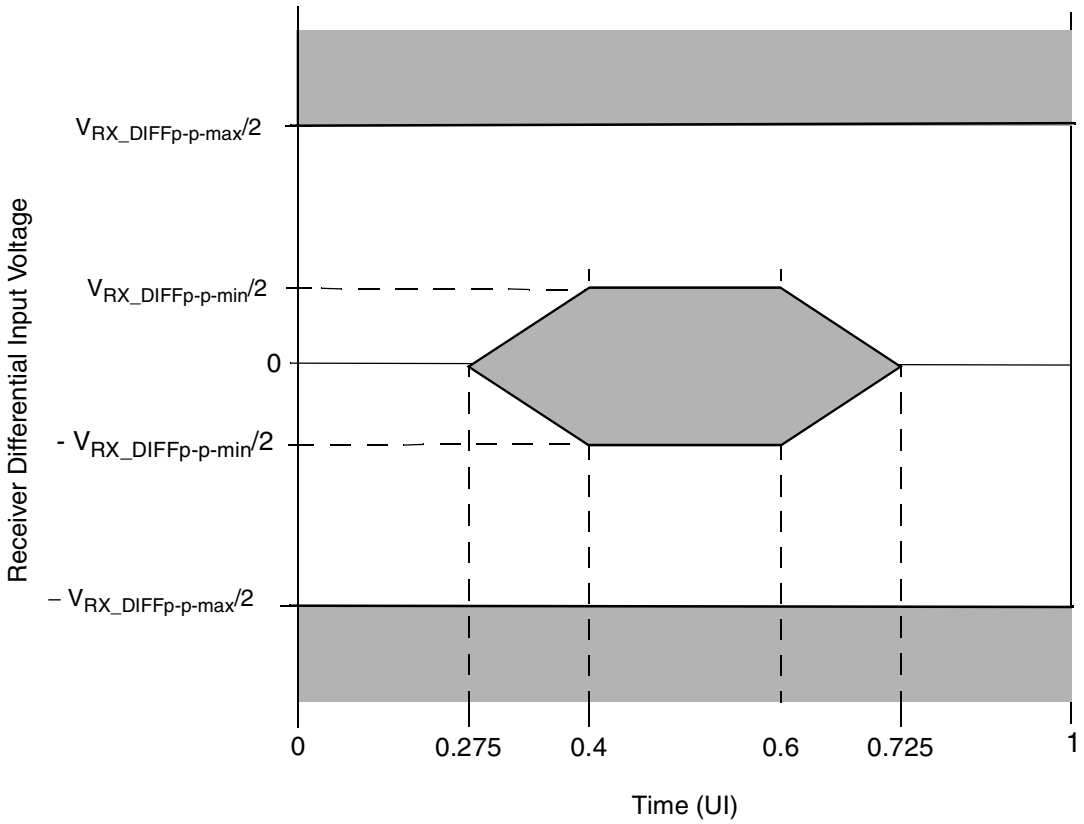


Figure 31. SGMII Receiver Input Compliance Mask

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDIO to EC_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
EC_MDC rise time	t_{MDCR}	—	—	10	ns	—
EC_MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. t_{CLKplb_clk} is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time t_{MDKHDX}. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

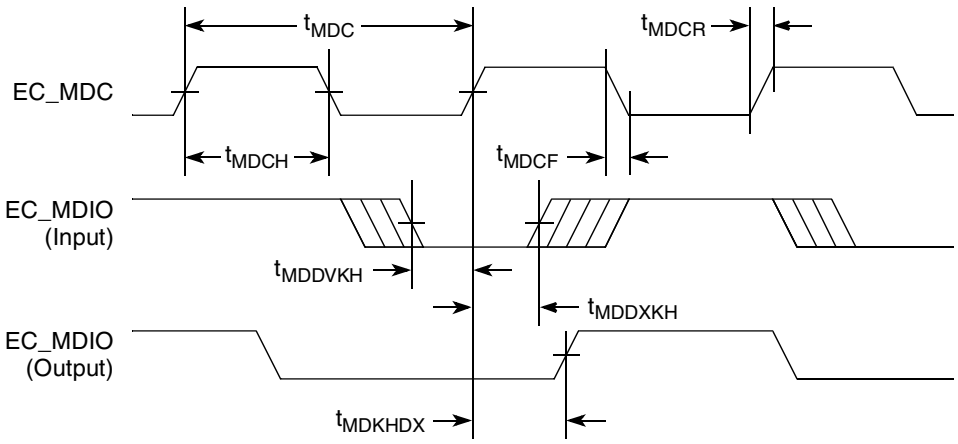


Figure 35. MII Management Interface Timing Diagram

2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC) (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V DC.

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	1.9	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.8	—	ns	3

This figure provides the eSDHC clock input timing diagram.

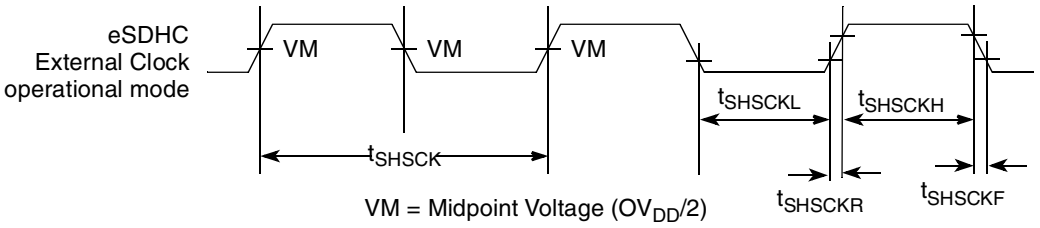


Figure 43. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

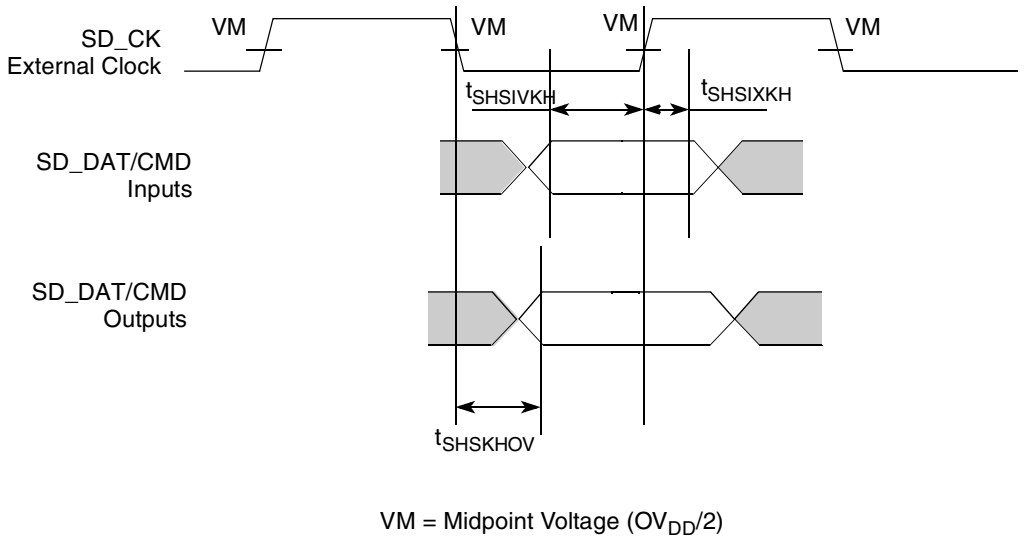


Figure 44. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.14 Programmable Interrupt Controller (PIC)

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

2.15 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

2.15.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Table 57. JTAG DC Electrical Characteristics

Parameter	Symbol [1]	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V

Table 68. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Failing time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 22, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.

This figure provides the AC test load for PCI.

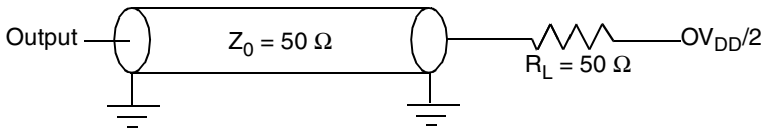


Figure 54. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

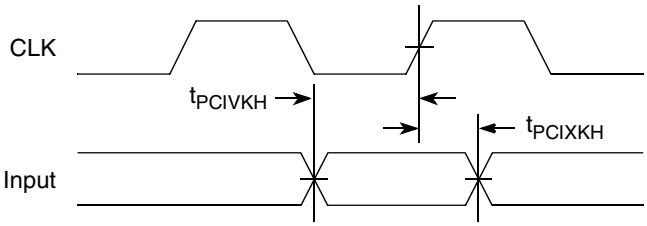


Figure 55. PCI Input AC Timing Measurement Conditions

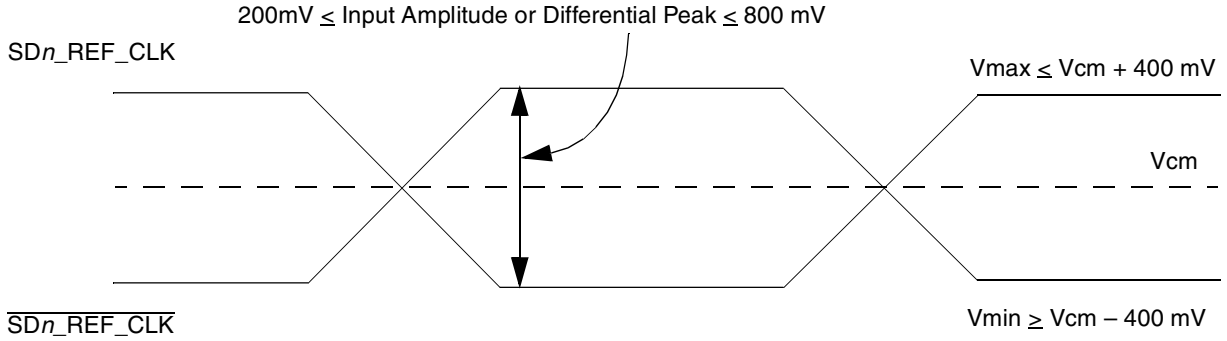


Figure 60. Differential Reference Clock Input DC Requirements (External AC-Coupled)

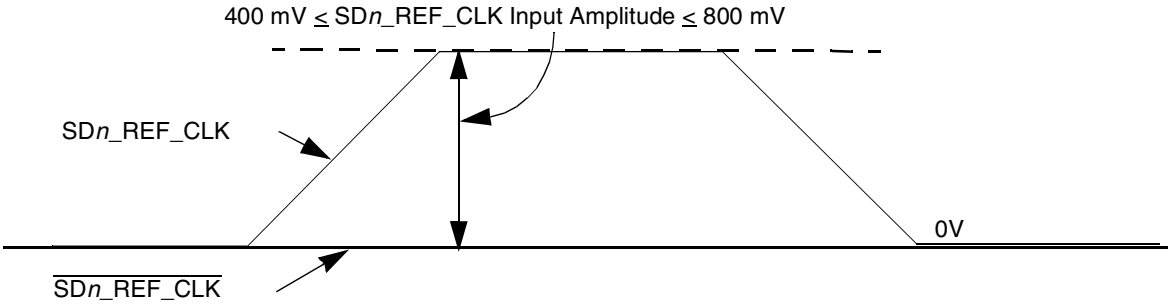


Figure 61. Single-Ended Reference Clock Input DC Requirements

2.20.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SnGND (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL (Low Voltage Positive Emitter-Coupled Logic) outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 62 to Figure 65 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the chip's SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with chip's SerDes reference clock input's DC requirement.

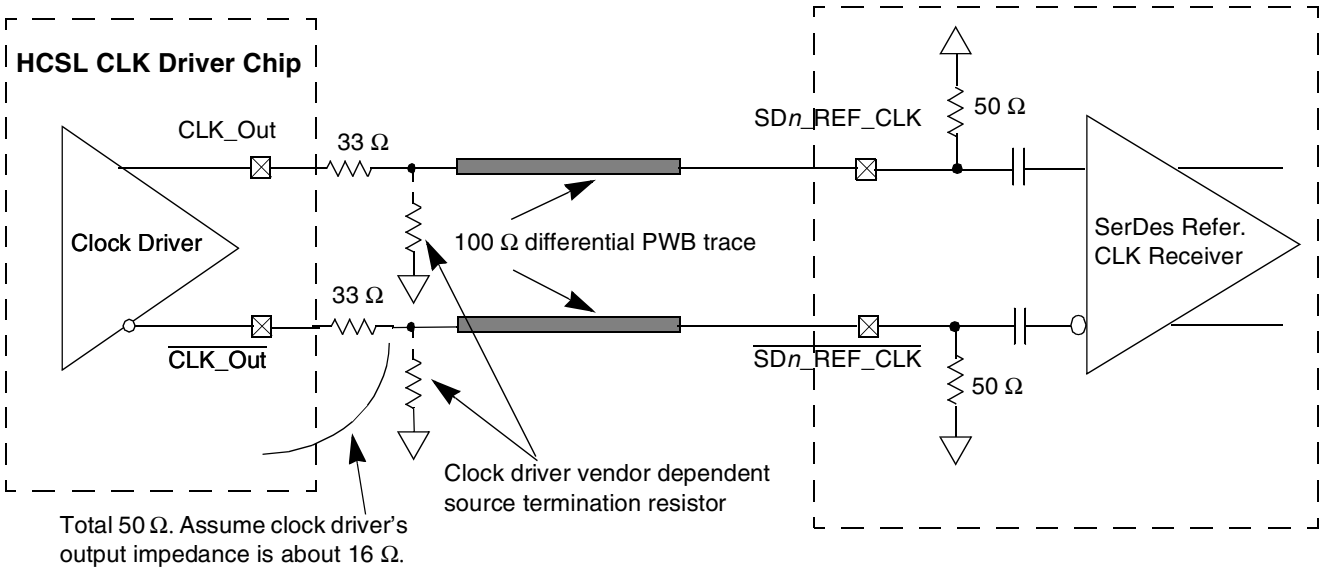


Figure 62. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the chip's SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

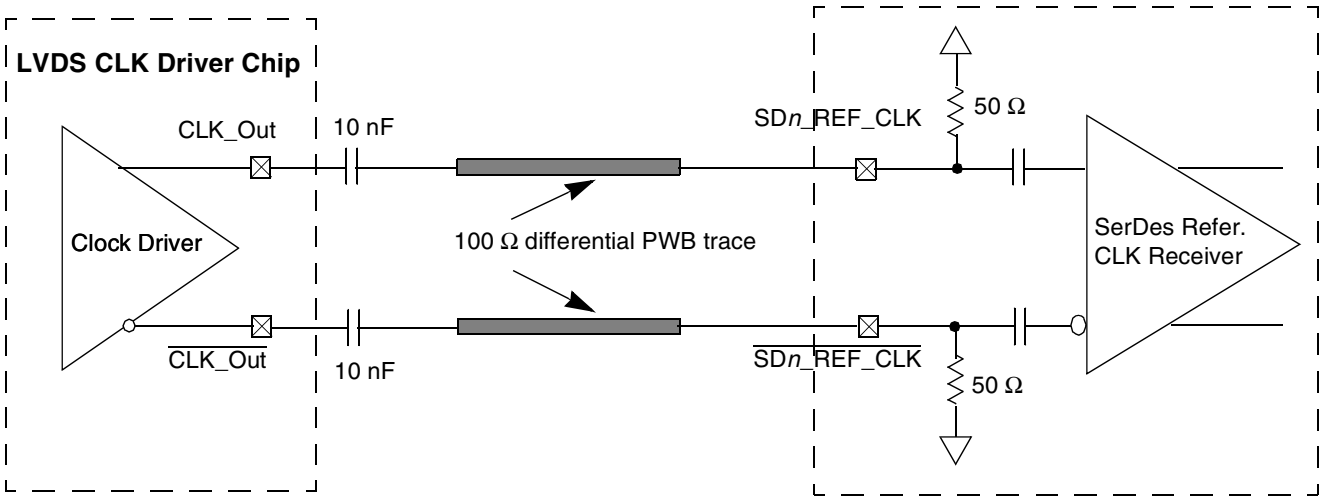


Figure 63. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Table 77. DDR Clock Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	cfg_ddr_pll[0:2]	000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

Table 79. Package Thermal Characteristics (continued)

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	< 0.1	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 •C/W

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.For system thermal modeling, the chip's thermal model without a lid is shown in Figure 72 The substrate is modeled as a block 29 x 29 x 1.2 mm with an in-plane conductivity of 19.8 W/m•K and a through-plane conductivity of 1.13 W/m•K. The solder balls and air are modeled as a single block 29 x 29 x 0.5 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 9.6 x 9.57 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 7.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

2.24.2 Recommended Thermal Model

This table shows the chip's thermal model.

Table 80. Thermal Model

Conductivity	Value	Units
Die (9.6x9.6 × 0.85 mm)		
Silicon	Temperature dependent	—
Bump/Underfill (9.6 x 9.6 × 0.07 mm) Collapsed Thermal Resistance		
Kz	7.5	W/m•K
Substrate (29 × 29 × 1.2 mm)		
Kx	19.8	W/m•K
Ky	19.8	
Kz	1.13	
Solder and Air (29 × 29 × 0.5 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	

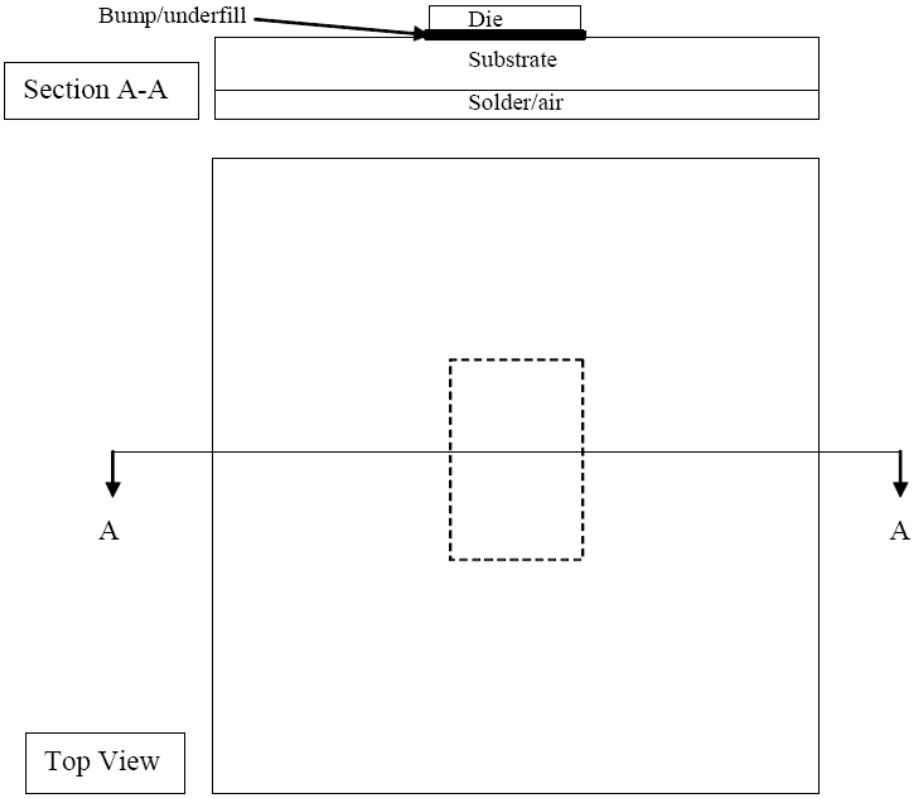


Figure 72. System-Level Thermal Model for the Chip (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

2.24.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values types and quantity of bulk capacitors.

3.5 SerDes Block Power Supply Decoupling Recommendations

he SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power (SnV_{DD} and XnV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the chip. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the chip as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (SnV_{DD} and XnV_{DD}) to the board ground plane on each side of the chip. This should be done for all SerDes supplies.
- Third, between the chip and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND pins of the chip.

3.7 Pull-Up and Pull-Down Resistor Requirements

The chip requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

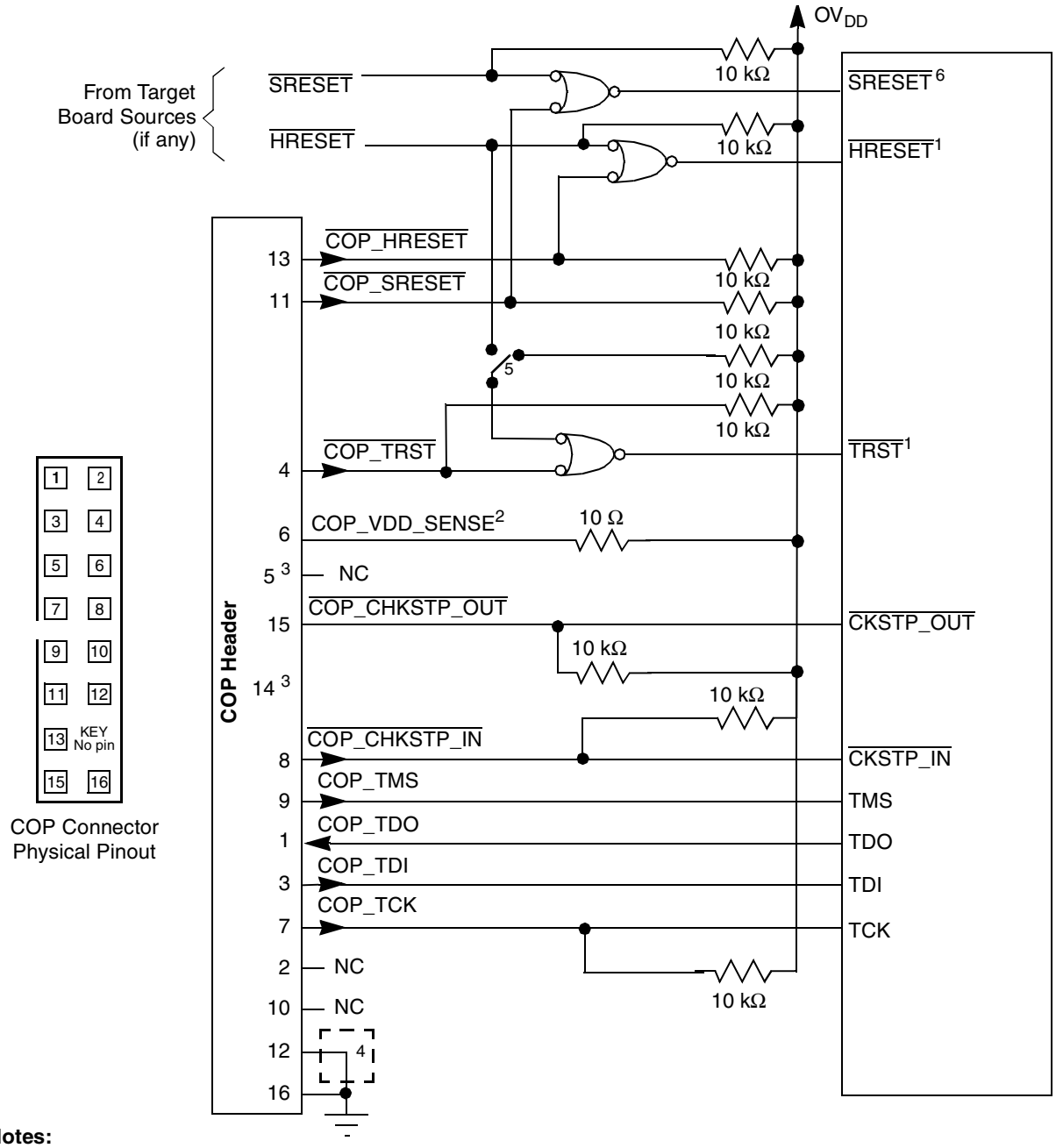
Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC1_TXD[3], $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The UART_SOUT[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. Please refer to the pinlist table (see Table 62) of the individual chip for more details.

See the PCI 2.2 specification for all pull-ups required for PCI.

3.8 Output Buffer DC Impedance

The chip drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 78. JTAG Interface Connection

4.1 Part Numbers Fully Addressed by this Document

This table shows the part numbering nomenclature.

Table 82. Part Numbering Nomenclature

MPC	*nnnn*	*E*	*C*	*VT*	*AA*	*X*	*R*
Product Code	**Part Identifier**	**Security Engine**	**Tiers and Temperature Range**	**Package [1]**	**Processor Frequency [2]**	**DDR Frequency [3]**	**Revision Level**
MPC	8536 8535	E = included	• A = Commercial tier standard temperature range (0° to 90°C) • B or Blank = industrial tier standard temperature range (0° to 105°C) • C = Industrial tier extended temperature range (–40° to 105°C)	• VT = FC-PBGA • (Pb-free) • PX = plastic standard	• AK = 600 MHz • AN = 800 MHz • AQ = 1000 MHz • AT = 1250 MHz • AU = 1333 MHz • AV = 1500 MHz	• G = 400 MHz • H = 500 MHz • J = 533 MHz • L = 667 MHz	• Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0190, 0x803F0191) • A = Ver. 1.2 (SVR = 0x803F0192)
		Blank = not included					• Blank = Ver. 1.0 or 1.1 (SVR = 0x80370190, 0x80370191) • A = Ver. 1.2 (SVR = 0x80370192)

Notes:

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.

5 Package Information

This section details package parameters, pin assignments, and dimensions.

5.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA) without a lid.

Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	2.23 mm
Maximum module height	2.8 mm
Solder Balls	96.5Sn/3.5Ag
Ball diameter (typical)	0.6 mm