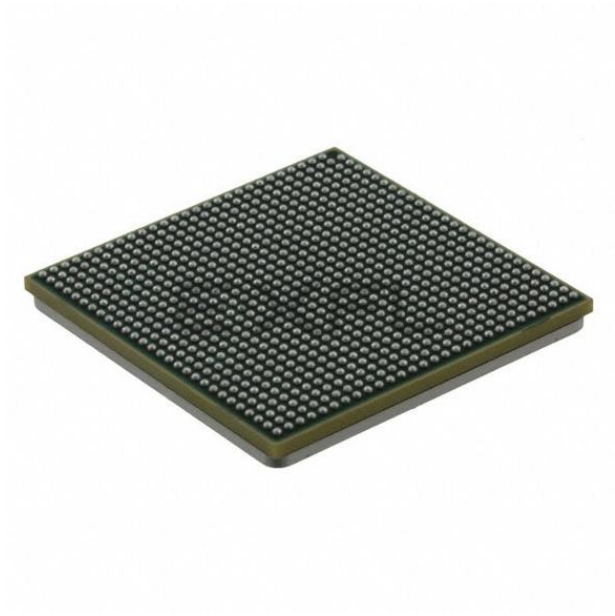

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8536avjavla

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals may be listed only once and may not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled-high.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD_CORE}/V_{DD_PLAT}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
17. This pin is only an output in FIFO mode when used as Rx Flow Control.
18. Do not connect.
19. These must be pulled up (100 Ω- 1 kΩ) to OVDD.
20. Independent supplies derived from board VDD.
21. Recommend a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD}.
22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.
23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
24. General-Purpose POR configuration of user system.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	–0.3 to 1.21	V	—
Platform supply voltage		V_{DD_PLAT}	–0.3 to 1.1	V	—
PLL core supply voltage		AV_{DD_CORE}	–0.3 to 1.21	V	—
PLL other supply voltage		AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers		SV_{DD}, $S2V_{DD}$	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}, $X2V_{DD}$	–0.3 to 1.1	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface		–0.3 to 1.65		
Three-speed Ethernet I/O		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	2
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	2
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	^0C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.
2. The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

This figure provides the AC test load for the DDR bus.

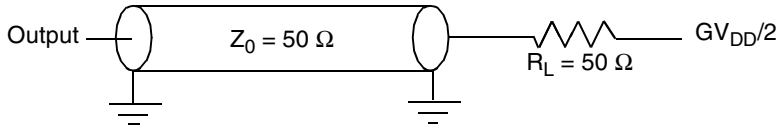

Figure 11. DDR AC Test Load

2.7 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the chip.

2.7.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the chip eSPI.

Table 20. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

2.7.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

Table 21. SPI AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_MOSI output—Master data hold time	t_{NIKHOX}	0.5	—	ns	3
	t_{NIKHOX}	4.0			4
SPI_MOSI output—Master data delay	t_{NIKHOV}	—	6.0	ns	3
	t_{NIKHOV}		7.4		4
SPI_CS outputs—Master data hold time	$t_{NIKHOX2}$	0	—	ns	—

2.9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps) — FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 2.10, "Ethernet Management Interface Electrical Characteristics."

The electrical characteristics for SGMII is specified in Section 2.9.3, "SGMII Interface Electrical Characteristics." The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

2.9.1.1 GMII, MII, TBI, RGMII, RMII and RTBI DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in the following tables. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	1.90	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	3

Notes:

1 LV_{DD} supports eTSECs 1.

2 TV_{DD} supports eTSECs 3.

3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

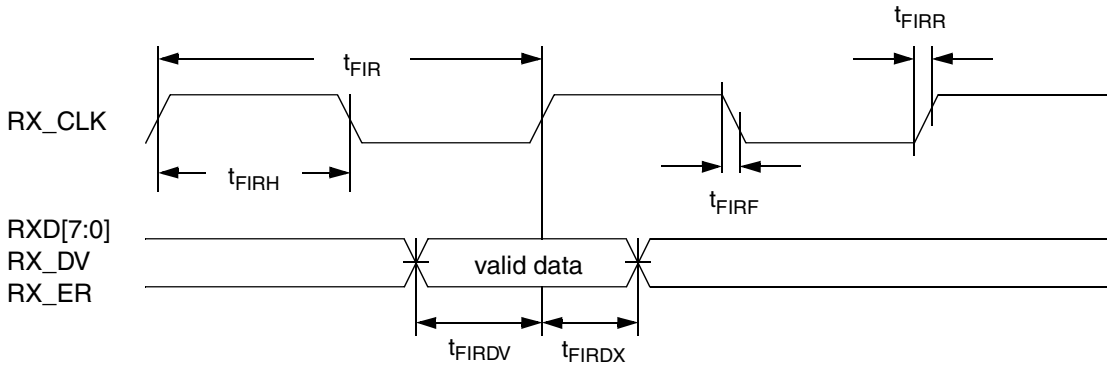

Figure 15. FIFO Receive AC Timing Diagram

2.9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

2.9.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 28. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTK}	—	8.0	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}[3]	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}	—	—	1.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{GTKHDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the GMII receive AC timing diagram.

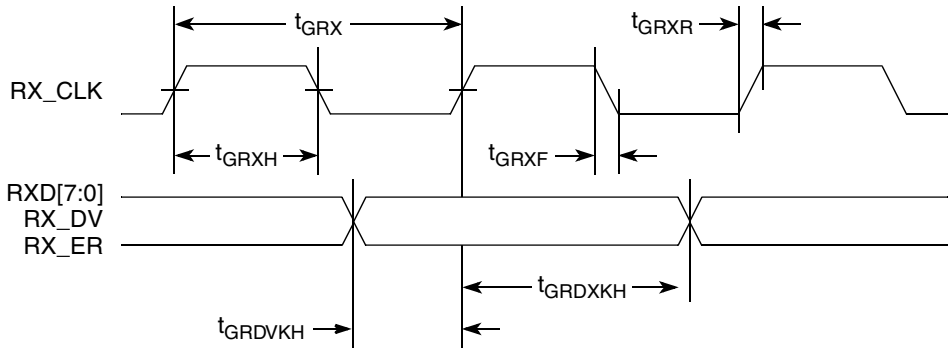

Figure 18. GMII Receive AC Timing Diagram

2.9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.9.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 30. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII receive AC timing diagram.

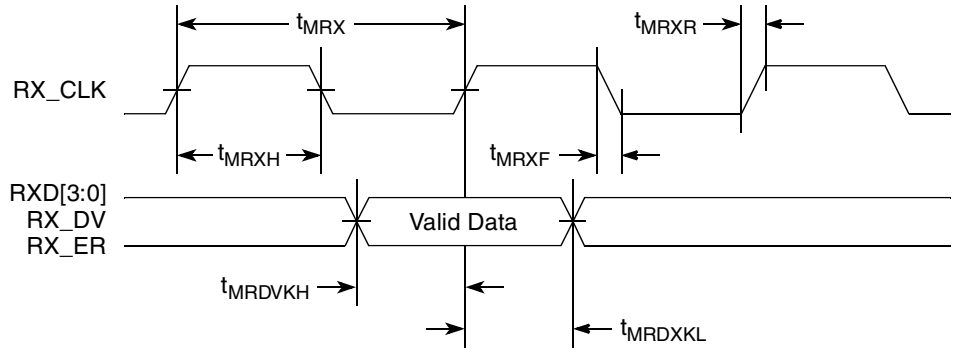

Figure 21. MII Receive AC Timing Diagram

2.9.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

2.9.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}[2]	1.0	—	5.0	ns
GTX_CLK rise (20%–80%)	t_{TTXR}	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{TTKHDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the TBI transmit AC timing diagram.

This figure shows the TBI receive AC timing diagram.

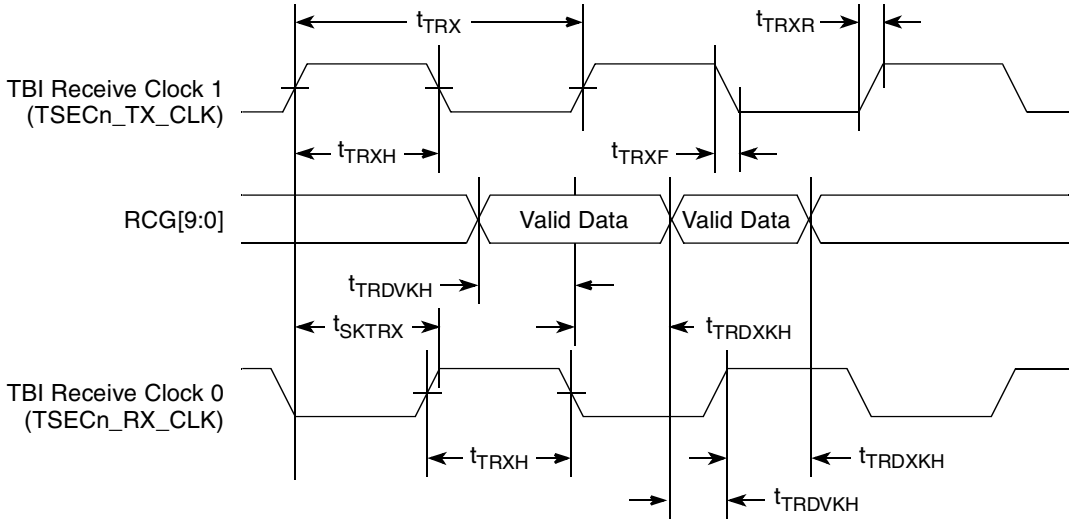

Figure 23. TBI Receive AC Timing Diagram

2.9.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used on in this mode, whereas for the dual-clock mode this is the PMA0 receive clock). The 125-MHz transmit clock is applied on the in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in the following table.

Table 34. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns

This figures show the local bus signals.

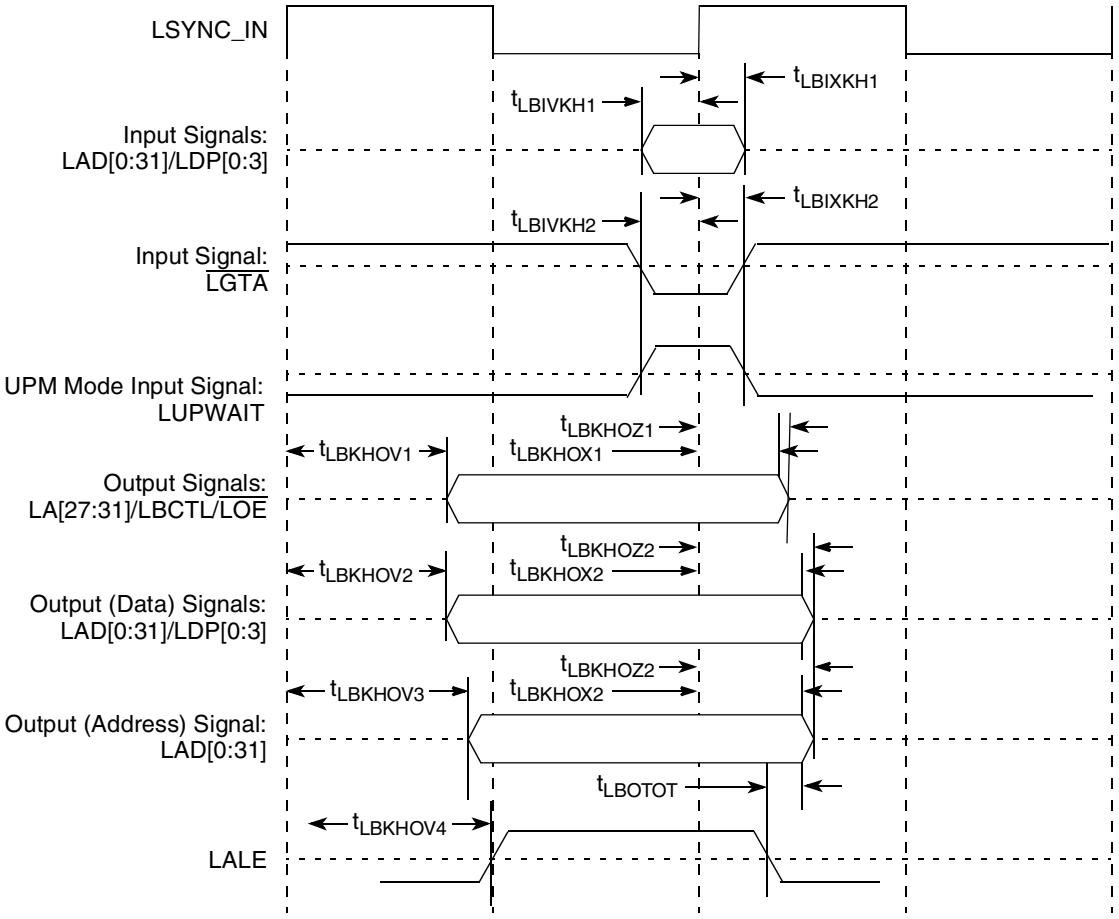

Figure 39. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

NOTE

In PLL bypass mode, some signals are launched and captured on the opposite edge of LCLK[n] to that used in PLL Enable Mode. In this mode, output signals are launched at the falling edge of the LCLK[n] and inputs signals are captured at the rising edge of LCLK[n] with the exception of LGTA/LUPWAIT (which is captured at the falling edge of the LCLK[n]).

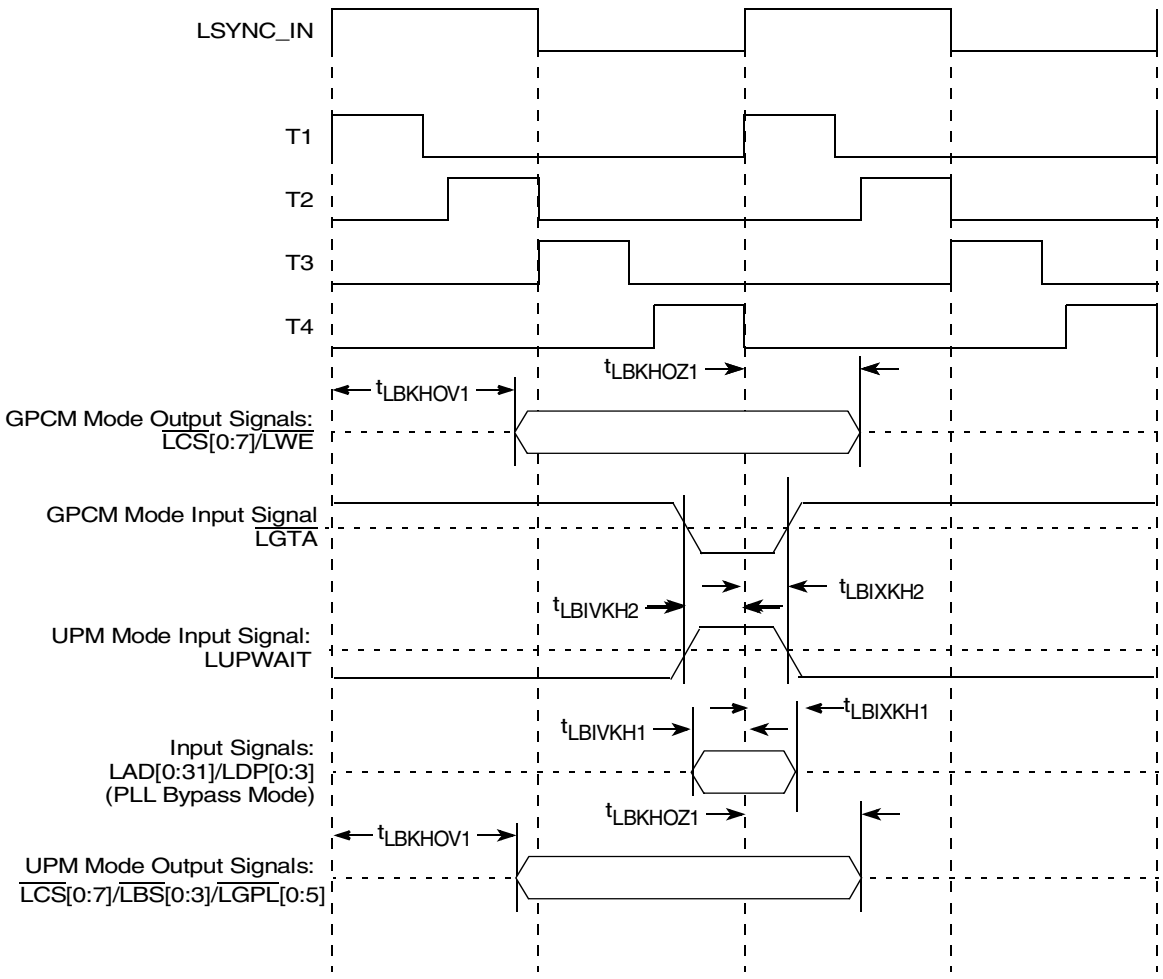

Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 * OVDD	OVDD+0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.25 * OVDD	V	—
Input/Output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—
Output high voltage	V_{OH}	I_{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	—

Table 60. Differential Transmitter (TX) Output Characteristics (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
TX Common Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXCC11}	 — — — — — —	 — — — — — —	 5 5 2 2 1 1	 dB	 1, 2
TX Impedance Balance 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_TXDC11}	 — — — — — —	 — — — — — —	 30 20 10 10 4 4	 dB	 1, 2
Deterministic jitter 1.5G 3.0G	U_{SATA_TXDJ}	—	—	 0.18 0.14	 UI	—
Total Jitter 1.5G 3.0G	U_{SATA_TXTJ}	—	—	 0.42 0.32	 UI	—

Notes:
1. Only applies when operating in 3.0Gb data rate mode.
2. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
3. Only applies to Gen1i mode.

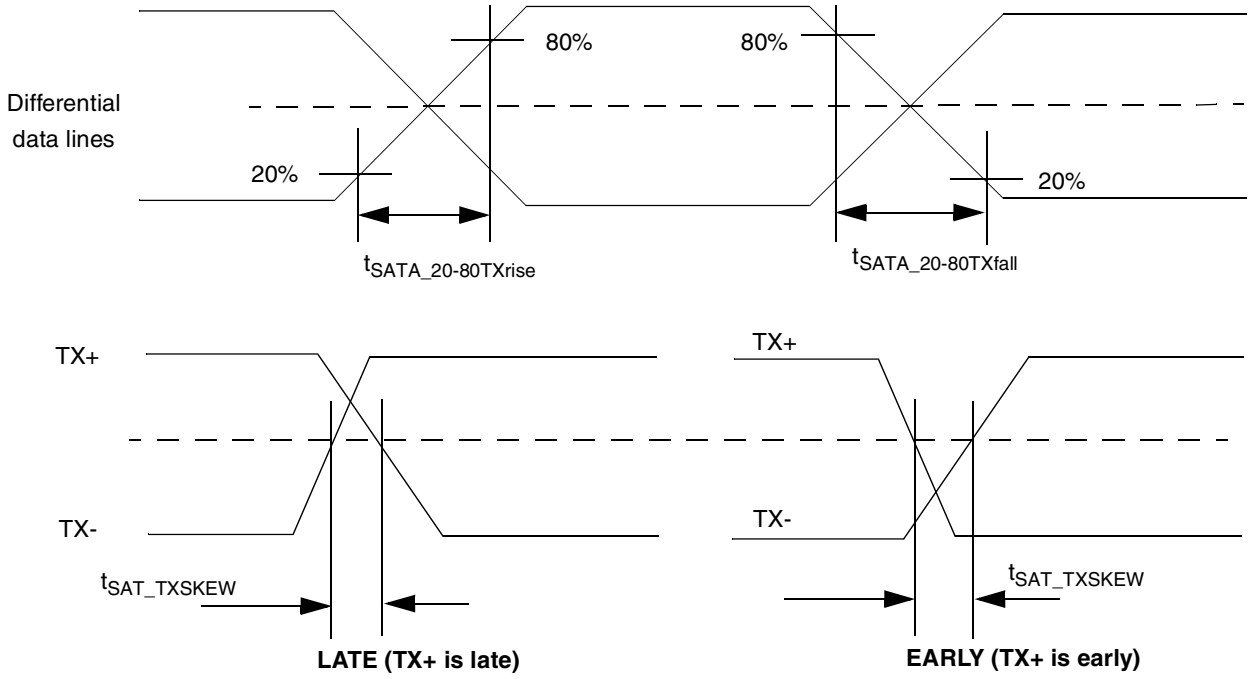

Figure 50. Signal Rise and Fall Times and Differential Skew

2.16.3 Differential Receiver (RX) Input Characteristics

This table provides the differential receiver (RX) input characteristics for the SATA interface.

Table 61. Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
RX Differential Input Voltage 1.5G 3.0G	V_{SATA_RXDIFF}	 240 240	 400 —	 600 750	mVp-p	1
RX rise/fall time 1.5G 3.0G	$t_{SATA\_20\text{-}80RX}$	100 67	— —	273 136	ps	—
RX Differential skew 1.5G 3.0G	t_{SATA_RXSKEW}	— —	— —	— 50	ps	—
RX Differential pair impedance 1.5G	$Z_{SATA\_RXDIFFIM}$	85	—	115	ohm	—
RX Single-Ended impedance 1.5G	Z_{SATA_RXSEIM}	40	—	—	ohm	—
DC Coupled Common Mode Voltage	V_{dc_cm}	200	250	450	mV	5

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 65. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	7.5	ns	3
GPIO outputs—minimum pulse width	t_{GTOWID}	12	ns	—

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

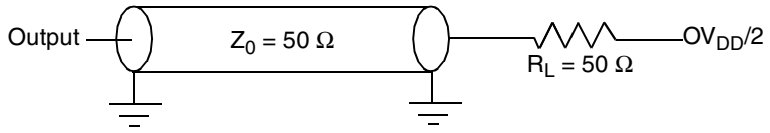

Figure 53. GPIO AC Test Load

2.19 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

2.19.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 67. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.19.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. This table provides the PCI AC timing specifications at 66 MHz.

Table 68. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 5
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7

Table 68. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Failing time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 22, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.

This figure provides the AC test load for PCI.

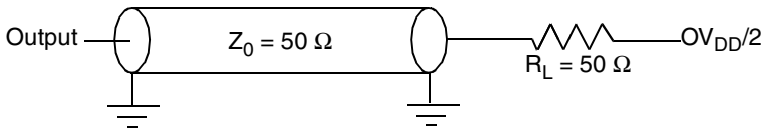

Figure 54. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

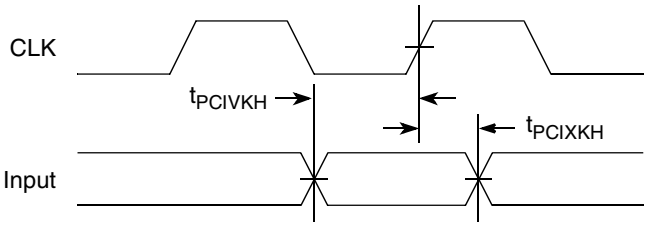

Figure 55. PCI Input AC Timing Measurement Conditions

— The external reference clock driver must be able to drive this termination.
— The SerDes reference clock input can be either differential or single-ended. See the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1V above SnGND (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800mV with the common mode voltage at 400mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SnGND (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

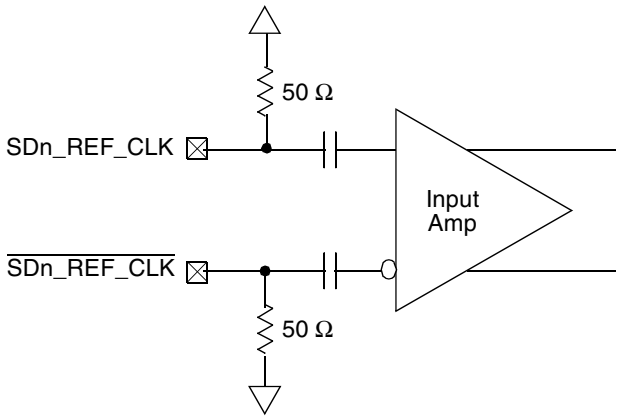

Figure 58. Receiver of SerDes Reference Clocks

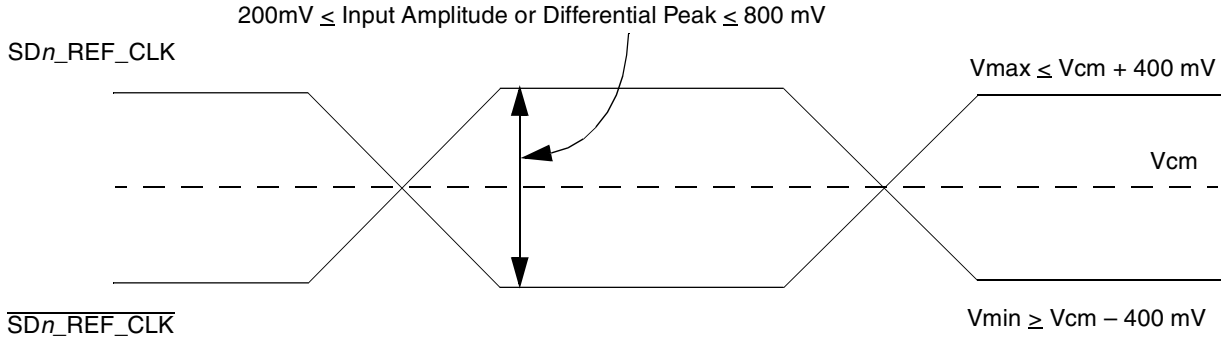

Figure 60. Differential Reference Clock Input DC Requirements (External AC-Coupled)

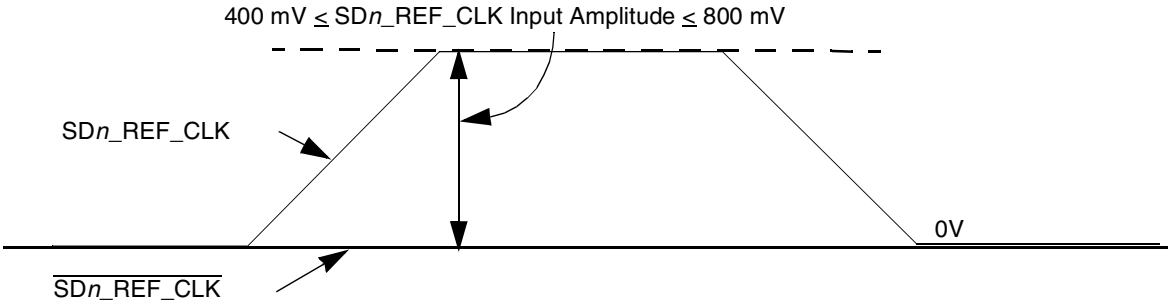

Figure 61. Single-Ended Reference Clock Input DC Requirements

2.20.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SnGND (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL (Low Voltage Positive Emitter-Coupled Logic) outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 62 to Figure 65 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the chip's SerDes reference clock receiver requirement provided in this document.

2.20.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 69. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.0V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 66.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 67.

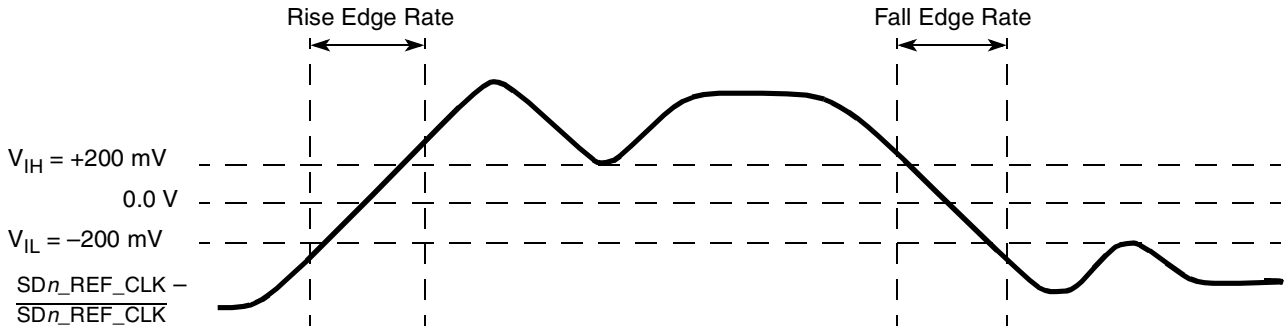

Figure 66. Differential Measurement Points for Rise and Fall Time

2.23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in the following table:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 75. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	Reserved	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

2.23.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in this table.

Table 76. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

2.23.4 DDR/DDRCLK PLL Ratio

The DDR memory controller complex can be synchronous with, or asynchronous to, the CCB, depending on configuration.

The following table describes the clock ratio between the DDR memory controller complex and the DDR/DDRCLK PLL reference clock, DDRCLK, which is not the memory bus clock.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for the DDR controller to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 77 reflects the DDR data rate to DDRCLK ratio, since the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, “CCB/SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, “e500 Core PLL Ratio.”
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, “DDR/DDRCLK PLL Ratio.”

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.