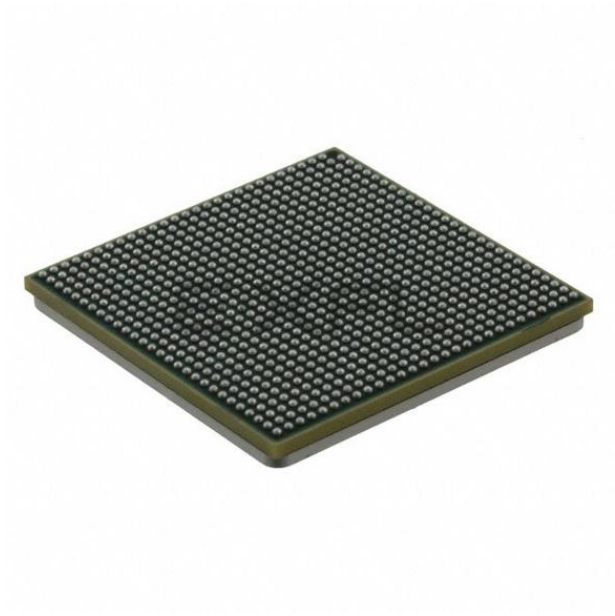

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 600MHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | SATA 3Gbps (2) |
| USB | USB 2.0 (3) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 90°C (TA) |
| Security Features | Cryptography |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8536eavjakga |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| DMA_DREQ[0:1] /GPIO[14:15] | DMA Request | AB10,AD11 | I | $OV_{DD}$ | — |
| DMA_DDONE[0:1] /GPIO[12:13] | DMA Done | AA11,AB11 | O | $OV_{DD}$ | — |
| DMA_DREQ[2]/LCS[5] | Chips selects / DMA Request | H16 | I/O | $BV_{DD}$ | 1,29 |
| DMA_DACK[2]/LCS[6] | Chips selects / DMA Ack | J16 | O | $BV_{DD}$ | 1,29 |
| DMA_DDONE[2]/LCS[7] | Chips selects / DMA Done | L18 | O | $BV_{DD}$ | 1,29 |
| DMA_DREQ[3]/IRQ[9] | External interrupt/DMA request | AE13 | I | $OV_{DD}$ | 1 |
| DMA_DACK[3]/IRQ[10] | External interrupt/DMA Ack | AD13 | I/O | $OV_{DD}$ | 1 |
| DMA_DDONE[3]/IRQ[11] | External interrupt/DMA done | AD14 | I/O | $OV_{DD}$ | 1 |
| **USB Port 1** | | | | | |
| USB1_D[7:0] | USB1 Data bits | AF1,AE2,AE1,AD2, AC2,AC1,AB2,AB1 | I/O | $OV_{DD}$ | — |
| USB1_NXT | USB1 Next data | AF2 | I | $OV_{DD}$ | — |
| USB1_DIR | USB1 Data Direction | AH1 | I | $OV_{DD}$ | — |
| USB1_STP | USB1 Stop | AG1 | O | $OV_{DD}$ | 5,9 |
| USB1_PWRFAULT | USB1 bus power fault. | AH2 | I | $OV_{DD}$ | — |
| USB1_PCTL0/GPIO[6] | USB1 Port control 0 | AC3 | O | $OV_{DD}$ | — |
| USB1_PCTL1/GPIO[7] | USB1 Port control 1 | AC4 | O | $OV_{DD}$ | — |
| USB1_CLK | USB1 bus clock | AD1 | I | $OV_{DD}$ | — |
| **USB Port 2** | | | | | |
| USB2_D[7:0] | USB2 Data bits | AE6,AC6,AF5,AE5, AF4,AE4,AE3,AD3 | I/O | $OV_{DD}$ | — |
| USB2_NXT | USB2 Next data | AC7 | I | $OV_{DD}$ | — |
| USB2_DIR | USB2 Data Direction | AF7 | I | $OV_{DD}$ | — |
| USB2_STP | USB2 Stop | AD7 | O | $OV_{DD}$ | 5,9 |
| USB2_PWRFAULT | USB2 bus power fault. | AC8 | I | $OV_{DD}$ | — |
| USB2_PCTL0/GPIO[8] | USB2 Port control 0 | AG9 | O | $OV_{DD}$ | — |
| USB2_PCTL1/GPIO[9] | USB2 Port control 1 | AC9 | O | $OV_{DD}$ | — |
| USB2_CLK | USB2 bus clock | AD5 | I | $OV_{DD}$ | — |
| — | | | | | |
| Reserved | — | AH8 | — | — | — |
| Reserved | — | AH7,AG6,AH6,AG5, AG4,AH4,AG3,AH3, AG7, AG8, AH9,AH5 | — | — | 27 |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|

**Notes:**

1. All multiplexed signals may be listed only once and may not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to $OV_{DD}$.
3. This pin must always be pulled-high.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the $V_{DD\_CORE}$/$V_{DD\_PLAT}$/GND planes internally and may be used by the core power supply to improve tracking and regulation.
15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
17. This pin is only an output in FIFO mode when used as Rx Flow Control.
18. Do not connect.
19. These must be pulled up (100 Ω- 1 kΩ) to OVDD.
20. Independent supplies derived from board VDD.
21. Recommend a pull-up resistor (1 KΩ) be placed on this pin to $OV_{DD}$.
22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.
23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
24. General-Purpose POR configuration of user system.

## 2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

**Table 2. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD\_CORE}$ | –0.3 to 1.21 | V | — |
| Platform supply voltage | | $V_{DD\_PLAT}$ | –0.3 to 1.1 | V | — |
| PLL core supply voltage | | $AV_{DD\_CORE}$ | –0.3 to 1.21 | V | — |
| PLL other supply voltage | | $AV_{DD}$ | –0.3 to 1.1 | V | — |
| Core power supply for SerDes transceivers | | $SV_{DD}$, $S2V_{DD}$ | –0.3 to 1.1 | V | — |
| Pad power supply for SerDes transceivers and PCI Express | | $XV_{DD}$, $X2V_{DD}$ | –0.3 to 1.1 | V | — |
| DDR SDRAM Controller I/O supply voltage | DDR2 SDRAM Interface | $GV_{DD}$ | –0.3 to 1.98 | V | — |
| | DDR3 SDRAM Interface | | –0.3 to 1.65 | | |
| Three-speed Ethernet I/O | | $LV_{DD}$ (eTSEC1) | –0.3 to 3.63<br>–0.3 to 2.75 | V | 2 |
| | | $TV_{DD}$ (eTSEC3) | –0.3 to 3.63<br>–0.3 to 2.75 | V | 2 |
| PCI, DUART, system control and power management, $I^2C$, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | — |
| Local bus I/O voltage | | $BV_{DD}$ | –0.3 to 3.63<br>–0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Input voltage | DDR2/DDR3 DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 3 |
| | DDR2/DDR3 DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3)<br>–0.3 to ($TV_{DD}$ + 0.3) | V | 3 |
| | Local bus signals | $BV_{IN}$ | –0.3 to ($BV_{DD}$ + 0.3) | — | — |
| | PCI, DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | $^0C$ | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.
2. The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
3. (M,L,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

## 2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

# 2.4 Input Clocks

## 2.4.1 System Clock Timing

This table provides the system clock (SYSCLK) AC timing specifications for the chip.

**Table 6. SYSCLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 33 | — | 133 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 7.5 | — | 30 | ns | — |
| SYSCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 2.1 | ns | 2 |
| SYSCLK duty cycle | $t_{KHK}/t_{SYSCLK}$ | 40 | — | 60 | % | — |
| SYSCLK jitter | — | — | — | +/-150 | ps | 3, 4 |

**Notes:**
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," and Section 2.23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 KHz and 60 KHz on SYSCLK.

## 2.4.2 PCI Clock Timing

When the PCI controller is configured for asynchronous operation, the reference clock for the PCI controller is not the SYSCLK input, but instead the PCI_CLK. This table provides the PCI reference clock AC timing specifications for the chip.

**Table 7. PCICLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| PCICLK frequency | $f_{PCICLK}$ | 33 | — | 66 | MHz | — |
| PCICLK cycle time | $t_{PCICLK}$ | 15 | — | 30 | ns | — |
| PCICLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 2.1 | ns | 1 |
| PCICLK duty cycle | $t_{KHK}/t_{PCICLK}$ | 40 | — | 60 | % | — |

**Notes:**
1. Rise and fall times for PCICLK are measured at 0.6 V and 2.7 V.

## 2.4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

## 2.4.4 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the chip.

**Table 8. EC_GTX_CLK125 AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $f_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC_GTX_CLK rise and fall time<br>$LV_{DD}$, $TV_{DD}$ = 2.5V<br>$LV_{DD}$, $TV_{DD}$ = 3.3V | $t_{G125R}/t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2 |

**Notes:**

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TVDD=2.5V, and from 0.6 and 2.7V for L/TVDD=3.3V at 0.6 V and 2.7 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.9.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

## 2.4.5 DDR Clock Timing

This table provides the DDR clock (DDRCLK) AC timing specifications for the chip.

**Table 9. DDRCLK AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3V ± 5%.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| DDRCLK frequency | $f_{DDRCLK}$ | 66 | — | 166 | MHz | 1 |
| DDRCLK cycle time | $t_{DDRCLK}$ | 6.0 | — | 15.15 | ns | — |
| DDRCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| DDRCLK duty cycle | $t_{KHK}/t_{DDRCLK}$ | 40 | — | 60 | % | — |
| DDRCLK jitter | — | — | — | +/– 150 | ps | 3, 4 |

**Notes:**

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. See Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

## 2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

### 2.8.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 22. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | – 0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**

1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 2.8.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 23. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | CCB clock/1,048,576 | baud | 2 |
| Maximum baud rate | CCB clock/16 | baud | 2,3 |
| Oversample rate | 16 | — | 4 |

**Notes:**

2. CCB clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the $8^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each $16^{th}$ sample.

## 2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

This figure shows the TBI receive AC timing diagram.

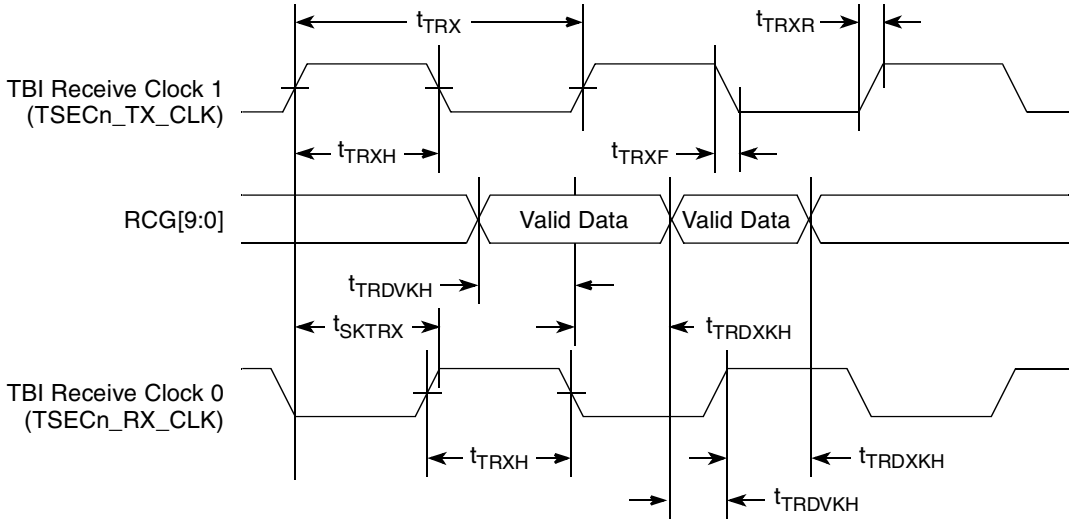



**Figure 23. TBI Receive AC Timing Diagram**

## 2.9.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used on in this mode, whereas for the dual-clock mode this is the PMA0 receive clock). The 125-MHz transmit clock is applied on the  in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in the following table.

**Table 34. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRR}$ | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDV}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDX}$ | 1.0 | — | — | ns |

**Table 36. RMII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise time TSECn_TX_CLK (20%–80%) | $t_{RMTR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSECn_TX_CLK (80%–20%) | $t_{RMTF}$ | 1.0 | — | 2.0 | ns |
| TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 2.0 | — | 10.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

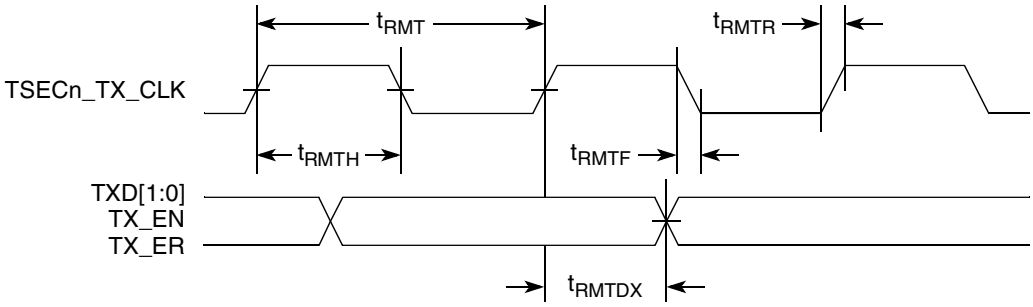



**Figure 26. RMII Transmit AC Timing Diagram**

## 2.9.2.7.2 RMII Receive AC Timing Specifications

**Table 37. RMII Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_RX_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns |
| TSECn_RX_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % |
| TSECn_RX_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time TSECn_RX_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns |

### 2.9.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

The following tables describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) as depicted in Figure 30.

**Table 39. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $X2V_{DD}$ | 0.95 | 1.0 | 1.05 | V | — |
| Output high voltage | VOH | — | — | $X2V_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$ | mV | 1 |
| Output low voltage | VOL | $X2V_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$ | — | — | mV | 1 |
| Output ringing | $V_{RING}$ | — | — | 10 | % | — |
| Output differential voltage[2, 3, 5] | $\lvert V_{OD}\rvert$ | 323 | 500 | 725 | mV | Equalization setting: 1.0x |
| | | 296 | 459 | 665 | | Equalization setting: 1.09x |
| | | 269 | 417 | 604 | | Equalization setting: 1.2x |
| | | 243 | 376 | 545 | | Equalization setting: 1.33x |
| | | 215 | 333 | 483 | | Equalization setting: 1.5x |
| | | 189 | 292 | 424 | | Equalization setting: 1.71x |
| | | 162 | 250 | 362 | | Equalization setting: 2.0x |
| Output offset voltage | $V_{OS}$ | 425 | 500 | 575 | mV | 1, 4 |
| Output impedance (single-ended) | $R_O$ | 40 | — | 60 | Ω | — |
| Mismatch in a pair | $\Delta R_O$ | — | — | 10 | % | — |
| Change in $V_{OD}$ between “0” and “1” | $\Delta \lvert V_{OD}\rvert$ | — | — | 25 | mV | — |
| Change in $V_{OS}$ between “0” and “1” | $\Delta V_{OS}$ | — | — | 25 | mV | — |
| Output current on short to GND | $I_{SA}$, $I_{SB}$ | — | — | 40 | mA | — |

**Notes:**

1. This will not align to DC-coupled SGMII. $X2V_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of the chip’s SerDes 2 control register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. $V_{OS}$ is also referred to as output common mode voltage.
   - 5.The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $X2V_{DD\text{-}Typ}$=1.0V, no common mode offset variation (VOS =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

## 2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

**Table 59. Reference Clock Input Requirements**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SD2_REF_CLK/_B reference clock cycle time | $t_{CLK\_REF}$ | 100 | — | 150 | MHz | 1 |
| SD2_REF_CLK/_B frequency tolerance | $t_{CLK\_TOL}$ | –350 | 0 | +350 | ppm | — |
| SD_REF_CLK/_B rise/fall time (80%-20%) | $t_{CLK\_RISE}/t_{CLK\_FALL}$ | — | — | 1 | ns | — |
| SD_REF_CLK/_B duty cycle (@50% X2VDD) | $t_{CLK\_DUTY}$ | 45 | 50 | 55 | % | — |
| SD_REF_CLK/_B cycle to cycle clock jitter (period jitter) | $t_{CLK\_CJ}$ | — | — | 100 | ps | — |
| SD_REF_CLK/_B phase jitter (peak-to-peak) | $t_{CLK\_PJ}$ | –50 | — | +50 | ps | 2,3 |

**Note:**

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

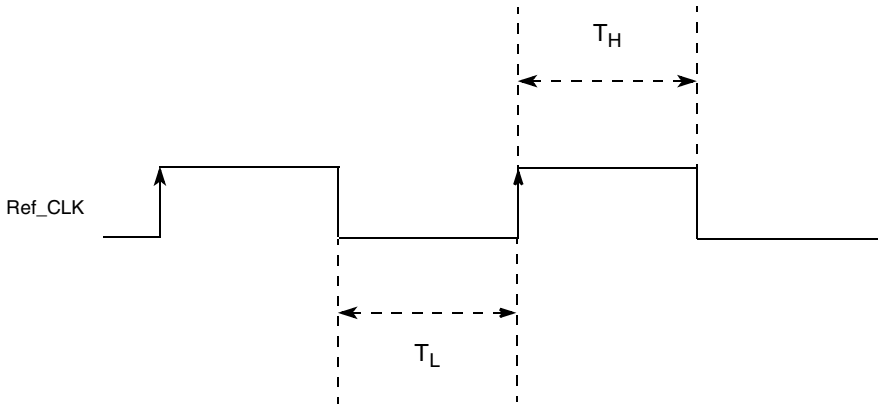



**Figure 49. Reference Clock Timing Waveform**

## 2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

### 2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

**Table 65. GPIO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | – 0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**

1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 66. GPIO Input and Output AC Timing Specifications[1]**

| Characteristic | Symbol [2] | Min | Unit | Notes |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 7.5 | ns | 3 |
| GPIO outputs—minimum pulse width | $t_{GTOWID}$ | 12 | ns | — |

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

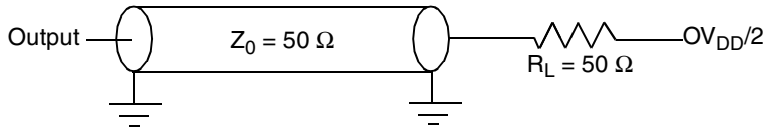



**Figure 53. GPIO AC Test Load**

### 2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the chip's SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 59 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SnGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SnGND). Figure 60 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SDn\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 61 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SDn\_REF\_CLK}}$) through the same source impedance as the clock input (SDn_REF_CLK) in use.

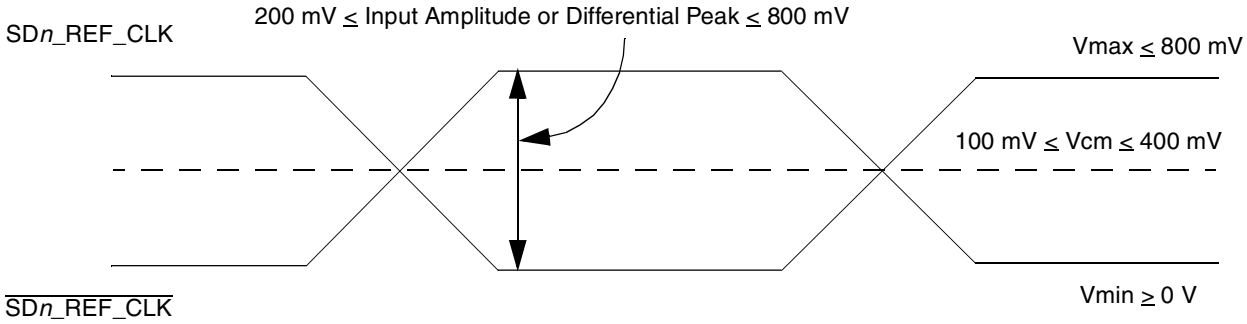



**Figure 59. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

**Table 72. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $L_{TX-SKEW}$ | Total Skew | — | — | 20 | ns | Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 71 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 70). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 71). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 2.22 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 70 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 71) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 70) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 71). Note that the series capacitors, CTX, are optional for the return loss measurement.

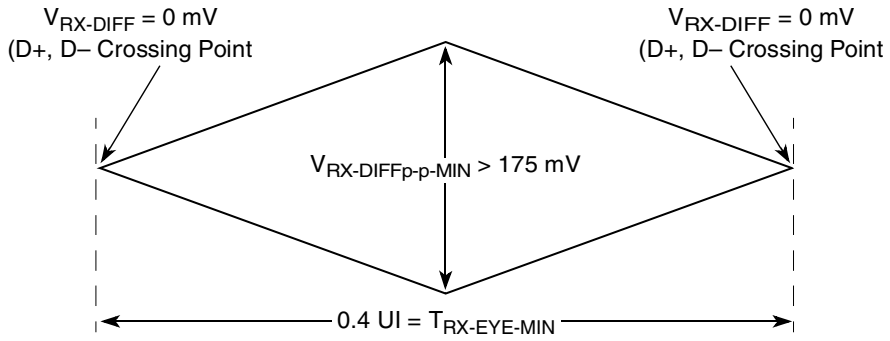



**Figure 70. Minimum Receiver Eye Timing and Voltage Compliance Specification**

## 2.22.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in the following figure.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

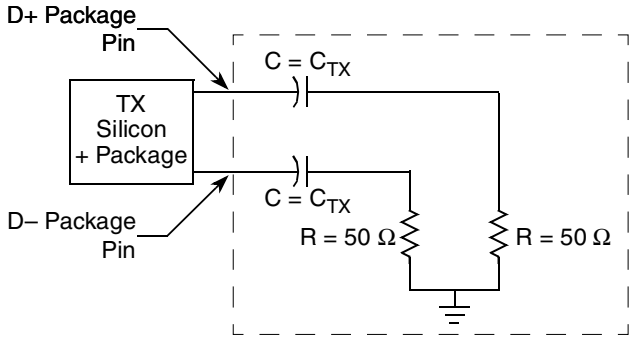



**Figure 71. Compliance Test/Measurement Load**

# 2.23 Clocking

This section describes the PLL configuration of the chip. Note that the platform clock is identical to the core complex bus (CCB) clock.

**Table 79. Package Thermal Characteristics (continued)**

| Characteristic | JEDEC Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JA}$ | 14 | °C/W | 1, 2 |
| Junction-to-board thermal | — | $R_{\theta JB}$ | 10 | °C/W | 3 |
| Junction-to-case thermal | — | $R_{\theta JC}$ | < 0.1 | °C/W | 4 |

**Notes**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 •C/W

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.For system thermal modeling, the chip's thermal model without a lid is shown in Figure 72 The substrate is modeled as a block 29 x 29 x 1.2 mm with an in-plane conductivity of 19.8 W/m•K and a through-plane conductivity of 1.13 W/m•K. The solder balls and air are modeled as a single block 29 x 29 x 0.5 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 9.6 x 9.57 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 7.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

## 2.24.2 Recommended Thermal Model

This table shows the chip's thermal model.

**Table 80. Thermal Model**

| Conductivity | Value | Units |
|---|---|---|
| **Die (9.6x9.6 × 0.85 mm)** | | |
| Silicon | Temperature dependent | — |
| **Bump/Underfill (9.6 x 9.6 × 0.07 mm) Collapsed Thermal Resistance** | | |
| Kz | 7.5 | W/m•K |
| **Substrate (29 × 29 × 1.2 mm)** | | |
| Kx | 19.8 | W/m•K |
| Ky | 19.8 | |
| Kz | 1.13 | |
| **Solder and Air (29 × 29 × 0.5 mm)** | | |
| Kx | 0.034 | W/m•K |
| Ky | 0.034 | |
| Kz | 12.1 | |

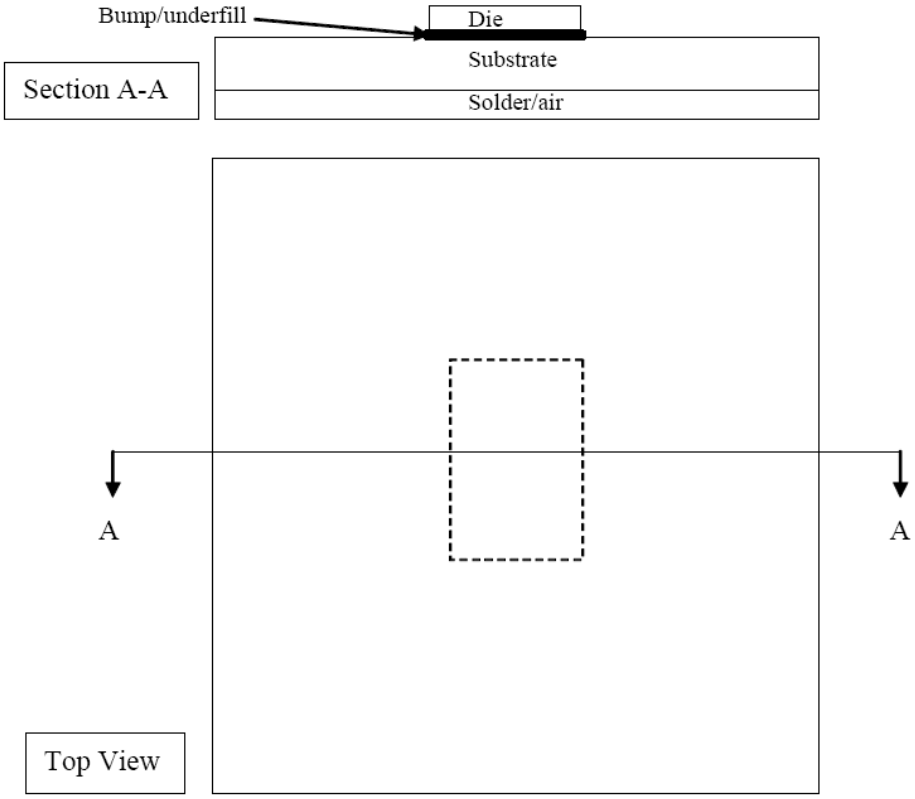



**Figure 72. System-Level Thermal Model for the Chip (Not to Scale)**

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

## 2.24.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

This figure shows the PLL power supply filter circuit.

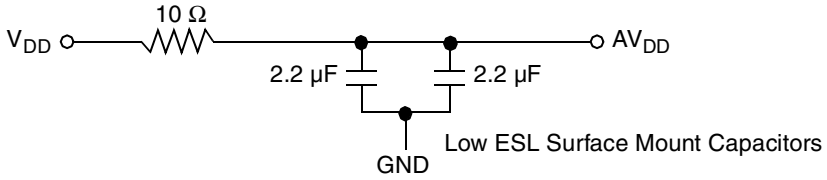
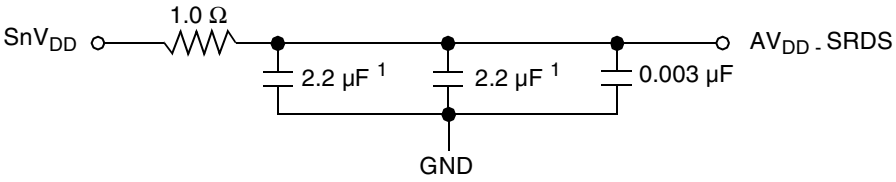



**Figure 75. Chip PLL Power Supply Filter Circuit**

The $AV_{DD}$_SRDS*n* signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 76. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the $AV_{DD}$_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from $AV_{DD}$_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.




1. An 0805 sized capacitor is recommended for system initial bring-up

**Figure 76. SerDes PLL Power Supply Filter Circuit**

Note the following:

- $AV_{DD}$ should be a filtered version of $SV_{DD}$.
- Signals on the SerDes interface are fed from the $XV_{DD}$ power plane.

## 3.3 Pin States in Deep Sleep State

In all low power mode by default, all input and output pads remain driven as per normal functional operation. The inputs remain enabled.

The exception is that in Deep Sleep mode, GCR[DEEPSLEEP_Z] can be used to tristate a subset of output pads, and disable the receivers of input pads as defined in Table 1. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for details.

## 3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, this chip can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ pin of the chip. These decoupling capacitors should receive their power from separate $V_{DD}$,$TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the chip using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it should be routed with short and large trace to minimize the inductance.

The following pins must be connected to XGND if not used:

- SD1_RX[7:4]
- $\overline{\text{SD1\_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

### 3.11.3 SerDes 2 Interface Entirely Unused

If the high-speed SerDes 2 interface (SGMII/ SATA) is not used at all, the unused pin should be terminated as described in this section. There are several Reserved pins that need to be either left floating or connected to X2GND. See SerDes2 in Table 1Table 1 for details.

The following pins must be left unconnected (float):

- SD2_TX[0]
- $\overline{\text{SD2\_TX[0]}}$
- Reserved pins L8, L9

The following pins must be connected to X2GND:

- SD2_RX[0]
- $\overline{\text{SD2\_RX[0]}}$
- SD2_REF_CLK
- $\overline{\text{SD2\_REF\_CLK}}$

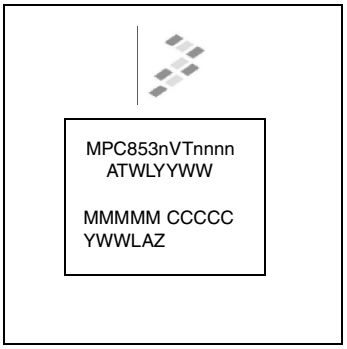
The POR configuration pin cfg_srds2_prtcl[0:2] on TSEC1_TXD[2], TSEC3_TXD[2], TSEC_1588_PUSLE_OUT1 can be used to power down SerDes 2 block for power saving. Note that both S2VDD and X2VDD must remain powered.

# 4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, “Part Numbers Fully Addressed by this Document.”

## 4.2 Part Marking

Parts are marked as in the example shown in the following figure.




FC-PBGA

**Notes:**

MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 80. Part Marking for FC-PBGA**

## 4.3 Part Numbering

These tables list all part numbers that are offered for the chip.

**Table 83. MPC8535 Part Numbers Commercial Tier**

| Core/Platform/ DDR (MHz) | Standard Temp Without Security | Standard Temp With Security | Notes |
|---|---|---|---|
| 600/400/400 | MPC8535AVTAKG(A) | MPC8535EAVTAKG(A) | — |
| 800/400/400 | MPC8535AVTANG(A) | MPC8535EAVTANG(A) | — |
| 1000/400/400 | MPC8535AVTAQG(A) | MPC8535EAVTAQG(A) | — |
| 1250/500/500 | MPC8535AVTATH(A) | MPC8535EAVTATH(A) | — |
| 1250/500/667 | MPC8535AVTATLA | MPC8535EAVTATLA | — |

**Table 84. MPC8535 Part Numbers Industrial Tier**

| Core/Platform/ DDR (MHz) | Standard Temp Without Security | Standard Temp With Security | Extended Temp Without Security | Extended Temp With Security | Notes |
|---|---|---|---|---|---|
| 600/400/400 | MPC8535BVTAKG(A) | MPC8535EBVTAKG(A) | MPC8535CVTAKG(A) | MPC8535ECVTAKG(A) | 1 |
| 800/400/400 | MPC8535BVTANG(A) | MPC8535EBVTANG(A) | MPC8535CVTANG(A) | MPC8535ECVTANG(A) | |
| 1000/400/400 | MPC8535BVTAQG(A) | MPC8535EBVTAQG(A) | MPC8535CVTAQG(A) | MPC8535ECVTAQG(A) | |
| 1250/500/500 | MPC8535BVTATH(A) | MPC8535EBVTATH(A) | MPC8535CVTATH(A) | MPC8535ECVTATH(A) | |
| 1250/500/667 | MPC8535BVTATLA | MPC8535EBVTATLA | MPC8535CVTATLA | MPC8535ECVTATLA | |

**Note:**

1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A

5. Capacitors may not be present on all devices
6. Caution must be taken not to short exposed metal capacitor pads on package top.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

# 6 Product Documentation

The following documents are required for a complete description of the chip and are needed to design properly with the part.

- *MPC8536E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8536ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)

# 7 Document Revision History

This table provides a revision history for this hardware specification.

**Table 85. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 5 | 09/2011 | • Removed PVDD from Table 1, “Pinout Listing.” |
| 4 | 06/2011 | • In Table 1, “Pinout Listing,” updated the power supply for TSEC3 pins to TVDD.<br>• Updated Table 56, “eSDHC AC Timing Specifications.”<br>• In Section 4.3, “Part Numbering,” added an extra bin (1250/500/667) to support DDR3. |
| 3 | 11/2010 | • In Table 1, “Pinout Listing,” added the following note: “For systems that boot from Local Bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required...” In addition, updated footnote 26 and added footnote 29 to PCI1_AD.<br>• Updated Table 21<br>• Updated Figure 25, “RGMII and RTBI AC Timing and Multiplexing Diagrams.”<br>• In Table 44, “MII Management DC Electrical Characteristics,” changed the Voh/Vol values for MDIO/MDC.<br>• Added Note 6 regarding USB*n*_DIR pin to Table 47, “USB General Timing Parameters6.”<br>• In Table 64, “I2C AC Electrical Specifications,” updated footnote 2.<br>• In Table 82, , Table 83, , Table 84, added the Revision Level A for Rev 1.2 |
| 2 | 09/2009 | **Note:**<br>• In Section 1, “Pin Assignments and Reset States,”updated the first sentence of the note to say, “The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration.”<br>• In Table 40, “SGMII DC Receiver Electrical Characteristics,” changed LSTSAB to LSTSA and LSTSEF to LSTSE for Note 4.<br>• Updated Die value and Bump/Underfill value in Table 84<br>**Note:** Updated Figure 81, “Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA,” and its notes. |
| 1 | 09/2009 | • In Table 3, “Recommended Operating Conditions,” for $V_{DD\_CORE}$, removed 1.1 ± 55 mV.<br>• In Table 5, “Power Dissipation 5,” remove note 5.<br>• In Table 5, ”Power Dissipation 5,” changed an “—” to “0.” |
| 0 | 08/2009 | • Initial public release. |