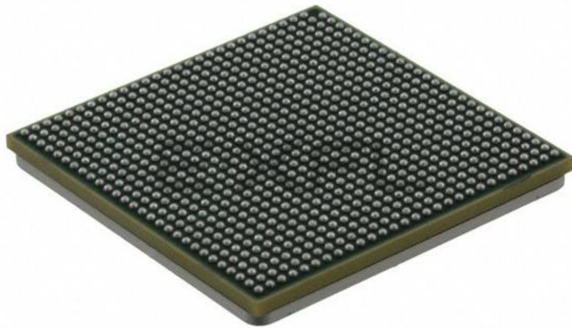

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8536eavjanga

	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH
1	MDQ[59]	AVDD_SRDS2	TSEC3_RX_CLK	TSEC3_RXD[3]	TSEC1_TX_EN	TSEC1_RXD[1]	TSEC1_RX_DV	USB1_D[0]	USB1_D[2]	USB1_CLK	USB1_D[5]	USB1_D[7]	USB1_STP	USB1_DIR
2	MDQ[63]	AGND_SRDS2	TSEC3_RXD[1]	TSEC3_RX_DV	TSEC1_GTX_CLK	TSEC1_RXD[0]	TSEC1_RXD[3]	USB1_D[1]	USB1_D[3]	USB1_D[4]	USB1_D[6]	USB1_NXT	OV_{DD}	USB1_PWRFAULT
3	GV_{DD}	SD2_PLL_TPA	TSEC3_RXD[2]	TSEC3_RXD[0]	TSEC1_TXD[3]	TSEC1_RXD[2]	TSEC1_RX_CLK	TSEC1_RXD[7]	USB1_PCTL0/GPIO[6]	USB2_D[0]	USB2_D[1]	GND	USB3_D[1]	USB3_D[0]
4	Rvsd	TSEC3_RX_ER	GND	TV_{DD}	TSEC1_TXD[1]	GND	LV_{DD}	TSEC1_TX_CLK	USB1_PCTL1/GPIO[7]	OV_{DD}	USB2_D[2]	USB2_D[3]	USB3_D[3]	USB3_D[2]
5	Rvsd	TSEC3_TXD[1]	TSEC3_GTX_CLK	TSEC3_TX_EN	TSEC1_TXD[2]	TSEC1_TXD[4]	TSEC1_TXD[6]	TSEC1_TX_ER	GND	USB2_CLK	USB2_D[4]	USB2_D[5]	USB3_D[4]	USB3_CLK
6	$S2V_{DD}$	TSEC3_TXD[0]	TSEC3_RXD[5]	TSEC3_RXD[4]	TSEC1_TXD[0]	TSEC1_RXD[4]	EC_GTX_CLK125	TSEC1_COL	USB2_D[6]	DMA_DACK[0]/GPIO[10]	USB2_D[7]	OV_{DD}	USB3_D[6]	USB3_D[5]
7	SD2_IMP_CAL_RX	TSEC3_TXD[2]	TV_{DD}	GND	TSEC_1588_TRIG_IN[1]	GND	LV_{DD}	TSEC1_RXD[6]	USB2_NXT	USB2_STP	GND	USB2_DIR	USB3_NXT	USB3_D[7]
8	NC	TSEC3_TXD[3]	TSEC3_TXD[5]	TSEC3_TXD[6]	TSEC_1588_TRIG_IN[0]	TSEC1_TXD[5]	TSEC1_TXD[7]	TSEC1_RXD[5]	USB2_PWRFAULT	SPI_CLK	SDHC_DAT[4]/SPI_CS[0]	SPI_MOSI	USB3_DIR	USB3_STP
9	NC	TSEC3_COL	TSEC3_TX_ER	TSEC3_TXD[4]	TSEC_1588_CLK	TSEC1_RX_ER	TSEC1_CRS	GND	USB2_PCTL1/GPIO[9]	SPI_MISO	GND	SDHC_DAT[6]/SPI_CS[2]	USB2_PCTL0/GPIO[8]	Rsvd
10	NC	TSEC3_CRS	TSEC3_TX_CLK	TSEC_1588_CLK_OUT	TSEC_1588_TRIG_OUT[1]	EC_MDC	SDHC_DAT[7]/SPI_CS[3]	DMA_DREQ[0]/GPIO[14]	SDHC_DAT[5]/SPI_CS[1]	OV_{DD}	DMA_DACK[1]/GPIO[11]	UART_SOUT[0]	SDHC_WP/GPIO[5]	SDHC_CMD
11	$X2V_{DD}$	TSEC_1588_PULSE_OUT2	TSEC_1588_TRIG_OUT[0]	TSEC_1588_PULSE_OUT1	MSRCID[4]	EC_MDIO	DMA_DDONE[0]/GPIO[12]	DMA_DDONE[1]/GPIO[13]	GND	DMA_DREQ[1]/GPIO[15]	UART_CTS[0]	OV_{DD}	SDHC_DAT[3]	SDHC_CD/GPIO[4]
12	X2GND	TSEC3_TXD[7]	TSEC3_RXD[7]	MSRCID[2]	MSRCID[0]	UART_CTS[1]	UART_SOUT[1]	UART_RTS[0]	UART_SIN[0]	UART_RTS[1]	GND	UART_SIN[1]	SDHC_DAT[0]	SDHC_DAT[1]
13	GND	VDD_CORE	TSEC3_RXD[6]	MDVAL	MSRCID[1]	GND	TEST_SEL	OV_{DD}	DDRCLK	IRQ[10]/DMA_DACK[3]	IRQ[9]/DMA_DREQ[3]	PCI1_REQ[2]	SDHC_CLK	SDHC_DAT[2]
14	VDD_CORE	GND	VDD_CORE	GND	MSRCID[3]	MCP	GND	UDE	PCI1_GNT[4]/GPIO[3]	IRQ[11]/DMA_DDONE[3]	OV_{DD}	PCI1_GNT[2]	IIC2_SDA	SYSCLK

DETAIL B

Figure 4. Chip Pin Map Detail B

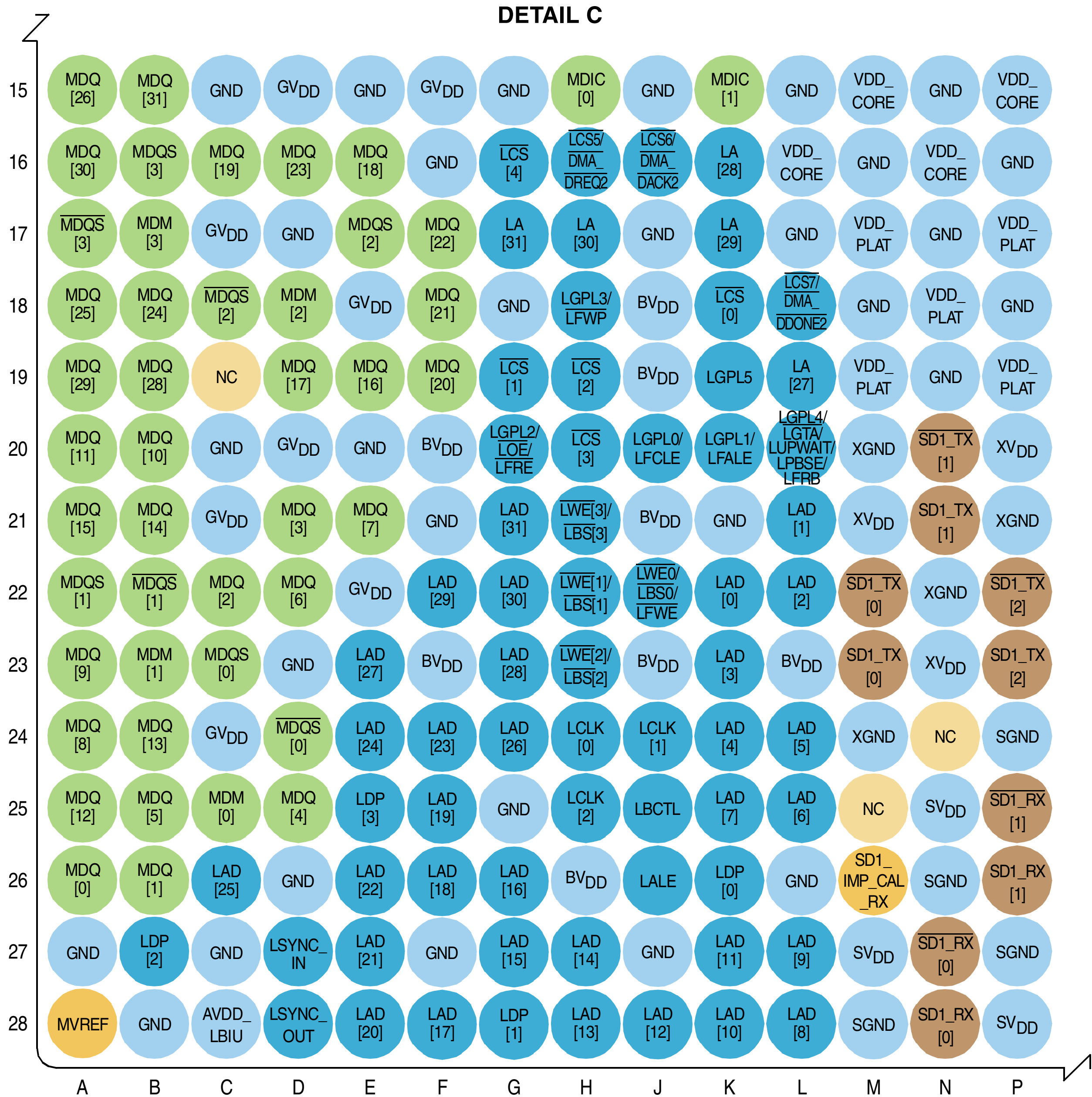
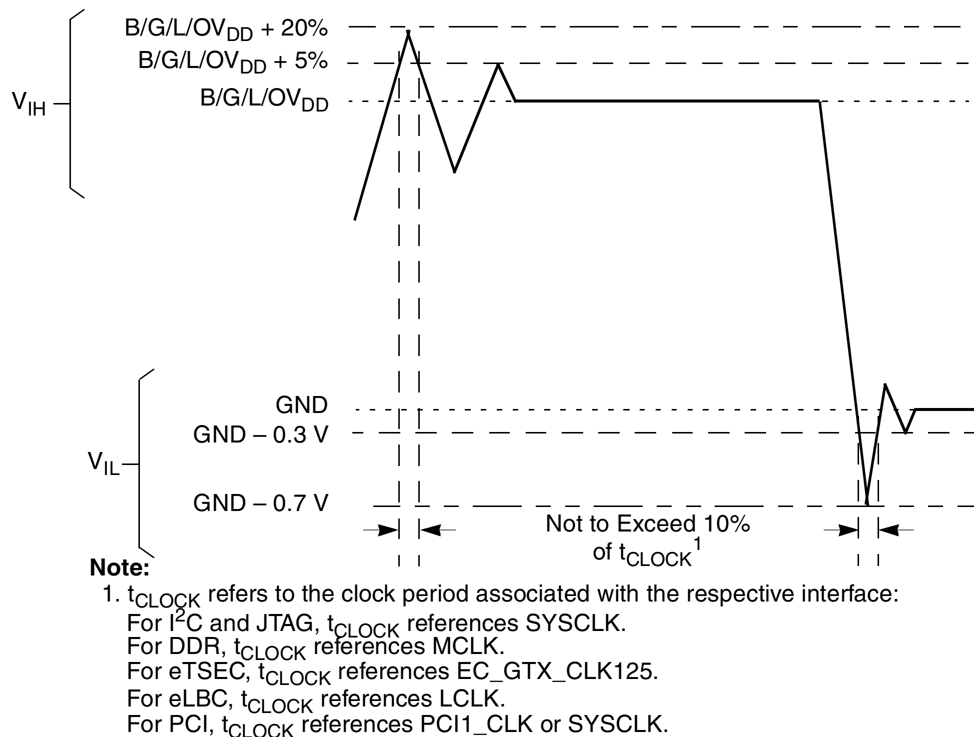


Figure 5. Chip Pin Map Detail C

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ[0:63]	Data	A26,B26,C22,D21,D25, B25,D22,E21,A24,A23, B20,A20,A25,B24,B21, A21,E19,D19,E16,C16, F19,F18,F17,D16,B18, A18,A15,B14,B19,A19, A16,B15,D1,F3,G1,H2, E4,G5,H3,J4,B2,C3,F2, G2,A2,B3,E1,F1,L5,L4, N3,P3,J3,K4,N4,P4,J1, K1,P1,R1,J2,K2,P2,R2	I/O	GV_{DD}	—
MECC[0:7]	Error Correcting Code	G12,D14,F11,C11, G14,F14,C13,D12	I/O	GV_{DD}	—
MAPAR_ERR	Address Parity Error	A13	I	GV_{DD}	—
MAPAR_OUT	Address Parity Out	A6	O	GV_{DD}	—
MDM[0:8]	Data Mask	C25,B23,D18,B17,G4, C2,L3,L2,F13	O	GV_{DD}	—
MDQS[0:8]	Data Strobe	D24,B22,C18,A17,J5, C1,M4,M2,E13	I/O	GV_{DD}	—
MDQS[0:8]	Data Strobe	C23,A22,E17,B16,K5, D2,M3,N1,D13	I/O	GV_{DD}	—
MA[0:15]	Address	B7,G8,C8,A10,D9,C10, A11,F9,E9,B12,A5, A12,D11,F7,E10,F10	O	GV_{DD}	—
MBA[0:2]	Bank Select	A4,B5,B13	O	GV_{DD}	—
MWE	Write Enable	B4	O	GV_{DD}	—
MRAS	Row Address Strobe	C5	O	GV_{DD}	—
MCAS	Column Address Strobe	E7	O	GV_{DD}	—
MCS[0:3]	Chip Select	D3,H6,C4,G6	O	GV_{DD}	—
MCKE[0:3]	Clock Enable	H10,K10,G10,H9	O	GV_{DD}	11
MCK[0:5]	Differential Clock 3 Pairs / DIMM	A9,J11,J6,A8,J13,H8	O	GV_{DD}	—
MCK[0:5]	Differential Clock 3 Pairs / DIMM	B9,H11,K6,B8,H13,J8	O	GV_{DD}	—
MODT[0:3]	On Die Termination	E5,H7,E6,F6	O	GV_{DD}	—
MDIC[0:1]	Calibration	H15,K15	I/O	GV_{DD}	26
Local Bus Controller Interface					

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



2. With the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 7. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The core voltage must always be provided at nominal 1.0 V . (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

Table 5. Power Dissipation (continued)[5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	1250	500	500	1.0	1.0	105 / 90	—	5.3/4.4	—	5.0/4.0	1, 3, 8
Thermal (W)							—	4.4/3.6	—	5.0/4.0	1, 4, 8
Typical (W)						65	2.2		1.7		1
Doze (W)							1.6	2.4	1.5	2.1	1
Nap (W)							0.8	1.6	1.5	2.1	1
Sleep (W)							0.8	1.6	1.1	1.7	1
Deep Sleep (W)						35	0	0	0.6	1.2	1, 6

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage (V_{DD}) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 ^{0}C, for Industrial Tier is 105 ^{0}C.
9. Platform power is the power supplied to all the V_{DD_PLAT} pins.

See Section 2.23.6.1, “SYSCLK to Platform Frequency Options,” for the full range of CCB frequencies that the chip supports.

2.4.6 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. The “platform clock (CCB) frequency” in the following formula refers to the maximum platform (CCB) frequency of the speed bins the part belongs to, which is defined in Table 73.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

2.4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

2.5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the chip. This table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HREST}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	Sysclk	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configurations (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configurations (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1
$\overline{\text{HRESET}}$ rise time	—	1	SYSCLK	—

Notes:

1. SYSCLK is the primary clock input for the chip.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
Local bus PLL	—	50	µs	—
PCI bus lock time	—	50	µs	—

2.9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps) — FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 2.10, “Ethernet Management Interface Electrical Characteristics.”

The electrical characteristics for SGMII is specified in Section 2.9.3, “SGMII Interface Electrical Characteristics.” The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

2.9.1.1 GMII, MII, TBI, RGMII, RMII and RTBI DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in the following tables. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	1.90	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	40	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:

1 LV_{DD} supports eTSECs 1.

2 TV_{DD} supports eTSECs 3.

3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 25. RGMII, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1,2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

1 LV_{DD} supports eTSECs 1.

2 TV_{DD} supports eTSECs 3.

3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

2.9.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

2.9.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 2.4.6, "Platform to FIFO Restrictions."

A summary of the FIFO AC specifications appears in the following tables.

Table 26. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period[2]	t_{FIT}	6.0	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps

Table 26. FIFO Mode Transmit AC Timing Specification (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}[1]	0.5	—	3.0	ns

Note:

1. Data valid t_{FITDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time – Max Hold)
2. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, “Platform to FIFO Restrictions,” for more detailed description.

Table 27. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period[1]	t_{FIR}	6.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Note:

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, “Platform to FIFO Restrictions,” for more detailed description.

Timing diagrams for FIFO appear in the following figures.

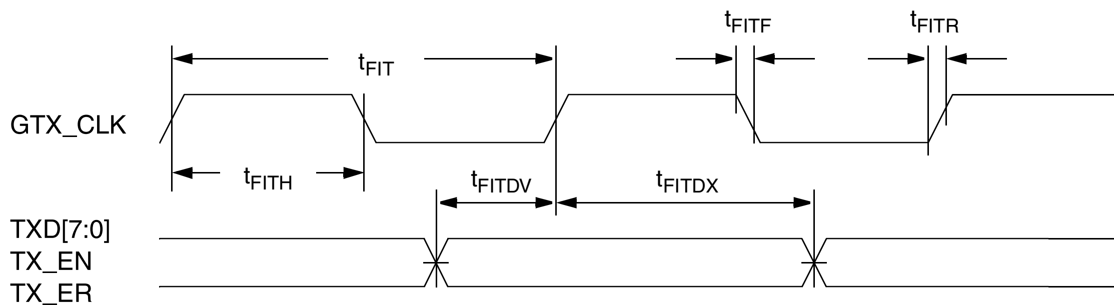


Figure 14. FIFO Transmit AC Timing Diagram

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC) (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V DC.

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	1.9	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.8	—	ns	3

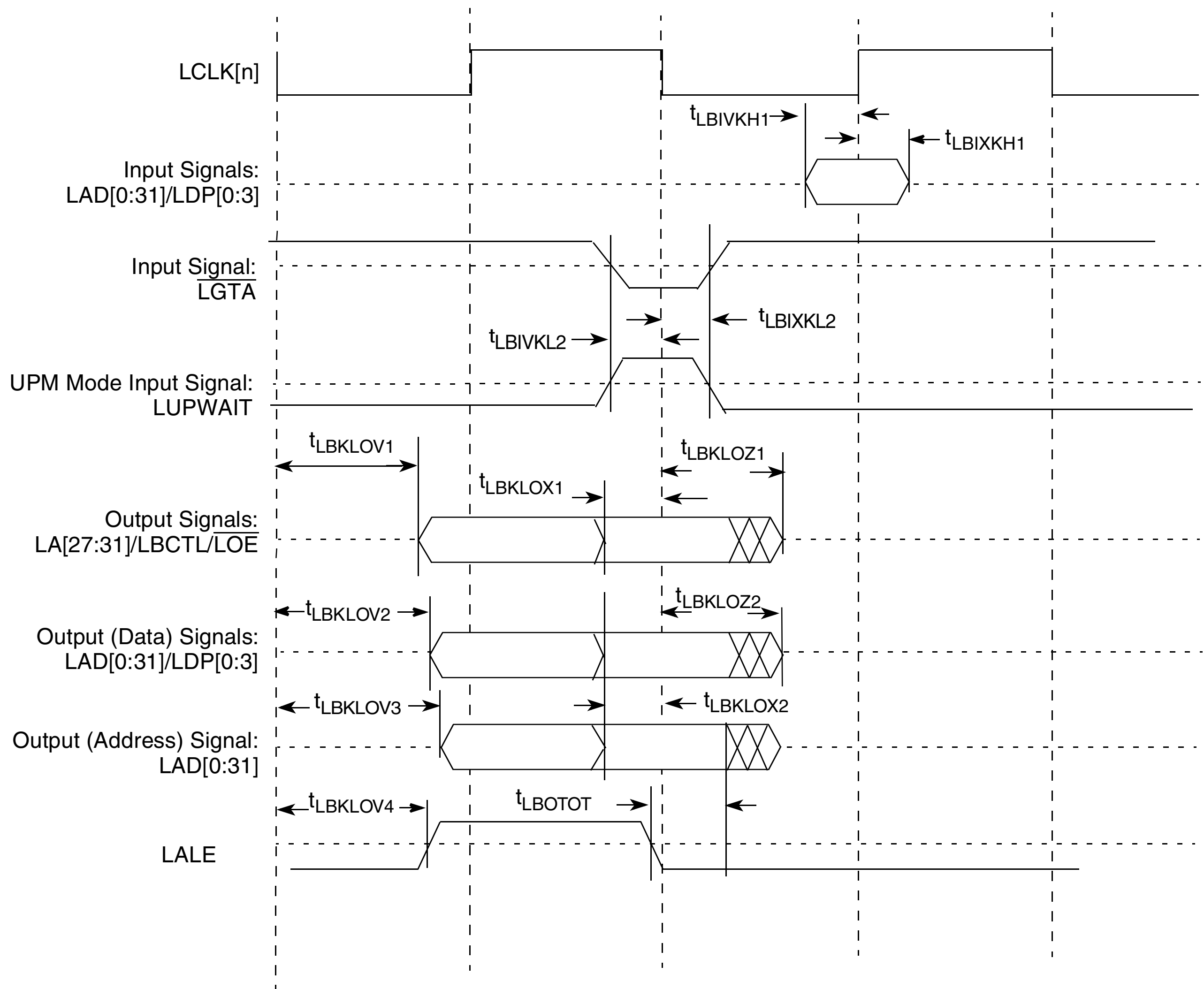


Figure 40. Local Bus Signals (PLL Bypass Mode)

This table describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 54. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	5.1	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	4.2	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	-1.4	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-2.0	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.4	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	0.5	ns	4

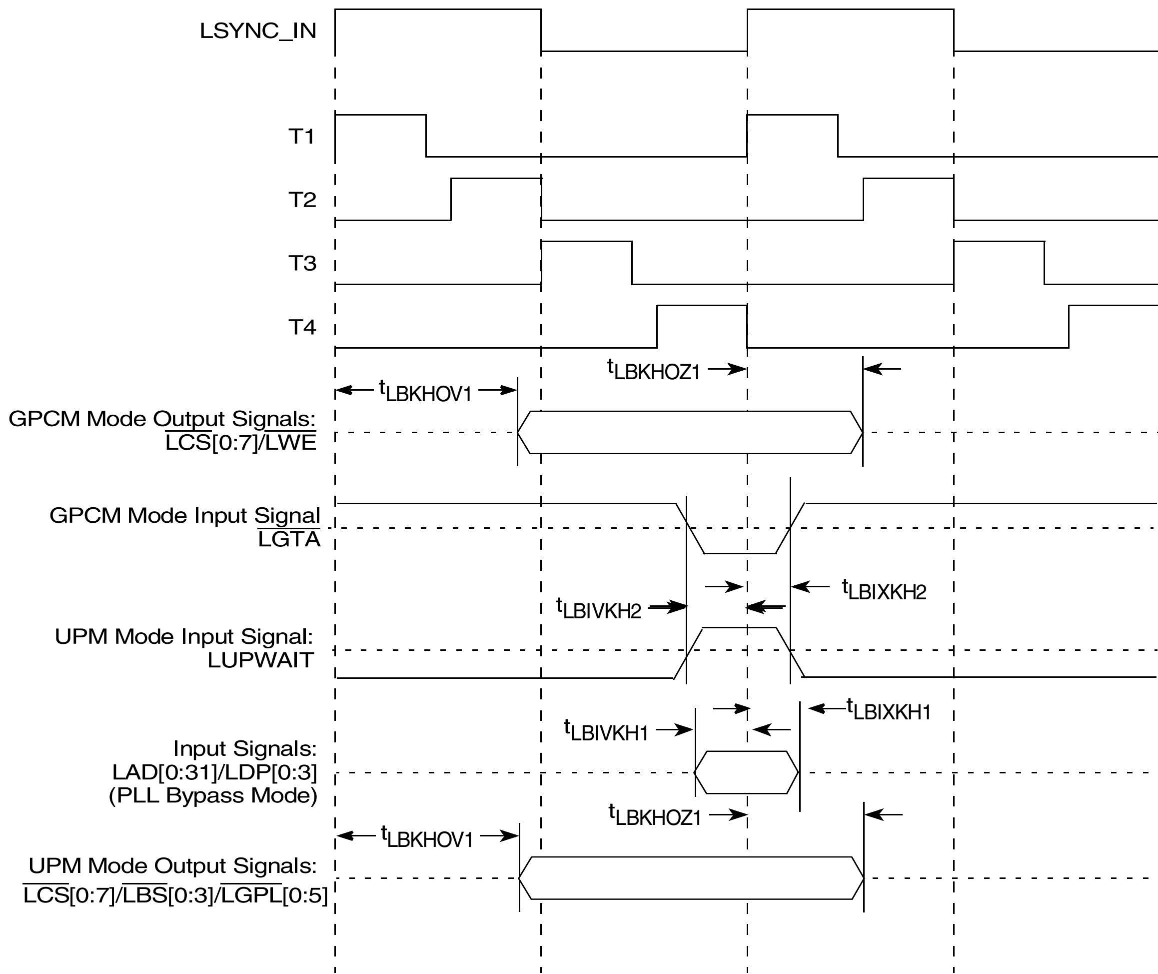


Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 * OVDD	OVDD+0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.25 * OVDD	V	—
Input/Output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—
Output high voltage	V_{OH}	I_{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	—

Table 61. Differential Receiver (RX) Input Characteristics (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
RX Differential Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_RXDD11}	— — — — — —	— — — — — —	18 14 10 8 3 1	dB	2, 3
RX Common Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_RXCC11}	— — — — — —	— — — — — —	5 5 2 2 2 1	dB	2, 3, 4
RX Impedance Balance 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz 1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz	RL_{SATA_RXDC11}	— — — — — —	— — — — — —	30 30 20 10 4 4	dB	2, 3
Deterministic jitter 1.5G 3.0G	U_{SATA_RXDJ}	—	—	0.4 0.47	UI	—
Total Jitter 1.5G 3.0G	U_{SATA_RXTJ}	—	—	0.65 0.65	UI	—

Notes:
1. The min values apply only to Gen1m, and Gen2m. the min values for Gen1i is 325 mVp-p and for Gen2i is 275 mVp-p.
2. Only applies when operating in 3.0Gb data rate mode.
3. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
4. The max value stated for 2.4 GHz - 3.0 GHz range only applies to Gen2i mode for Gen2m the value is 1.
5. Only applies to Gen1i mode.

2.16.4 Out-of-Band (OOB) Electrical Characteristics

This table provides the Out-of-Band (OOB) electrical characteristics for the SATA interface of the chip.

Table 62. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA_OOBDETE}$	50 75	100 125	200 200	mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	646.67	666.67	686.67	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA_UIOOBTXWakeGap}$	—	160	—	UI	—
COMWAKE Gap Detection Windows	$T_{SATA_OOBDetWakeGap}$	55	—	175	ns	—
COMINIT/ COMRESET Gap Detection Windows	$T_{SATA_OOBDetCOMGap}$	175	—	525	ns	—

2.17 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interfaces of the chip.

2.17.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 63. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	OV_{DD}	3.13	3.47	V	—
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

2.20.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 69. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.0V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn_REF_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 66.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 67.

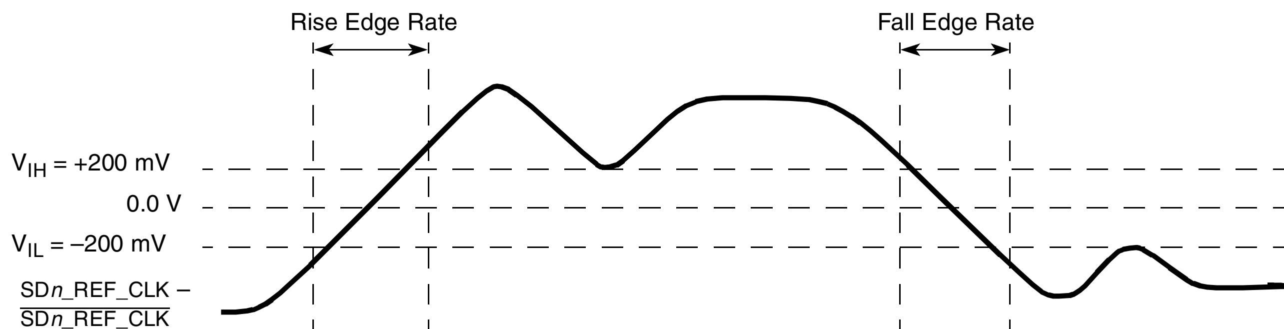


Figure 66. Differential Measurement Points for Rise and Fall Time

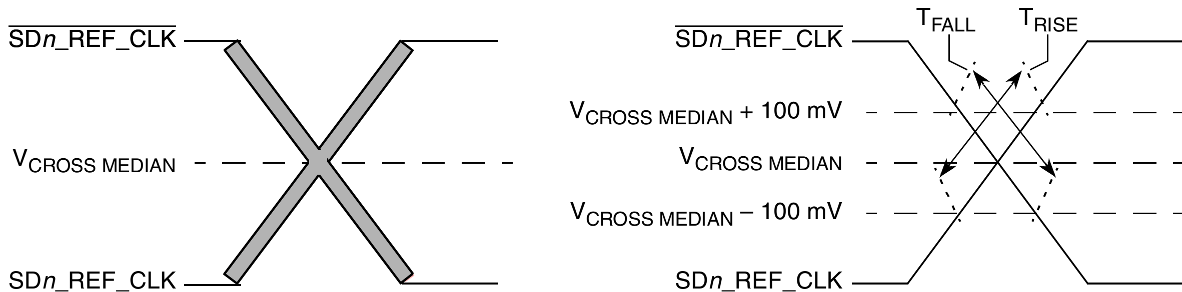


Figure 67. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 2.9.3.2, “AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK”
- Section 2.21.2, “AC Requirements for PCI Express SerDes Clocks”

2.20.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/SD1_REF_CLK were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/SD2_REF_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane’s transmitter and receiver.

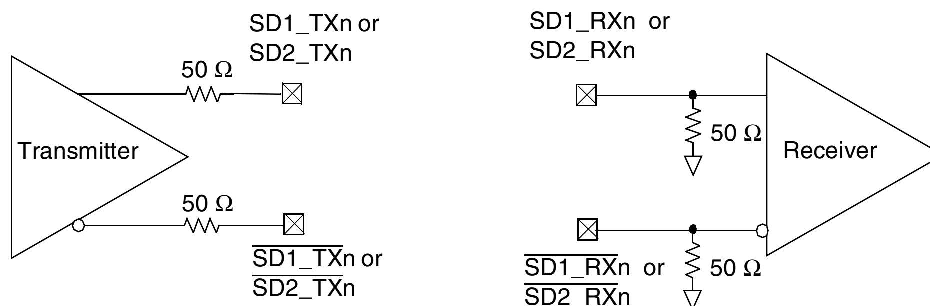


Figure 68. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SATA or SGMII) in this document based on the application usage:

- Section 2.9.3, “SGMII Interface Electrical Characteristics”
- Section 2.21, “PCI Express”
- Section 2.16, “Serial ATA (SATA)”

Please note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

Table 72. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 71 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 70). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 71). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.22 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 70 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 71) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 70) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Table 77. DDR Clock Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	**cfg_ddr_pll[0:2]**	000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, “CCB/SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, “e500 Core PLL Ratio.”
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, “DDR/DDRCLK PLL Ratio.”

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values types and quantity of bulk capacitors.

3.5 SerDes Block Power Supply Decoupling Recommendations

he SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power (SnV_{DD} and XnV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the chip. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the chip as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (SnV_{DD} and XnV_{DD}) to the board ground plane on each side of the chip. This should be done for all SerDes supplies.
- Third, between the chip and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND pins of the chip.

3.7 Pull-Up and Pull-Down Resistor Requirements

The chip requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC1_TXD[3], $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The UART_SOUT[0:1] and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. Please refer to the pinlist table (see Table 62) of the individual chip for more details.

See the PCI 2.2 specification for all pull-ups required for PCI.

3.8 Output Buffer DC Impedance

The chip drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).