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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8536eavjaula

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.1 Pin Map

See Table 1 for the MPC8535E pinout, which is a subset of the MPC8536E.



MPC8535E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 5

Pin Assignments and Reset States

	A	В	С	D	Е	F	G	Н	J	К	L	М	Ν	Р	_/_
1		GV _{DD}	MDQS [5]	MDQ [32]	MDQ [46]	MDQ [47]	MDQ [34]	GND	MDQ [56]	MDQ [57]	GND	GV _{DD}	MDQS [7]	MDQ [58]	N
2	MDQ [44]	MDQ [40]	MDM [5]	MDQS [5]	GV _{DD}	MDQ [42]	MDQ [43]	MDQ [35]	MDQ [60]	MDQ [61]	MDM [7]	MDQS [7]	GND	MDM [62]	
3	GND	MDQ [45]	MDQ [41]	MCS [0]	GND	MDQ [33]	GV _{DD}	MDQ [38]	MDQ [52]	GV _{DD}	MDM [6]	MDQS [6]	MDQ [50]	MDQ [51]	
4	MBA [0]	MWE	MCS [2]	GV _{DD}	MDQ [36]	GND	MDM [4]	GND	MDQ [39]	MDQ [53]	MDQ [49]	MDQS [6]	MDQ [54]	MDQ [55]	
5	MA [10]	MBA [1]	MRAS	GND	MODT [0]	GV _{DD}	MDQ [37]	GV _{DD}	MDQS [4]	MDQS [4]	MDQ [48]	GND	GV _{DD}	GND	
6	MAPAR_ OUT	NC	GND	GV _{DD}	MODT [2]	MODT [3]	MCS [3]	MCS [1]	MCK [2]	MCK [2]	SD2_ IMP_CAL _TX	SD2_ REF_ CLK	S2GND	SD2_RX [0]	
7	GND	MA [0]	GV _{DD}	NC	MCAS	MA [13]	GV _{DD}	MODT [1]	NC	GND	SD2_ PLL_ TPD	SD2_ REF_ CLK	S2V _{DD}	SD2_RX [0]	
8	MCK [3]	MCK [3]	MA [2]	GND	GV _{DD}	GND	MA [1]	MCK [5]	MCK [5]	GND	Rsvd	S2GND	SD2_RX [1]	S2GND	
9	MCK [0]	<u>МСК</u> [0]	GV _{DD}	MA [4]	MA [8]	MA [7]	GV _{DD}	MCKE [3]	NC	NC	Rsvd	S2V _{DD}	SD2_RX [1]	S2GND	
10	MA [3]	GND	MA [5]	NC	MA [14]	MA [15]	MCKE [2]	MCKE [0]	GV _{DD}	MCKE [1]	NC	X2GND	NC	NC	
11	MA [6]	gv _{DD}	MECC [3]	MA [12]	GV _{DD}	MECC [2]	GV _{DD}	<u>МСК</u> [1]	MCK [1]	GND	X2V _{DD}	SD2_TX [1]	X2GND	SD2_TX [0]	
12	MA [11]	MA [9]	GND	MECC [7]	GND	NC	MECC [0]	GV _{DD}	GND	GV _{DD}	X2GND	SD2_TX [1]	X2V _{DD}	SD2_TX [0]	
13	MAPAR_ ERR	MBA [2]	MECC [6]	MDQS [8]	MDQS [8]	MDM [8]	GND	MCK [4]	MCK [4]	VDD_ CORE	GND	VDD_ CORE	GND	VDD_ CORE	
14	GND	MDQ [27]	GV _{DD}	MECC [1]	GV _{DD}	MECC [5]	MECC [4]	GV _{DD}	GND	GV _{DD}	VDD_ CORE	GND	VDD_ CORE	GND	1
7							DET								

Figure 3. Chip Pin Map Detail A

This table provides the pin-out listing for the 783 FC-PBGA package.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes				
PCI									
PCI1_AD[31:0]	Muxed Address / data	AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26	I/O	OV _{DD}	_				
PCI1_C_BE[3:0]	Command/Byte Enable	AD18, AD20,AD22, AH25	I/O	OV _{DD}	29				
PCI1_PAR	Parity	AC22	I/O	OV _{DD}	29				
PCI1_FRAME	Frame	AE20	I/O	OV _{DD}	2,29				
PCI1_TRDY	Target Ready	AF21	I/O	OV _{DD}	2,29				
PCI1_IRDY	Initiator Ready	AB20	I/O	OV _{DD}	2,29				
PCI1_STOP	Stop	AD21	I/O	OV _{DD}	2,29				
PCI1_DEVSEL	Device Select	AC21	I/O	OV _{DD}	2,29				
PCI1_IDSEL	Init Device Select	AE16	I	OV _{DD}	29				
PCI1_PERR	Parity Error	AB21	I/O	OV _{DD}	2,29				
PCI1_SERR	System Error	AF22	I/O	OV _{DD}	2,4,29				
PCI1_REQ[4:3]/GPIO[1:0]	Request	AE15,Y15	I	OV _{DD}	—				
PCI1_REQ[2:1]	Request	AF13,W16	I	OV _{DD}	29				
PCI1_REQ[0]	Request	AA16	I/O	OV _{DD}	29				
PCI1_GNT[4:3]/GPIO[3:2]	Grant	AC14, AA15	0	OV _{DD}					
PCI1_GNT[2:1]	Grant	AF14,Y16	0	OV _{DD}	5,9,25,29				
PCI1_GNT[0]	Grant	W18	I/O	OV _{DD}	29				
PCI1_CLK	PCI Clock	AH26	I	OV _{DD}	29				

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	_	XV _{DD}	_
S2VDD	SerDes 2 core logic supply	R6,N7,M9		S2V _{DD}	_
X2VDD	SerDes 2 transceiver supply	R11,N12,L11		X2V _{DD}	_
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13		V _{DD_CORE}	
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	_	V _{DD_PLAT}	
AVDD_CORE	CPU PLL supply	AH16	—	$AV_{DD_{CORE}}$	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV _{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV _{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV _{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV _{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	_	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V _{DD_CORE}	13
SENSEVDD_PLAT	_	W17	—	V _{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13			_
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	_	-	_

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND	SerDes 1 Transceiver core logic GND (xcorevss)	M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28	_		_
X2GND	SerDes 2 Transceiver pad GND (xpadvss)	R12,M10,N11,L12	—	—	—
S2GND	SerDes 2 Transceiver core logic GND (xcorevss)	P8,P9,N6,M8	—	—	—
AGND_SRDS	SerDes 1 PLL GND	V27	—	—	_
AGND_SRDS2	SerDes 2 PLL GND	T2	—	—	_
SENSEVSS	GND Sensing	V16	—	—	13
	Analog	g Signals			
MVREF	SSTL2 reference voltage	A28	Reference voltage for DDR	GVDD/2	
SD1_IMP_CAL_RX	Rx impedance calibration	M26		200Ω (±1%) to GND	_
SD1_IMP_CAL_TX	Tx impedance calibration	AE28	—	100Ω (±1%) to GND	—
SD1_PLL_TPA	PLL test point analog	V26	—	AVDD_SRD S analog	18
SD2_IMP_CAL_RX	Rx impedance calibration	R7	_	200Ω (±1%) to GND	_
SD2_IMP_CAL_TX	Tx impedance calibration	L6		100Ω (±1%) to GND	_
SD2_PLL_TPA	PLL test point analog	Т3		AVDD_SRD S2 analog	18
Reserved	—	R4	—	—	_
Reserved	—	R5	_	—	_
	No Con	nect Pins			
NC	_	C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9	_	—	

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
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Notes:

- 1. All multiplexed signals may be listed only once and may not re-occur.
- 2. Recommend a weak pull-up resistor (2–10 K Ω) be placed on this pin to OV_{DD}.
- 3. This pin must always be pulled-high.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
- 8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
- 10.For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V_{DD_CORE}/V_{DD_PLAT}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
- 16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 17. This pin is only an output in FIFO mode when used as Rx Flow Control.
- 18. Do not connect.
- 19.These must be pulled up (100 Ω 1 k Ω) to OVDD.
- 20. Independent supplies derived from board VDD.
- 21. Recommend a pull-up resistor (1 K Ω) be placed on this pin to OV_{DD}.
- 22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP.
- 23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
- 24. General-Purpose POR configuration of user system.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings¹

	Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltag	e	V _{DD_CORE}	-0.3 to 1.21	V	—
Platform supply vo	Itage	V _{DD_PLAT}	-0.3 to 1.1	V	—
PLL core supply vo	oltage	AV _{DD_CORE}	-0.3 to 1.21	V	
PLL other supply v	oltage	AV _{DD}	-0.3 to 1.1	V	
Core power supply	for SerDes transceivers	SV_DD , $\mathrm{S2V}_\mathrm{DD}$	-0.3 to 1.1	V	—
Pad power supply	for SerDes transceivers and PCI Express	XV _{DD,} X2V _{DD}	-0.3 to 1.1	V	
DDR SDRAM	DDR2 SDRAM Interface	GV _{DD}	–0.3 to 1.98	V	—
Controller I/O supply voltage DDR3 SDRAM Interface			-0.3 to 1.65		
Three-speed Ether	net I/O	LV _{DD} (eTSEC1)	-0.3 to 3.63 -0.3 to 2.75	V	2
		TV _{DD} (eTSEC3)	-0.3 to 3.63 -0.3 to 2.75	V	2
PCI, DUART, syste eSDHC, eSPI and	m control and power management, I ² C, USB, JTAG I/O voltage, MII management voltage	OV _{DD}	-0.3 to 3.63	V	
Local bus I/O volta	ge	BV _{DD}	-0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98	V	_
Input voltage	DDR2/DDR3 DRAM signals	MV _{IN}	-0.3 to (GV _{DD} + 0.3)	V	3
	DDR2/DDR3 DRAM reference	MV _{REF}	-0.3 to (GV _{DD} + 0.3)	V	
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	-0.3 to (LV _{DD} + 0.3) -0.3 to (TV _{DD} + 0.3)	V	3
	Local bus signals	BV _{IN}	-0.3 to (BV _{DD} + 0.3)	V V V V V V V V V V V V V V V V V V V	—
	PCI, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	I V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 1 V 3 V 3 V 3 V 3 V 3 V 3 V 3 V 3 V 3 V 3 V 5 V 3 V 5 V 3 V 5 V 3 V 5 V 3 V 5 V 3 V 5 V 3 V 0 0.3) V 0.3) 0 0	3
Storage temperatu	re range	T _{STG}	-55 to 150	$\begin{array}{c ccccc} 3.63 & V \\ 2.75 & & \\ 3.63 & V \\ 3.63 & V \\ 3.63 & V \\ 2.75 & \\ 1.98 & & \\ DD + 0.3) & V \\ DD + 0.3) & V \\ DD + 0.3) & V \\ DD + 0.3) & & \\ DD + 0.3) & V \\ 150 & ^{0}C & \\ \end{array}$	

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.

The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.

3. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

	Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage		V _{DD_CORE}	1.0 ± 50 mV	V	—
Platform supply voltag	le	V _{DD_PLAT}	1.0 ± 50 mV	V	—
PLL core supply voltage	ge	AV _{DD_CORE}	1.0 ± 50 mV	V	2
PLL other supply volta	age	AV _{DD}	1.0 ± 50 mV	V	2
Core power supply for	SerDes transceivers	SV _{DD}	1.0 ± 50 mV	V	_
Pad power supply for	SerDes transceivers and PCI Express	XV _{DD}	1.0 ± 50 mV	V	_
DDR SDRAM	DDR2 SDRAM Interface	GV _{DD}	1.8 V ± 90 mV	V	3
voltage	DDR3 SDRAM Interface	Symbol Recommended Value Uni V_{DD_CORE} $1.0 \pm 50 \text{ mV}$ V V_{DD_PLAT} $1.0 \pm 50 \text{ mV}$ V AV_{DD_CORE} $1.0 \pm 50 \text{ mV}$ V AV_{DD} $1.0 \pm 50 \text{ mV}$ V AV_{DD} $1.0 \pm 50 \text{ mV}$ V AV_{DD} $1.0 \pm 50 \text{ mV}$ V SV_{DD} $1.0 \pm 50 \text{ mV}$ V GV_{DD} $1.8 \text{ V} \pm 90 \text{ mV}$ V $I.S \text{ V} \pm 125 \text{ mV}$ V $2.5 \text{ V} \pm 125 \text{ mV}$ V $SB, eSDHC,$ OV_{DD} $3.3 \text{ V} \pm 165 \text{ mV}$ V BV_{DD} $3.3 \text{ V} \pm 165 \text{ mV}$ V $2.5 \text{ V} \pm 125 \text{ mV}$ $1.8 \text{ V} \pm 90 \text{ mV}$ V BV_{DD} $GND \text{ to GV_{DD}$ V $2.5 \text{ V} \pm 125 \text{ mV}$ V D D V			
Three-speed Ethernet	t I/O voltage	LV _{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	5
		TV _{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, system of eSPI and JTAG I/O vo	control and power management, I ² C, USB, eSDHC, Itage, MII management voltage	OV _{DD}	3.3 V ± 165 mV	V	4
Local bus I/O voltage		BV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Platform supply voltage PLL core supply voltage PLL other supply voltage Core power supply for SerDes transform Pad power supply for SerDes transform DDR SDRAM DDR2 SE Controller I/O supply DDR3 SE Three-speed Ethernet I/O voltage PCI, DUART, system control and eSPI and JTAG I/O voltage Input voltage DDR2 and DDR	DDR2 and DDR3 SDRAM Interface signals	MV _{IN}	GND to GV _{DD}	V	3
	DDR2 and DDR3 SDRAM Interface reference	MV _{REF}	GV _{DD} /2 ± 1%	V	—
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	5
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	—
	PCI, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	4
Operating Temperature range	Commercial		T _A = 0 (min) to T _J = 90(max)		
	Industrial standard temperature range		T _A = 0 (min) to T _J = 105 (max)	°C	6
	Extended temperature range	• 0	T _A = -40 (min) to T _J = 105 (max)		

Table 3. Recommended Operating Conditions

Notes:

- 2. This voltage is the input to the filter discussed in Section 3.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
- 3. Caution: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 5. Caution: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 6. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Figure 7. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

The core voltage must always be provided at nominal 1.0 V. (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GVDD of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
<= 667 MHz		$0.9 imes t_{MCK}$			7
MDQS epilogue end	t _{DDKHME}			ns	6
<= 667 MHz		$0.4 imes t_{MCK}$	$0.6 imes t_{MCK}$		7

Note:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8536E PowerQUICC III Integrated Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 7. Maximum DDR2 and DDR3 frequency is 667 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Table 36. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
Rise time TSECn_TX_CLK (20%–80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	2.0	—	10.0	ns

Note:

 The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.



Figure 26. RMII Transmit AC Timing Diagram

2.9.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSECn_RX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSECn_RX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSECn_RX_CLK peak-to-peak jitter	t _{RMRJ}	_	_	250	ps
Rise time TSECn_RX_CLK (20%-80%)	t _{RMRR}	1.0	_	2.0	ns



Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)

2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

Table 55. eSDHC interface DC Electrical Characteristics

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Input high voltage	V _{IH}	—	0.625 * OVDD	OVDD+0.3	V	_
Input low voltage	V _{IL}	—	-0.3	0.25 * OVDD	V	_
Input/Output leakage current	I _{IN} /I _{OZ}	—	-10	10	uA	_
Output high voltage	V _{OH}	I _{OH} = -100 uA @OVDDmin	0.75 * OVDD	—	V	_

This figure provides the AC test load for TDO and the boundary-scan outputs.



Figure 45. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 46. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.



This figure provides the boundary-scan timing diagram.



Figure 48. Boundary-Scan Timing Diagram

2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

Parameter	Symbol	Min	Typical	Max	Units	Notes
RX Differential Mode Return loss 150 MHz - 300 MHz		_	_	18		2, 3
300 MHz - 600 MHz 600 MHz - 1.2 GHz	RL _{SATA_RXDD11}	—	—	14 10	dB	
1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz		_ _ _	_ _ _	8 3 1		
RX Common Mode Return loss 150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz	RL _{SATA_RXCC11}	 	 	5 5 2	dB	2, 3, 4
1.2 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz		 	 	2 2 1		
RX Impedance Balance						2, 3
150 MHz - 300 MHz 300 MHz - 600 MHz 600 MHz - 1.2 GHz	RL _{SATA_RXDC11}	 	 	30 30 20	dB	
2.4 GHz - 2.4 GHz 2.4 GHz - 3.0 GHz 3.0 GHz - 5.0 GHz				10 4 4		
Deterministic jitter 1.5G 3.0G	U _{SATA_RXDJ}	_	_	0.4 0.47	UI	_
Total Jitter 1.5G 3.0G	U _{SATA_RXTJ}	_	_	0.65 0.65	UI	_

Table 61. Differential Receiver (RX) Input Characteristics (continued)

Notes:

1. The min values apply only to Gen1m, and Gen2m. the min values for Gen1i is 325 mVp-p and for Gen2i is 275 mVp-p.

2. Only applies when operating in 3.0Gb data rate mode.

3. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.

4. The max value stated for 2.4 GHz - 3.0 GHz range only applies to Gen2i mode for Gen2m the value is 1.

5. Only applies to Gen1i mode.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the chip's SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
 - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For external DC-coupled connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 59 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
 - For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SnGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SnGND). Figure 60 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
 - The reference clock can also be single-ended. The SDn REF CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with SDn REF CLK either left unconnected or tied to ground.
 - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 61 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.



SDn_REF_CLK

 $Vmin \ge 0 V$

Figure 59. Differential Reference Clock Input DC Requirements (External DC-Coupled)

Symbol	Parameter	Min	Nom	Max	Units	Comments
L _{TX-SKEW}	Total Skew		_	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Table 72. Differential Receiver (RX) Input Specifications (continued)

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 71 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 70). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes see Figure 71). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
- 6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.22 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 70 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 71) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 70) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

2.23.1 Clock Ranges

This table provides the clocking specifications for the processor cores and Table 74 provides the clocking specifications for the memory bus.

	Maximum Processor Core Frequency									
Characteristic	600	MHz	800	MHz	1000	MHz	125	0 MHz	Unit	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	600	600	600	800	600	1000	600	1250	MHz	1, 2
CCB frequency	400	400	400	400	333	400	333	500		
DDR Data Rate	400	400	400	400	400	400	400	500		

Table 73. Processor Core Clocking Specifications

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," Section 2.23.3, "e500 Core PLL Ratio," and Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.

2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. This table provides the clocking specifications for the memory bus.

Table 74	. Memory	Bus	Clocking	Specifications
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	Maximum Process	or Core Frequency			
Characteristic	600, 800, ⁻	1000, 1250	Unit	Notes	
	Min	Мах			
DDR Memory bus clock speed	200	250	MHz	1, 2, 3, 4	

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," Section 2.23.3, "e500 Core PLL Ratio," and Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.

2. The Memory bus clock refers to the chip's memory controllers' MCK[0:5] and MCK[0:5] output clocks, running at half of the DDR data rate.

- 3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
- 4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 2.23.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

Functional Signals	Reset Configuration Name	Value (Binary)	DDR:DDRCLK Ratio
		000	3:1
		001	4:1
TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT	efa ddr pill0:21	010	6:1
		011	8:1
	cig_ddi_ph[0.2]	100	10:1
		101	12:1
		110	Reserved
		111	Synchronous mode

Table 77. DDR Clock Ratio	able 7	7. DDR	Clock	Ratic
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2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

Hardware Design Considerations

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, "CCB/SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, "e500 Core PLL Ratio."
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, "DDR/DDRCLK PLL Ratio."

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

Ordering Information

4.2 Part Marking

Parts are marked as in the example shown in the following figure.



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 80. Part Marking for FC-PBGA

4.3 Part Numbering

These tables list all part numbers that are offered for the chip.

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Notes
600/400/400	MPC8535AVTAKG(A)	MPC8535EAVTAKG(A)	—
800/400/400	MPC8535AVTANG(A)	MPC8535EAVTANG(A)	—
1000/400/400	MPC8535AVTAQG(A)	MPC8535EAVTAQG(A)	—
1250/500/500	MPC8535AVTATH(A)	MPC8535EAVTATH(A)	—
1250/500/667	MPC8535AVTATLA	MPC8535EAVTATLA	—

Table 84. MPC8535 Part Numbers Industrial Tier

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Extended Temp Without Security	Extended Temp With Security	Notes
600/400/400	MPC8535BVTAKG(A)	MPC8535EBVTAKG(A)	MPC8535CVTAKG(A)	MPC8535ECVTAKG(A)	1
800/400/400	MPC8535BVTANG(A)	MPC8535EBVTANG(A)	MPC8535CVTANG(A)	MPC8535ECVTANG(A)	
1000/400/400	MPC8535BVTAQG(A)	MPC8535EBVTAQG(A)	MPC8535CVTAQG(A)	MPC8535ECVTAQG(A)	
1250/500/500	MPC8535BVTATH(A)	MPC8535EBVTATH(A)	MPC8535CVTATH(A)	MPC8535ECVTATH(A)	
1250/500/667	MPC8535BVTATLA	MPC8535EBVTATLA	MPC8535CVTATLA	MPC8535ECVTATLA	

Note:

1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A